TQMa7x
User's Manual

TQMa7x UM 0203
07.01.2022

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	01.08.2017	Petz		First issue
0200	22.02.2018	Petz	All	Complete rework
0201	04.06.2018	Petz	All 1.9 3.2.2.2 Table 14, 3.2.4 3.2.4.1, 3.2.4.2 3.2.5 4.1, 6.6	Typo, formatting, external links updated “IMX7DCEC Data Sheet” added Warning extended Updated Added Removed Updated
0202	24.10.2018	Petz	All 3.2.5.4 3.2.7.4 3.2.5.9, 3.2.7.6 Table 60	Formatting, links updated Power domain added Information added Warnings updated “Package temperature” replaced with “Case temperature” Case temperature DDR3L SDRAM changed to +95 °C
0203	07.01.2022	Kreuzer	All	Complete rework for TQMa7x hardware revision 0200

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TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the system power supply has been switched off. Violation of this guideline may result in damage / destruction of the TQMa7x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa7x circuit diagram
- MBa7x User's Manual
- IMX7DCEC Data Sheet
- IMX7DRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa7x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa7x revision 02xx in combination with the MBa7x revision 02xx and also refers to some software settings.
A certain TQMa7x version does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP i.MX7 Reference Manuals (5), (6).
The TQMa7x is a universal Minimodule based on the NXP ARM® i.MX7 CPU. For i.MX7 details, see Table 7.
The Cortex®-A7 cores of these CPUs are clocked with up to 1 GHz.

2.1 Block diagram i.MX7D

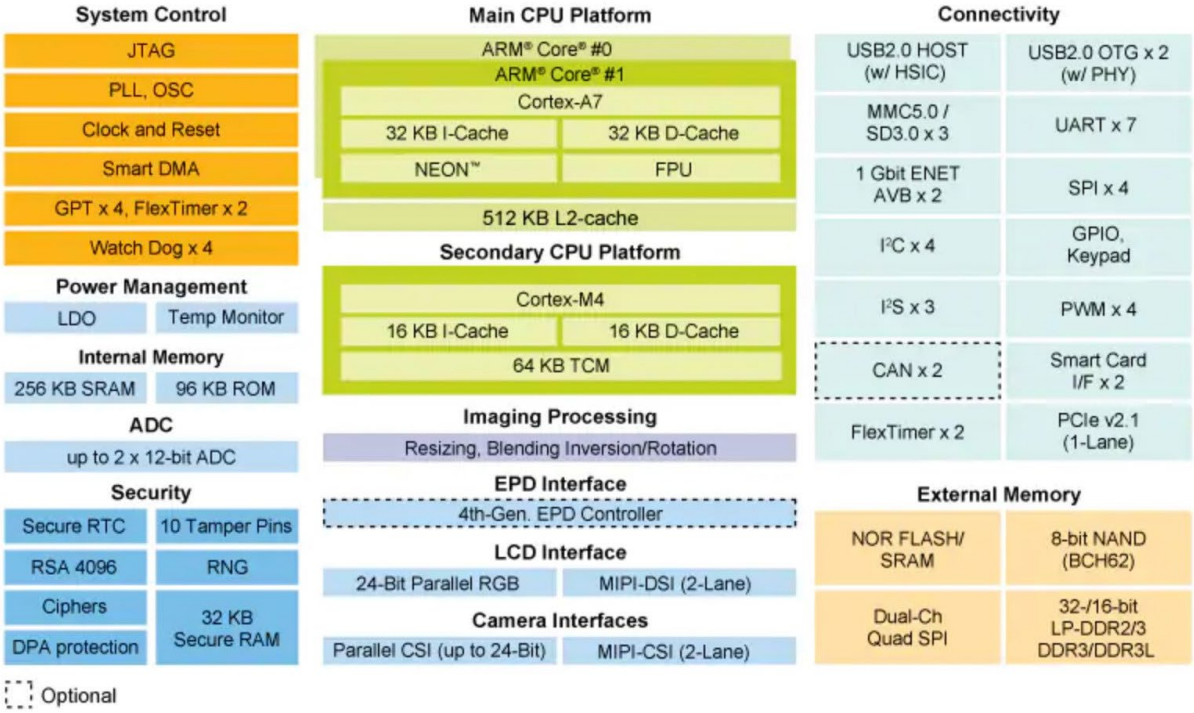


Figure 1: Block diagram i.MX7D
(Source: NXP)

The TQMa7x extends the TQC product range and offers an outstanding computing performance.
A suitable i.MX7 derivative (i.MX7Solo, i.MX7Dual) can be selected for each requirement.

All essential i.MX7 pins are routed to the TQMa7x connectors.
There are therefore no restrictions using the TQMa7x with respect to an integrated customised design.
All essential components like i.MX7, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMa7x.
The TQMa7x main features are:

- NXP i.MX7S (Solo) or i.MX7D (Dual), Cortex®-A7 + Cortex®-M4
- Up to 2 Gbyte DDR3L SDRAM with 32 bit interface
- Up to 32 Gbyte eMMC 5.0 NAND flash
- Up to 256 Mbyte Quad-SPI NOR flash (assembly option)
- 64 kbit EEPROM
- RTC (assembly option)
- Temperature sensor
- NXP Power Management Integrated Circuit
- All essential i.MX7 pins are routed to the TQMa7x connectors
- Extended temperature range
- Single supply voltage 5 V

The MBa7x also serves as an evaluation board for the TQMa7x.

2.2 Key functions and characteristics

The following interfaces are provided by default at the TQMa7x connectors. [1]

Table 2: Default interfaces

Interface	Qty.	Remark
ADC	2	4 channels each
CAN	2	FLEXCAN1 / FLEXCAN2
CCM	2	1 × Differential CLK 1 × Single-Ended CLK
ENET / RGMII	2	ENET1: 10/100/1000 Base-T (Ethernet) ENET2: 10/100/1000 Base-T (Ethernet): only on TQMa7D
GPIO	9	–
I²C	3	I2C1 is used for devices on the TQMa7x
JTAG	1	SJC / JTAG
LCD	1	24 bit RGB parallel
MIPI CSI	1	2 lanes
MIPI DSI	1	2 lanes
PCIe	1	PCIe 2.0: 1 lane; only on TQMa7D
PWM	4	–
QSPI	1	SPI NOR flash (assembly option)
SAI	1	I²S / ESAI
SDHC	1	uSDHC1: 4 bit, SD card UHS-I (SDR104)
SIM	1	ISO-7816 smart card interface
SPI	2	–
TAMPER	10	–
UART	5	9600 to 115200 Baud; 8N1; 4 UARTs with RTS# / CTS#
USB HSIC	1	Host
USB OTG	2	OTG2: Only on TQMa7D
WDOG	1	WDOG output and Reset

With an adapted pin configuration, other i.MX7 interfaces can be used alternatively to the standard configuration.
In essence, these are:

- Parallel CSI interface
- EIM interface
- EPDC interface
- Flexible Timer Module
- General-Purpose Memory Interface
- General-Purpose Timer
- Keypad port
- Medium-Quality Sound module
- More GPIOs
- Additional SIM interface
- More Audio, I²C, SPI and UART interfaces
- More Watchdog Timer

1: Number of interfaces and configuration depend on i.MX7 and TQMa7x derivative.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa7x, and the BSP provided by TQ-Systems, see also chapter 5.

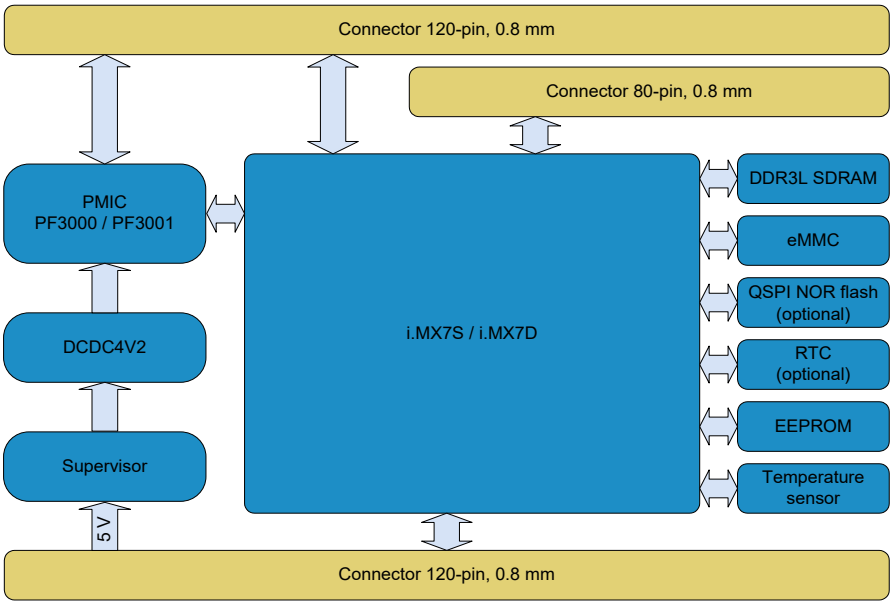


Figure 2: Block diagram TQMa7x (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The pin assignment listed in Table 3, Table 4, Table 5, and Table 8 refer to the BSP provided by TQ-Systems in combination with the Starterkit MBa7x. The multiple pin configurations by different i.MX7-internal function units must be taken note of, when the function of i.MX7 signals is altered.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX7 Data Sheets (1), (2), the i.MX7 Reference Manuals (5), (6), and the PMIC Data Sheet (4).

Attention: TQMa7x, malfunction or destruction	
	Depending on the configuration, many i.MX7 pins can provide several different functions. Please take note of the information in the i.MX7 Reference Manuals (5), (6), concerning the configuration of these pins before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa7x.

Note: TQMa7S / TQMa7D, pinout	
	The pinout in chapter 3.1.2 refers to the TQMa7S, the pinout in chapter 3.1.3 refers to the TQMa7D. The signals at connectors X1 and X2 are identical, some signals at X3 though, have different functions at the TQMa7S and the TQMa7D. The descriptions given in the following tables should be taken note of: – RFU: Reserved for future use. Pin has no function. Do not connect. – NC: These pins must never be connected and have to be left open. Please contact TQ-Support for details.

3.1.2 Pinout

Table 3: Pinout connector X1

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	Pin	5 V	Power	VCC5V	1	2	VCC5V	Power	5 V	Pin	–
–	Pin	5 V	Power	VCC5V	3	4	VCC5V	Power	5 V	Pin	–
–	Pin	5 V	Power	VCC5V	5	6	VCC5V	Power	5 V	Pin	–
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	9	10	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	11	12	DGND	Power	0 V	P	–
–	Pout	3.3 V	Power	VCC3V3_V33	13	14	VCC_SD	Power	1.8 V / 3.3 V	Pout	–
–	Pout	3.3 V	Power	VCC3V3_VLDO3	15	16	VSNVS	Power	3.0 V	Pout	–
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	I	3.0 V	Config	LICELL	19	20	RESET_OUT#	Config	3.3 V	O	–
–	I	3.3 V	Config	PMIC_PWRON	21	22	RESET_IN#	Config	3.3 V	I	–
–	P	0 V	Power	DGND	23	24	IMX_ONOFF	Config	3.3 V	I	AC8
K1	I/O	3.3 V	I2C	I2C1_SDA	25	26	VCC3V3_MB_EN	Power	1.5 V	Pout	–
J2	O	3.3 V	I2C	I2C1_SCL	27	28	RFU	–	–	–	–
–	P	0 V	Power	DGND	29	30	DGND	Power	0 V	P	–
K3	I/O	3.3 V	I2C	I2C2_SDA	31	32	ECSPI1_MOSI	SPI	3.3 V	O	G5
K2	O	3.3 V	I2C	I2C2_SCL	33	34	ECSPI1_MISO	SPI	3.3 V	I	H4
–	P	0 V	Power	DGND	35	36	ECSPI1_SS0#	SPI	3.3 V	O	H5
K6	I/O	3.3 V	I2C	I2C3_SDA	37	38	ECSPI1_SS1#	SPI	3.3 V	O	L3
K5	O	3.3 V	I2C	I2C3_SCL	39	40	ECSPI1_SS2#	SPI	3.3 V	O	L4
–	P	0 V	Power	DGND	41	42	ECSPI1_SS3#	SPI	3.3 V	O	L5
N2	O	3.3 V	PWM	PWM1_OUT	43	44	DGND	Power	0 V	P	–
N3	O	3.3 V	PWM	PWM2_OUT	45	46	ECSPI1_SCLK	SPI	3.3 V	O	H3
–	P	0 V	Power	DGND	47	48	DGND	Power	0 V	P	–
N5	O	3.3 V	PWM	PWM3_OUT	49	50	CCM_CLK1_P	CCM	1.8 V	I/O	Y2
N1	O	3.3 V	WDOG	WDOG1#	51	52	CCM_CLK1_N	CCM	1.8 V	I/O	Y1
–	P	0 V	Power	DGND	53	54	DGND	Power	0 V	P	–
W3	I	1.8 V	CCM	CCM_CLK2	55	56	UART3_CTS#	UART	3.3 V	O	M6
–	P	0 V	Power	DGND	57	58	UART3_RTS#	UART	3.3 V	I	M5
L1	I	3.3 V	UART	UART5_RX	59	60	UART3_RX	UART	3.3 V	I	M1
L2	O	3.3 V	UART	UART5_TX	61	62	UART3_TX	UART	3.3 V	O	M2
–	P	0 V	Power	DGND	63	64	DGND	Power	0 V	P	–
–	Pout	1.8 V	Power	VDDA1P8_SW2	65	66	VCC1V8_IN	Power	1.8 V	Pin	–
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AC1	A	1.8 V	ADC	ADC2_IN0	69	70	ADC1_IN0	ADC	1.8 V	A	AD1
AC2	A	1.8 V	ADC	ADC2_IN1	71	72	ADC1_IN1	ADC	1.8 V	A	AD3
AB1	A	1.8 V	ADC	ADC2_IN2	73	74	ADC1_IN2	ADC	1.8 V	A	AE2
AB2	A	1.8 V	ADC	ADC2_IN3	75	76	ADC1_IN3	ADC	1.8 V	A	AE3
–	P	0 V	Power	DGND	77	78	DGND	Power	0 V	P	–
P4	I	3.3 V	BOOT	BOOT_MODE0	79	80	GPIO1_IO09	GPIO	3.3 V	I/O	R2
P5	I	3.3 V	BOOT	BOOT_MODE1	81	82	GPIO2_IO28	GPIO	3.3 V	I/O	K24
–	P	0 V	Power	DGND	83	84	GPIO2_IO29	GPIO	3.3 V	I/O	K23
U2	I	3.3 V	JTAG	JTAG_TRST#	85	86	GPIO2_IO30	GPIO	3.3 V	I/O	H24
U4	I	3.3 V	JTAG	JTAG_TMS	87	88	GPIO2_IO31	GPIO	3.3 V	I/O	K20
U3	I	3.3 V	JTAG	JTAG_TDI	89	90	GPIO4_IO03	GPIO	3.3 V	I/O	L6
U6	O	3.3 V	JTAG	JTAG_TDO	91	92	GPIO5_IO12	GPIO	3.3 V	I/O	E3
U1	I	3.3 V	JTAG	JTAG_MOD	93	94	GPIO7_IO12	GPIO	3.3 V	I/O	D16
U5	I	3.3 V	JTAG	JTAG_TCK	95	96	GPIO7_IO15	GPIO	3.3 V	I/O	D19
–	P	0 V	Power	DGND	97	98	DGND	Power	0 V	P	–
AA3	I	1.8 V	TAMPER	TAMPER8	99	100	TAMPER9	TAMPER	1.8 V	I	Y3
AA4	I	1.8 V	TAMPER	TAMPER6	101	102	TAMPER7	TAMPER	1.8 V	I	Y4
AA5	I	1.8 V	TAMPER	TAMPER4	103	104	TAMPER5	TAMPER	1.8 V	I	Y5
AB6	I	1.8 V	TAMPER	TAMPER2	105	106	TAMPER3	TAMPER	1.8 V	I	Y7
AA7	I	1.8 V	TAMPER	TAMPER0	107	108	TAMPER1	TAMPER	1.8 V	I	Y8
–	P	0 V	Power	DGND	109	110	DGND	Power	0 V	P	–
M23	I	3.3 V	UART	UART6_RX	111	112	UART7_RX	UART	3.3 V	I	L22
L25	O	3.3 V	UART	UART6_TX	113	114	UART7_TX	UART	3.3 V	O	L21
L23	O	3.3 V	UART	UART6_CTS#	115	116	UART7_CTS#	UART	3.3 V	O	K25
L24	I	3.3 V	UART	UART6_RTS#	117	118	UART7_RTS#	UART	3.3 V	I	L20
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

3.1.2 Pinout (continued)

Table 4: Pinout connector X2

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
B4	O	1.8 V / 3.3 V	USDHC	SD1_RESET#	3	4	PMIC_SD_VSEL	Config	3.3 V	O	R1
A5	I/O	1.8 V / 3.3 V	USDHC	SD1_DATA0	5	6	SD1_CMD	USDHC	1.8 V / 3.3 V	I/O	C5
A4	I/O	1.8 V / 3.3 V	USDHC	SD1_DATA2	7	8	SD1_DATA1	USDHC	1.8 V / 3.3 V	I/O	D6
B5	O	1.8 V / 3.3 V	USDHC	SD1_CLK	9	10	SD1_DATA3	USDHC	1.8 V / 3.3 V	I/O	D5
–	P	0 V	Power	DGND	11	12	SD1_WP	USDHC	1.8 V / 3.3 V	I	C4
J5	O	3.3 V	SPI	ECSPI2_SCLK	13	14	SD1_CD#	USDHC	1.8 V / 3.3 V	I	C6
H6	I	3.3 V	SPI	ECSPI2_MISO	15	16	DGND	Power	0 V	P	–
N6	I	3.3 V	USB_OTG	USB_OTG1_OC	17	18	ECSPI2_MOSI	SPI	3.3 V	O	G6
P1	I	3.3 V	USB_OTG	USB_OTG1_PWR	19	20	ECSPI2_SS0#	SPI	3.3 V	O	J6
C8	Pin	5 V	Power	USB_OTG1_VBUS	21	22	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	23	24	USB_OTG1_CHD#	USB_OTG	3.3 V	O	C7
A8	I/O	3.3 V	USB_OTG	USB_OTG1_DN	25	26	USB_OTG1_ID	USB_OTG	3.3 V	I	B7
B8	I/O	3.3 V	USB_OTG	USB_OTG1_DP	27	28	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	29	30	SAI1_TX_DATA	SAI	3.3 V	O	E11
B12	I/O	3.3 V	HSIC	USB_HOST_STROBE	31	32	SAI1_TX_BCLK	SAI	3.3 V	O	C11
–	P	0 V	Power	DGND	33	34	SAI1_TX_SYNC	SAI	3.3 V	O	D11
A12	I/O	3.3 V	HSIC	USB_HOST_DATA	35	36	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	37	38	SAI1_RX_DATA	SAI	3.3 V	I	E12
E10	O	3.3 V	SAI	SAI1_MCLK	39	40	SAI1_RX_BCLK	SAI	3.3 V	I	D12
–	P	0 V	Power	DGND	41	42	SAI1_RX_SYNC	SAI	3.3 V	I	C12
D15	O	3.3 V	WDOG	WDOG2#	43	44	DGND	Power	0 V	P	–
E19	I	3.3 V	WDOG	WDOG2_RESET#	45	46	ENET1_MDC	ENET	3.3 V	O	T1
–	P	0 V	Power	DGND	47	48	ENET1_MDIO	ENET	3.3 V	I/O	R5
F16	O	3.3 V	RGMII	RGMII1_TXC	49	50	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	51	52	RGMII1_RXC	RGMII	3.3 V	I	F15
F17	O	3.3 V	RGMII	RGMII1_TD0	53	54	DGND	Power	0 V	P	–
E17	O	3.3 V	RGMII	RGMII1_TD1	55	56	RGMII1_RD0	RGMII	3.3 V	I	E14
E18	O	3.3 V	RGMII	RGMII1_TD2	57	58	RGMII1_RD1	RGMII	3.3 V	I	F14
D18	O	3.3 V	RGMII	RGMII1_TD3	59	60	RGMII1_RD2	RGMII	3.3 V	I	D13
E16	O	3.3 V	RGMII	RGMII1_TX_CTL	61	62	RGMII1_RD3	RGMII	3.3 V	I	E13
–	P	0 V	Power	DGND	63	64	RGMII1_RX_CTL	RGMII	3.3 V	I	E15
F6	I/O	3.3 V	SIM	SIM_TRXD	65	66	DGND	Power	0 V	P	–
E5	O	3.3 V	SIM	SIM_RST#	67	68	LCD_ENABLE	LCD	3.3 V	O	F25
F5	O	3.3 V	SIM	SIM_SVEN	69	70	DGND	Power	0 V	P	–
E6	O	3.3 V	SIM	SIM_PD	71	72	LCD_CLK	LCD	3.3 V	O	E20
E4	O	3.3 V	SIM	SIM_CLK	73	74	DGND	Power	0 V	P	–
C21	O	3.3 V	LCD	LCD_RESET#	75	76	LCD_HSYNC	LCD	3.3 V	O	E25
–	P	0 V	Power	DGND	77	78	LCD_VSYNC	LCD	3.3 V	O	F24
D21	O	3.3 V	LCD	LCD_DATA00	79	80	DGND	Power	0 V	P	–
B22	O	3.3 V	LCD	LCD_DATA02	81	82	LCD_DATA01	LCD	3.3 V	O	A22
C22	O	3.3 V	LCD	LCD_DATA04	83	84	LCD_DATA03	LCD	3.3 V	O	A23
A24	O	3.3 V	LCD	LCD_DATA06	85	86	LCD_DATA05	LCD	3.3 V	O	B23
–	P	0 V	Power	DGND	87	88	LCD_DATA07	LCD	3.3 V	O	F20
E21	O	3.3 V	LCD	LCD_DATA08	89	90	DGND	Power	0 V	P	–
B24	O	3.3 V	LCD	LCD_DATA10	91	92	LCD_DATA09	LCD	3.3 V	O	C23
F21	O	3.3 V	LCD	LCD_DATA12	93	94	LCD_DATA11	LCD	3.3 V	O	G20
D23	O	3.3 V	LCD	LCD_DATA14	95	96	LCD_DATA13	LCD	3.3 V	O	E22
–	P	0 V	Power	DGND	97	98	LCD_DATA15	LCD	3.3 V	O	C24
B25	O	3.3 V	LCD	LCD_DATA16	99	100	DGND	Power	0 V	P	–
E23	O	3.3 V	LCD	LCD_DATA18	101	102	LCD_DATA17	LCD	3.3 V	O	G21
C25	O	3.3 V	LCD	LCD_DATA20	103	104	LCD_DATA19	LCD	3.3 V	O	D24
D25	O	3.3 V	LCD	LCD_DATA22	105	106	LCD_DATA21	LCD	3.3 V	O	E24
–	P	0 V	Power	DGND	107	108	LCD_DATA23	LCD	3.3 V	O	G23
M20	O	3.3 V	QSPI	QSPI_SCLK	109	110	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	111	112	QSPI_DATA0	QSPI	3.3 V	I/O	P20
M21	O	3.3 V	QSPI	QSPI_SS0#	113	114	QSPI_DATA1	QSPI	3.3 V	I/O	P21
M22	O	3.3 V	QSPI	QSPI_SS1#	115	116	QSPI_DATA2	QSPI	3.3 V	I/O	N20
N22	O	3.3 V	QSPI	QSPI_RESET#	117	118	QSPI_DATA3	QSPI	3.3 V	I/O	N21
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

3.1.2 Pinout (continued)

Table 5: Pinout connector X3 (only TQMa7S)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
T5	I	3.3 V	CAN	CAN2_RX	3	4	CAN1_RX	CAN	3.3 V	I	T2
T6	O	3.3 V	CAN	CAN2_TX	5	6	CAN1_TX	CAN	3.3 V	O	T3
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
P3	I	3.3 V	GPIO	GPIO1_IO07	9	10	UART4_CTS#	UART	3.3 V	O	E9
P2	I	3.3 V	GPIO	GPIO1_IO06	11	12	UART4_RTS#	UART	3.3 V	I	E8
B11	–	–	NC	NC	13	14	UART4_RX	UART	3.3 V	I	D9
–	–	–	NC	NC	15	16	UART4_TX	UART	3.3 V	O	D8
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	–	–	–	RFU	19	20	NC	NC	–	–	A10
–	–	–	–	RFU	21	22	NC	NC	–	–	B10
–	–	–	–	RFU	23	24	DGND	Power	0 V	P	–
–	–	–	–	RFU	25	26	CSI_D1_N	MIPI	1.8 V	I	A14
–	P	0 V	Power	DGND	27	28	CSI_D1_P	MIPI	1.8 V	I	B14
A18	O	1.8 V	MIPI	DSI_D1_N	29	30	DGND	Power	0 V	P	–
B18	O	1.8 V	MIPI	DSI_D1_P	31	32	CSI_CLK_N	MIPI	1.8 V	I	A15
–	P	0 V	Power	DGND	33	34	CSI_CLK_P	MIPI	1.8 V	I	B15
A19	O	1.8 V	MIPI	DSI_CLK_N	35	36	DGND	Power	0 V	P	–
B19	O	1.8 V	MIPI	DSI_CLK_P	37	38	CSI_D0_N	MIPI	1.8 V	I	A16
–	P	0 V	Power	DGND	39	40	CSI_D0_P	MIPI	1.8 V	I	B16
A20	O	1.8 V	MIPI	DSI_D0_N	41	42	DGND	Power	0 V	P	–
B20	O	1.8 V	MIPI	DSI_D0_P	43	44	TEMP_EVENT#	Config	(2)	O	–
–	P	0 V	Power	DGND	45	46	RFU	–	–	–	–
D3	I	3.3 V	GPIO	GPIO5_IO09	47	48	RFU	–	–	–	–
C3	I	3.3 V	GPIO	GPIO5_IO10	49	50	RFU	–	–	–	–
–	P	0 V	Power	DGND	51	52	DGND	Power	0 V	P	–
H25	I	3.3 V	GPIO	GPIO2_IO27	53	54	GPIO2_IO21	GPIO	3.3 V	I	G24
–	P	0 V	Power	DGND	55	56	DGND	Power	0 V	P	–
H23	I	3.3 V	GPIO	GPIO2_IO22	57	58	GPIO2_IO16	GPIO	3.3 V	I	J21
H22	I	3.3 V	GPIO	GPIO2_IO23	59	60	GPIO2_IO17	GPIO	3.3 V	I	J20
J25	I	3.3 V	GPIO	GPIO2_IO24	61	62	GPIO2_IO18	GPIO	3.3 V	I	H21
J24	I	3.3 V	GPIO	GPIO2_IO25	63	64	GPIO2_IO19	GPIO	3.3 V	I	H20
K21	I	3.3 V	GPIO	GPIO2_IO26	65	66	GPIO2_IO20	GPIO	3.3 V	I	G25
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AE11	–	–	NC	NC	69	70	NC	NC	–	–	AC11
AD11	–	–	NC	NC	71	72	NC	NC	–	–	AB11
–	P	0 V	Power	DGND	73	74	DGND	Power	0 V	P	–
AE10	–	–	NC	NC	75	76	NC	NC	–	–	AC10
AD10	–	–	NC	NC	77	78	NC	NC	–	–	AB10
–	P	0 V	Power	DGND	79	80	DGND	Power	0 V	P	–

2 Active low open-drain output. Maximum pull-up-voltage 3.6 V

3.1.2 Pinout (continued)

Table 6: Pinout connector X3 (only TQMa7D)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
T5	I	3.3 V	CAN	CAN2_RX	3	4	CAN1_RX	CAN	3.3 V	I	T2
T6	O	3.3 V	CAN	CAN2_TX	5	6	CAN1_TX	CAN	3.3 V	O	T3
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
P3	I	3.3 V	USB_OTG	USB_OTG2_PWR	9	10	UART4_CTS#	UART	3.3 V	O	E9
P2	I	3.3 V	USB_OTG	USB_OTG2_OC	11	12	UART4_RTS#	UART	3.3 V	I	E8
B11	I	3.3 V	USB_OTG	USB_OTG2_ID	13	14	UART4_RX	UART	3.3 V	I	D9
C10	Pin	3.3 V	Power	USB_OTG2_VBUS	15	16	UART4_TX	UART	3.3 V	O	D8
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	–	–	–	RFU	19	20	USB_OTG2_DN	USB_OTG	3.3 V	I/O	A10
–	–	–	–	RFU	21	22	USB_OTG2_DP	USB_OTG	3.3 V	I/O	B10
–	–	–	–	RFU	23	24	DGND	Power	0 V	P	–
–	–	–	–	RFU	25	26	CSI_D1_N	MIPI	1.8 V	I	A14
–	P	0 V	Power	DGND	27	28	CSI_D1_P	MIPI	1.8 V	I	B14
A18	O	1.8 V	MIPI	DSI_D1_N	29	30	DGND	Power	0 V	P	–
B18	O	1.8 V	MIPI	DSI_D1_P	31	32	CSI_CLK_N	MIPI	1.8 V	I	A15
–	P	0 V	Power	DGND	33	34	CSI_CLK_P	MIPI	1.8 V	I	B15
A19	O	1.8 V	MIPI	DSI_CLK_N	35	36	DGND	Power	0 V	P	–
B19	O	1.8 V	MIPI	DSI_CLK_P	37	38	CSI_D0_N	MIPI	1.8 V	I	A16
–	P	0 V	Power	DGND	39	40	CSI_D0_P	MIPI	1.8 V	I	B16
A20	O	1.8 V	MIPI	DSI_D0_N	41	42	DGND	Power	0 V	P	–
B20	O	1.8 V	MIPI	DSI_D0_P	43	44	TEMP_EVENT#	Config	(2)	O	–
–	P	0 V	Power	DGND	45	46	RFU	–	–	–	–
D3	I/O	3.3 V	ENET	ENET2_MDIO	47	48	RFU	–	–	–	–
C3	O	3.3 V	ENET	ENET2_MDC	49	50	RFU	–	–	–	–
–	P	0 V	Power	DGND	51	52	DGND	Power	0 V	P	–
H25	O	3.3 V	RGMII	RGMII2_TXC	53	54	RGMII2_RXC	RGMII	3.3 V	I	G24
–	P	0 V	Power	DGND	55	56	DGND	Power	0 V	P	–
H23	O	3.3 V	RGMII	RGMII2_TD0	57	58	RGMII2_RD0	RGMII	3.3 V	I	J21
H22	O	3.3 V	RGMII	RGMII2_TD1	59	60	RGMII2_RD1	RGMII	3.3 V	I	J20
J25	O	3.3 V	RGMII	RGMII2_TD2	61	62	RGMII2_RD2	RGMII	3.3 V	I	H21
J24	O	3.3 V	RGMII	RGMII2_TD3	63	64	RGMII2_RD3	RGMII	3.3 V	I	H20
K21	O	3.3 V	RGMII	RGMII2_TX_CTL	65	66	RGMII2_RX_CTL	RGMII	3.3 V	I	G25
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AE11	I	1.8 V	PCIE	PCIE_RX_N	69	70	PCIE_TX_N	PCIE	1.8 V	O	AC11
AD11	I	1.8 V	PCIE	PCIE_RX_P	71	72	PCIE_TX_P	PCIE	1.8 V	O	AB11
–	P	0 V	Power	DGND	73	74	DGND	Power	0 V	P	–
AE10	I	1.8 V	PCIE	PCIE_REFCLK_IN_N	75	76	PCIE_REFCLK_OUT_N	PCIE	1.8 V	O	AC10
AD10	I	1.8 V	PCIE	PCIE_REFCLK_IN_P	77	78	PCIE_REFCLK_OUT_P	PCIE	1.8 V	O	AB10
–	P	0 V	Power	DGND	79	80	DGND	Power	0 V	P	–

3.2 System components

3.2.1 i.MX7

3.2.1.1 i.MX7 derivatives

Depending on the TQMa7x version, one of the following i.MX7 derivatives is assembled.

Table 7: i.MX7 derivatives

CPU	Manufacturer number	Mask revision	CPU clock	Temperature range
i.MX7 Solo Industrial	MCIMX7S5EVM08SC	1.2	800 MHz	–20 °C to +105 °C
i.MX7 Dual Industrial	MCIMX7D5EVM10SC	1.2	1000 MHz	–20 °C to +105 °C

3.2.1.2 eFuses

The eFuses in the i.MX7 are available for the user, except for the MAC address eFuses.

TQMa7x modules are delivered pre-programmed with MAC addresses from the TQ-Systems MAC address pool. The MAC address LOCK-FUSE WP (Write Protect) is burnt, which permits to temporarily overwrite the MAC address for test purposes. If this is not desired, the MAC address LOCK-FUSE OP (Overwrite Protect) can be burned by the user.

3.2.1.3 i.MX7 errata

Attention: Malfunction or destruction	
	Please take note of the current i.MX7 errata (7).

3.2.1.4 Boot modes

The i.MX7 contains a ROM with integrated boot loader.

After power-up, the boot code initializes the hardware and then loads the program image from the selected boot device. As standard boot device of the TQMa7x e.g. the integrated e-MMC or the optional SPI-NOR-Flash can be chosen.

As an alternative to booting from the integrated eMMC or the QSPI NOR flash, additional boot interfaces are available, see 3.2.1.6.

More information about boot interfaces and its configuration is to be taken from the i.MX7 Data Sheets (1), (2), and the i.MX7 Reference Manuals (5), (6).

The boot device and its configuration, as well as different i.MX7 settings have to be set via different boot mode registers.

Therefore, the i.MX7 provides two possibilities:

- Burning and reading internal eFuses
- Reading dedicated GPIO pins

The exact behaviour during booting depends on the value of register BT_FUSE_SEL (default = 0).

The following table shows the behaviour of the BT_FUSE_SEL bit in dependence of the selected boot mode.

Table 8: Boot modes and BT_FUSE_SEL

BOOT_MODE[1:0]	Boot type	BT_FUSE_SEL	Usage
00 (default)	Boot from eFuses	BT_FUSE_SEL = 0: Boot using Serial Loader (default) BT_FUSE_SEL = 1: Boot mode configuration is taken from eFuses	Series production
01	Serial Downloader	Boot using Serial-Loader (USB OTG1)	Development / production
10	Internal Boot	BT_FUSE_SEL = 0: Boot configuration is taken from BOOT_CFG pins (default) BT_FUSE_SEL = 1: Boot configuration is taken from eFuses	Development
11	Reserved	n.a.	n.a.

Note: Field software update concept	
	It is recommended to provide a redundant update concept for field software updates, when designing a carrier board.

3.2.1.5 Boot configuration

Some general settings are done with eFuses, independent from the boot device.

Table 9: General boot settings

i.MX7		TQMa7x		
eFuse	Option	Setting [3]	Signal	Pin
BOOT_CFG19	**Infinite-Loop (for debug purposes):** 0 – Disabled 1 – Enabled	0	LCD_DATA19	X2-104
BOOT_CFG18	**i.MX7 / DDR Clock:** 0 - i.MX7: 792 MHz; DDR: 533 MHz 1 - i.MX7: 396 MHz; DDR: 266 MHz	0	LCD_DATA18	X2-101
BOOT_CFG17	**Recovery Boot Enable:** 0 – Disabled 1 – Enabled	0	LCD_DATA17	X2-102
BOOT_CFG16	**BT_MMU_DISABLE (MMU / L1 D Cache):** 0 – Enabled 1 – Disabled	0	LCD_DATA16	X2-99

Note: Boot configuration	
	The eMMC on the TQMa7x is configured as default boot device at delivery.

3: Voltage level or condition of eFuse.

3.2.1.6 Boot interfaces

In the next chapters, the configuration of the following boot devices is described:

- eMMC
- QSPI NOR flash
- SD card

3.2.1.7 Boot device eMMC

Table 10: Boot configuration eMMC at uSDHC3

i.MX7		TQMa7x		
eFuse	Option	Setting [4]	Signal	Pin
BOOT_CFG15	**Boot Device:** 0010 – MMC / eMMC	0	LCD_DATA15	X2-98
BOOT_CFG14		0	LCD_DATA14	X2-95
BOOT_CFG13		1	LCD_DATA13	X2-96
BOOT_CFG12		0	LCD_DATA12	X2-93
BOOT_CFG11	**Port Selection:** 00 – uSDHC1 01 – uSDHC2 10 – uSDHC3	1	LCD_DATA11	X2-94
BOOT_CFG10		0	LCD_DATA10	X2-91
BOOT_CFG9	**eMMC Reset:** 0 – Disabled 1 – Enabled	0	LCD_DATA09	X2-92
BOOT_CFG7	**Boot Speed:** 0 – Normal / Regular Boot 1 – Fast Boot	0	LCD_DATA07	X2-88
BOOT_CFG6	**Bus width:** 000 – 1 bit 001 – 4 bit 010 – 8 bit 101 – 4 bit DDR (MMC 4.4) 110 – 8 bit DDR (MMC 4.4)	0	LCD_DATA06	X2-85
BOOT_CFG5		1	LCD_DATA05	X2-86
BOOT_CFG4		0	LCD_DATA04	X2-83
BOOT_CFG3	**Speed Selection:** 00 – Normal Speed 01 – High Speed 10 – Reserved for HS200	0	LCD_DATA03	X2-84
BOOT_CFG2		0	LCD_DATA02	X2-81

4: Voltage level or condition of eFuse.

3.2.1.8 Boot device QSPI NOR flash

Table 11: Boot configuration QSPI NOR flash at QSPI

i.MX7		TQMa7x		
eFuse	Option	Setting [5]	Signal	Pin
BOOT_CFG15	**Boot Device:** 0100 – QSPI	0	LCD_DATA15	X2-98
BOOT_CFG14		1	LCD_DATA14	X2-95
BOOT_CFG13		0	LCD_DATA13	X2-96
BOOT_CFG12		0	LCD_DATA12	X2-93
BOOT_CFG11	**QSPI Instance:** 0 – QSPI0 1 – Reserved	0	LCD_DATA11	X2-94
BOOT_CFG10	**SDR SMP:** 000 – Default 001…111 – Reserved	0	LCD_DATA10	X2-91
BOOT_CFG9		0	LCD_DATA09	X2-92
BOOT_CFG8		0	LCD_DATA08	X2-89
BOOT_CFG7	**Half Speed Phase Selection:** 0 – At non-inverted clock 1 – At inverted clock	0	LCD_DATA07	X2-88
BOOT_CFG6	**Half Speed Delay:** 0 – One clock delay 1 – Two clock delay	0	LCD_DATA06	X2-85
BOOT_CFG5	**Full Speed Phase Selection:** 0 – At non-inverted clock 1 – At inverted clock	0	LCD_DATA05	X2-86
BOOT_CFG4	**Full Speed Delay:** 0 – One clock delay 1 – Two clock delay	0	LCD_DATA04	X2-83

5: Voltage level or condition of eFuse.

3.2.1.9 Boot device SD card

Table 12: Boot configuration SD card at uSDHC1

i.MX7		TQMa7x		
eFuse	Option	Setting [6]	Signal	Pin
BOOT_CFG15	**Boot Device:** 0001 – SD / eSD	0	LCD_DATA15	X2-98
BOOT_CFG14		0	LCD_DATA14	X2-95
BOOT_CFG13		0	LCD_DATA13	X2-96
BOOT_CFG12		1	LCD_DATA12	X2-93
BOOT_CFG11	**Interface-Selection:** 00 – uSDHC1 01 – uSDHC2 10 – uSDHC3	0	LCD_DATA11	X2-94
BOOT_CFG10		0	LCD_DATA10	X2-91
BOOT_CFG9	**SD Power Cycle:** 0 – Disabled 1 – Enabled	0	LCD_DATA09	X2-92
BOOT_CFG8	**SD Loopback Clock Source:** 0 – Through SD pad 1 – Direct	0	LCD_DATA08	X2-89
BOOT_CFG7	**Boot Speed:** 0 – Normal / Regular Boot 1 – Fast Boot	0	LCD_DATA07	X2-88
BOOT_CFG4	**Bus-Width:** 0 – 1 bit 1 – 4 bit	1	LCD_DATA04	X2-83
BOOT_CFG3	**Speed-Selection:** 000 – Normal / SDR12 001 – High / SDR25 010 – Not applicable for uSDHC1 (7) 011 – Not applicable for uSDHC1 (7) 101 – Reserved for DDR50	0	LCD_DATA03	X2-84
BOOT_CFG2		0	LCD_DATA02	X2-81
BOOT_CFG1		1	LCD_DATA01	X2-82

6: Voltage level or condition of eFuse.
7: More details can be found in the i.MX7 Reference-Manual (5), chapter 6.6.5.3.3.

3.2.2 Memory

The TQMa7x provides the following memories:

- DDR3L (32 bit)
- QSPI NOR flash
- eMMC
- EEPROM

3.2.2.1 DDR3L SDRAM

Two DDR3L Samsung K4B2G1646F-BMK0 SDRAM chips type DDR3L-1600 128M16 are assembled on the TQMa7x.
The chips have one common chip select and are connected to the i.MX7 with a bus width of 32 bit.
The following block diagram shows how the DDR3L SDRAM is connected to the i.MX7.

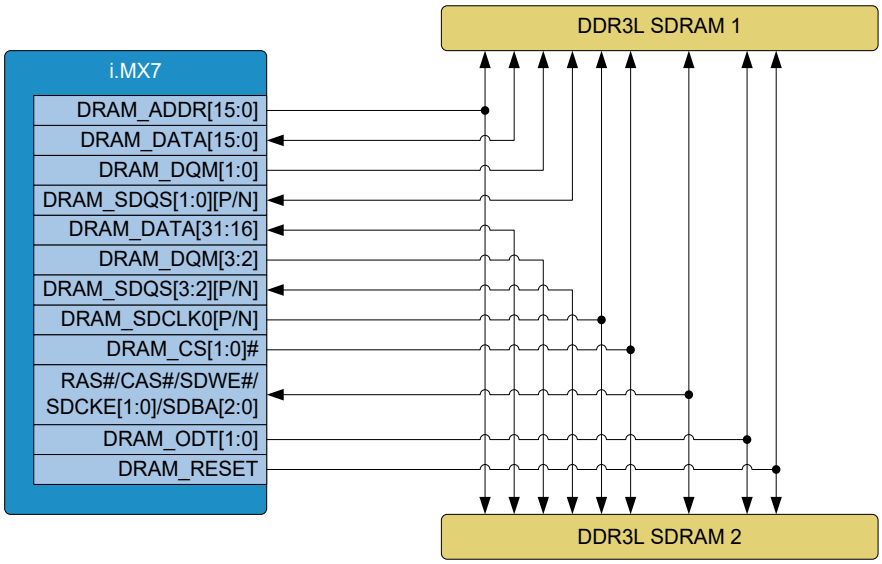


Figure 3: Block diagram DDR3L SDRAM interface

3.2.2.2 eMMC NAND flash

An 8 Gbyte SanDisk SDINBDG4-8G-T eMMC or an 8 Gbyte Micron MTFC8GAKAJCN-1M eMMC is assembled on the TQMa7x.
The eMMC contains the boot loader and can contain operating system and application software. The Hardware Reset-Function depends on the BSP.
The following block diagram shows how the eMMC flash is connected to the i.MX7.

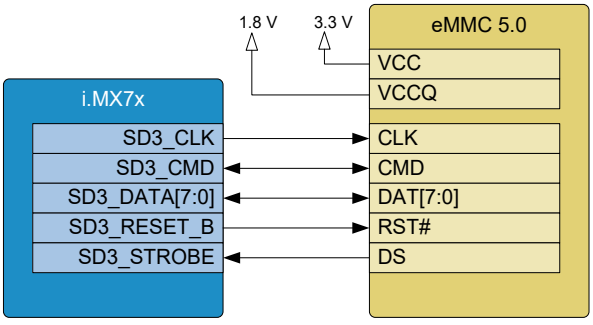


Figure 4: Block diagram eMMC interface

Attention: Malfunction or destruction	
	Some eMMC have a too high drive-strength. This can lead to poor signal integrity and a life time reduction of the CPU. When using an own bootloader or operating system it is essential to implement the SET_DSR routine, which is part of the BSP provided by TQ-Systems since revision 01xx. Since not all types of eMMC allow a driver strength adaptation, eMMC signals were attenuated by serial terminations from TQMa7x revision 02xx onwards. Therefore, from TQMa7x revision 02xx onwards, the SET_DSR routine may no longer be used. The additional signal damping might cause malfunctions.

The following eMMC modes are supported at the USDHC3 port of the i.MX7:

Table 13: USDHC3 eMMC modes

eMMC mode	1 bit	4 bit	8 bit	Fast boot	Remark
Normal Speed	Yes	Yes	Yes	No (8)	Not tested
High Speed	Yes	Yes	Yes	No (8)	–
HS200	n.a. (9)	Yes	Yes	No (8)	–
HS400	n.a. (9)	n.a. (9)	Yes	No (8)	Default in BSP provided by TQ-Systems

Attention: Malfunction or destruction	
	An implementation of the SET_DSR routine from the BSP Rev.0104 must no longer be carried out for modules from REV.0200 onwards, as this can lead to malfunctions due to additional signal attenuation.

3.2.2.3 QSPI NOR flash

A 64 Mbyte Micron QSPI NOR flash type MT25QL512ABB8E12-0SIT is available as assembly option. It can e.g., serve as boot device or as recovery device.

The following block diagram shows how the QSPI NOR flash is connected to the i.MX7.

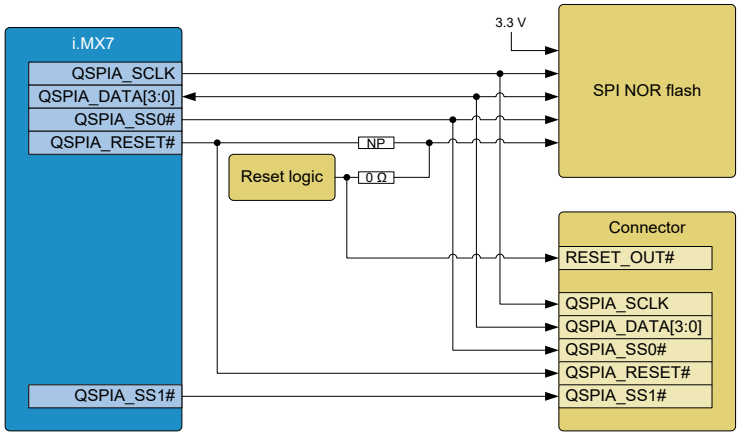


Figure 5: Block diagram QSPI NOR flash interface

8: Not supported by software.
9: Not specified by JEDEC.

The QSPI interface is routed to connector X2 to connect external QSPI memory. However, the interface should only be used on the mainboard if the optional QSPI-NOR flash on the TQMa7x is not equipped, as this can lead to a strong influence on the signal shapes depending on the transmission rate.
The following block diagram shows the QSPI interface:

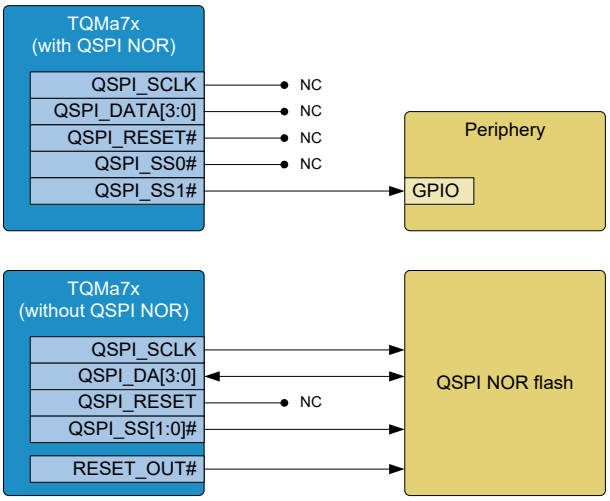


Figure 6: Block diagram external QSPI NOR flash interface

Attention: Malfunction or destruction	
	The QSPI interface may only be used as memory interface. Other SPI devices have to be connected at the eCSPI interfaces.

3.2.2.4 EEPROM M24C64

The TQMa7x provides a 64 Kbit serial EEPROM type STM M24C64-RDW6TP, which contains TQMa7x-specific data, see Table 16.
The user can also store own data in this EEPROM. It is connected to the I2C1 bus of the i.MX7. Write-Control (WC) is not supported.

The following block diagram shows how the EEPROM is connected to the i.MX7.

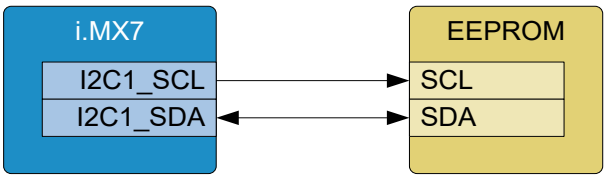


Figure 7: Block diagram EEPROM interface

- The I²C address of the EEPROM is `0x50 / 101 0000b`

In the EEPROM, TQMa7x-specific data is stored. It is, however, not essential for the correct operation of the TQMa7x.
The user can delete or alter the data.

In the following table, the parameters stored in the EEPROM are shown.

Table 14: TQMa7x-specific data in the EEPROM

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code
0x80	–	–	$8{,}064_{(10)}$	–	(Unused)

3.2.3 RTC

Depending on the version of TQMa7x, the i.MX7-internal RTC is used, or a discrete RTC DS1339U is assembled on the TQMa7x.

Note: i.MX7 RTC	
	In ON-mode the i.MX7-internal RTC can always be used, but resets itself on TQMa7x versions with assembled DS1339U when the TQMa7x supply (5 V) is switched off, since the i.MX7 SNVS domain is not supplied anymore in this case.

3.2.3.1 i.MX7 RTC

The i.MX7 provides an RTC, which has its own power domain (SNVS). The accuracy of this RTC is mainly determined by the characteristics of the quartz used. The type FC-135R assembled on the TQMa7x has a standard frequency tolerance of ±20 ppm @ +25 °C. (Parabolic coefficient: max. -0.04×10^{-6} / °C^2).

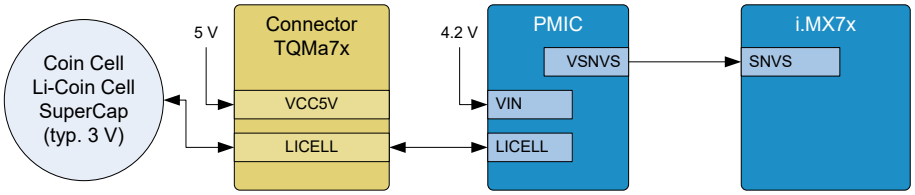


Figure 8: Block diagram i.MX7 RTC supply

The RTC power domain SNVS of the i.MX7 is supplied by the PMIC-internal regulator VSNVS. This regulator is supplied either by VIN (VCC4V2) or by LICELL. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (4). It is to be taken note of that the typical charging current is only 60 µA.

Note: i.MX7 RTC	
	On TQMa7x versions with assembled DS1339U the i.MX7 SNVS domain is not supplied by LICELL and hence the i.MX7-internal RTC can only be used in ON-mode.

Table 15: Current consumption i.MX7 RTC at LICELL

Voltage LICELL	Current consumption LICELL	Remark
3.2 V	7.1 µA typical; 10 µA maximal	VCC5V = 0 V T_{amb} = +25 °C
3.0 V	7.1 µA typical; 10 µA maximal	
2.1 V	6.1 µA typical; 10 µA maximal	

On account of the high power consumption of the i.MX7-internal RTC the optional RTC on the TQMa7x is recommended for long term bridging.

Note: Current consumption of i.MX7-internal RTC	
	A coin cell is not suitable for long term bridging on account of the high current consumption of the i.MX7-internal RTC. A Lithium coin cell or a SuperCap might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 µA. For long term bridging an external RTC connected at the I²C bus on the carrier board or the optional RTC DS1339U on the TQMa7x is recommended.

3.2.3.2 RTC DS1339U

In addition to the i.MX7-internal RTC, an optional I²C RTC type Maxim DS1339U-33+ is available.
The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The type CM7V used on the TQMa7x has a standard frequency tolerance of ±20 ppm @ +25 °C. (Parabolic coefficient: max. -0.04×10^{-6} / °C²).

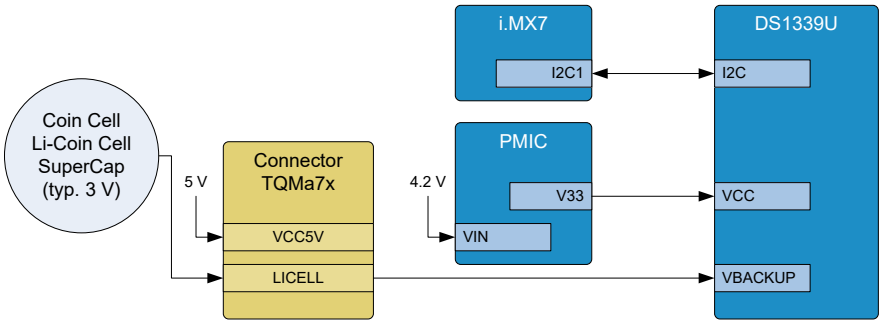


Figure 9: Block diagram DS1339U RTC on TQMa7x

- The I²C address of the RTC is `0x68 / 110 1000b`

The following table shows the current consumption of the DS1339U RTC assembled on the TQMa7x.

Table 16: Current consumption DS1339U on TQMa7x at LICELL

Voltage LICELL	Current consumption LICELL	Remark
3.2 V	0.44 µA typical; 0.7 µA maximal (10)	VCC5V = 0 V Tamb = +25 °C
3.0 V	0.44 µA typical; 0.7 µA maximal (10)	
2.1 V	0.4 µA typical; 0.7 µA maximal (10)	

Note: Assembled DS1339U	
	If the DS1339U is assembled, the SNVS voltage domain is not supplied by LICELL. The i.MX7 SNVS functions are therefore only available when the TQMa7x is supplied with 5 V. Coin cells cannot be charged at LICELL, when the DS1339U is assembled. The RTC DS1339U is directly supplied by LICELL. The PMIC supplies the RTC when the TQMa7x is powered with 5 V.

10: See Data Sheet DS1339U (9).

3.2.4 Temperature sensor

A temperature sensor SE97BTP with integrated EEPROM is assembled on TQMa7x revision 02xx. It is placed on the top side of the TQMa7x (D7, Figure 25).

The temperature sensor / EEPROM is connected to the i.MX7 I2C1 bus with the address `0x1E / 001 1110b`.

The "EVENT#"-output (over temperature) of the SE97BTP is routed as an open drain to X3-44 (TEMP_EVENT#). It requires a pull-up on the mainboard to a voltage of up to 3.6 V.

The following block diagram shows how the temperature sensor is connected to the i.MX7.

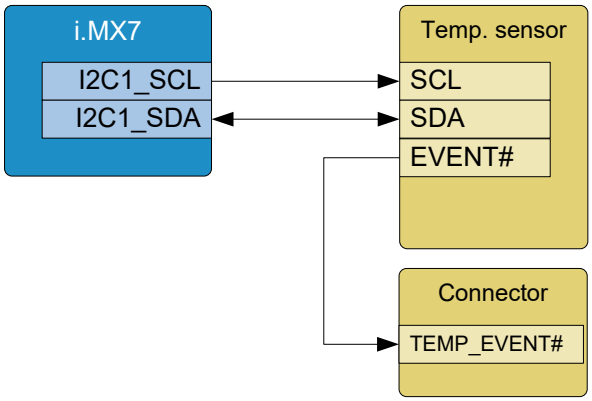


Figure 10: Block diagram temperature sensor interface SE97BTP

Half of the memory area of 256 bytes can be permanently protected against write accesses by register accesses. Thus module-internal data can be deposited here, which are to be stored permanently. The EEPROM can operate in two different modes, which are shown in the following table.

Table 17: EEPROM SE97BTP

Mode	I²C address	Range	Size	Remark
Protection Mode	`0x36 / 011 0110b`	`00h to 7Fh`	128 Byte	PWP or RWP
Normal Mode	`0x56 / 101 0110b`	`80h to FFh`	128 Byte	No protection

3.2.5 Interfaces

3.2.5.1 Overview

The following three interfaces are used exclusively on the TQMa7x and are not routed to the connectors.

Table 18: TQMa7x-internally used interfaces

Interface	Qty.	Chapter	Remark
uSDHC3	1	3.2.7.21	eMMC, 8 bit
DDR	1	3.2.2.1	DDR3L SDRAM, 32 bit
SD2_RESET#	1	3.2.8	PMIC_INT# (Ball G3)

In the following chapters, only the primarily interfaces are described.

Table 19: Primarily multiplexed interfaces

Interface	Qty.	Chapter	Remark
ADC	2	3.2.5.2	4 channels each
CAN	2	3.2.5.6	FLEXCAN1 / FLEXCAN2
CCM	2	3.2.5.3	1 × CLK differential (In/Out), 1 × CLK Single-Ended (In)
ECSPI	2	3.2.5.4	ECSPI1 / ECSPI2
ENET	1	3.2.5.5	RGMII (GbE)
ENET	1	3.2.5.5	RGMII (GbE), only TQMa7D
GPIO	9	3.2.5.7	–
I^2C	3	3.2.5.8	I2C1 / I2C2 / I2C3
LCD	1	3.2.5.9	24 bit RGB
MIPI_CSI	1	3.2.5.10	–
MIPI_DSI	1	3.2.5.11	–
PCIe	1	3.2.5.12	Only TQMa7D
PWM	4	3.2.5.13	–
QSPI	1	3.2.5.14	SPI NOR flash
SAI	1	3.2.5.15	–
SDHC	1	3.2.5.21	uSDHC1: 4 bit, SD card UHS-I (SDR104)
SIM	1	3.2.5.16	–
SJC	1	3.2.5.17	JTAG
TAMPER	10	3.2.5.18	–
UART	5	3.2.5.19	–
USB HSIC	1	3.2.5.20	–
USB OTG	1	3.2.5.20	With Host function
USB OTG	1	3.2.5.20	With Host function, only TQMa7D
WDOG	1	3.2.5.22	Including Reset

3.2.5.2 ADC

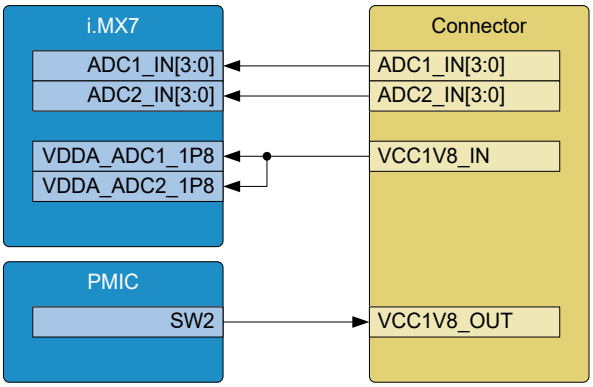


Figure 11: Block diagram ADC

Two ADC interfaces with four channels each and 12 bit resolution are available. Technical details are to be taken from the i.MX7 Reference Manuals (5), (6).

The reference voltage VCC1V8_OUT (VDDA1P8_SW2) is provided by the PMIC on the TQMa7x and routed to TQMa7x connector X1-65. For applications without high precision, VCC1V8_IN (X1-66) can be connected with VCC1V8_OUT on the carrier board.

For high precision, an external voltage reference can be connected to VCC1V8_IN. This is, however, application-specific, but has to meet at least the following parameters:

- Voltage at VCC1V8_IN: 1.71 V to 1.89 V (typically 1.8 V)
- Current rating VCC1V8_IN: max. 15 mA
- Adherence of i.MX7 Power-Sequencing

The ADC, as well as the i.MX7 temperature sensor has to be supplied via pin VCC1V8_IN, X1-66.

The following table shows the signals used by the ADC interface.

Table 20: ADC

Signal	Direction	Pin	Power domain
ADC1_IN0	I	X1-70	VCC1V8_IN
ADC1_IN1	I	X1-72	
ADC1_IN2	I	X1-74	
ADC1_IN3	I	X1-76	
ADC2_IN0	I	X1-69	
ADC2_IN1	I	X1-71	
ADC2_IN2	I	X1-73	
ADC2_IN3	I	X1-75	

3.2.5.3 CCM

The clock controller module of the i.MX7 provides two programmable clocks:

- CCM_CLK1_N/P is optionally a differential (LVDS) clock input or clock output.
- CCM_CLK2 is a Single-Ended clock input.

The following table shows the signals used by the CCM interface.

Table 21: CCM

Signal	Direction	Pin	Power domain
CCM_CLK1_P	I/O	X1-50	VDDA1P8_SW2
CCM_CLK1_N	I/O	X1-52	
CCM_CLK2	I	X1-55	

3.2.5.4 ECSPI

The i.MX7 provides four ECSPI interfaces. ECSPI1 and ECSPI2 are available as primary function at the TQMa7x connectors.
The following table shows the signals used by the ECSPI1 and the ECSPI2 interfaces.

Table 22: ECSPI1and ECSPI2

Signal	Direction	Pin	Remark	Power domain
ECSPI1_MISO	I	X1-34	–	VCC3V3_V33
ECSPI1_MOSI	O	X1-32	–	
ECSPI1_SCLK	O	X1-46	–	
ECSPI1_SS0#	O	X1-36	–	
ECSPI1_SS1#	O	X1-38	–	
ECSPI1_SS2#	O	X1-40	–	
ECSPI1_SS3#	O	X1-42	–	
ECSPI2_MISO	I	X2-15	Alternative: SD1_DATA6	
ECSPI2_MOSI	O	X2-18	Alternative: SD1_DATA5	
ECSPI2_SCLK	O	X2-13	Alternative: SD1_DATA4	
ECSPI2_SS0#	O	X2-20	Alternative: SD1_DATA7	

3.2.5.5 ENET

The i.MX7D provides two 10/100/1000 MAC cores, which support MII, RMII and RGMII. The i.MX7S only provides the ENET1 interface. The ENET2 interface pins of the i.MX7S can be used as GPIOs.
All signals are supplied by a 3.3 V power domain. The RGMII signals are available at the connectors as primary function.

The following table shows the signals used by the RGMII interfaces:

Table 23: ENET1 and ENET2

TQMa7D		TQMa7S		Pin
Signal	Direction	Signal	Direction	
ENET1_MDIO	I/O	ENET1_MDIO	I/O	X2-48
ENET1_MDC	O	ENET1_MDC	O	X2-46
RGMII1_RD0	I	RGMII1_RD0	I	X2-56
RGMII1_RD1	I	RGMII1_RD1	I	X2-58
RGMII1_RD2	I	RGMII1_RD2	I	X2-60
RGMII1_RD3	I	RGMII1_RD3	I	X2-62
RGMII1_RX_CTL	I	RGMII1_RX_CTL	I	X2-64
RGMII1_RXC	I	RGMII1_RXC	I	X2-52
RGMII1_TD0	O	RGMII1_TD0	O	X2-53
RGMII1_TD1	O	RGMII1_TD1	O	X2-55
RGMII1_TD2	O	RGMII1_TD2	O	X2-57
RGMII1_TD3	O	RGMII1_TD3	O	X2-59
RGMII1_TX_CTL	O	RGMII1_TX_CTL	O	X2-61
RGMII1_TXC	O	RGMII1_TXC	O	X2-49
ENET2_MDIO	I/O	GPIO5_IO09	I/O	X3-47
ENET2_MDC	O	GPIO5_IO10		X3-49
RGMII2_RD0	I	GPIO2_IO16		X3-58
RGMII2_RD1	I	GPIO2_IO17		X3-60
RGMII2_RD2	I	GPIO2_IO18		X3-62
RGMII2_RD3	I	GPIO2_IO19		X3-64
RGMII2_RX_CTL	I	GPIO2_IO20		X3-66
RGMII2_RXC	I	GPIO2_IO21		X3-54
RGMII2_TD0	O	GPIO2_IO22		X3-57
RGMII2_TD1	O	GPIO2_IO23		X3-59
RGMII2_TD2	O	GPIO2_IO24		X3-61
RGMII2_TD3	O	GPIO2_IO25		X3-63
RGMII2_TX_CTL	O	GPIO2_IO26		X3-65
RGMII2_TXC	O	GPIO2_IO27		X3-53

3.2.5.6 FLEXCAN

The i.MX7 provides two integrated CAN 2.0B controllers. Both signals pairs are available at the TQMa7x connectors.
The drivers required have to be implemented on the carrier board.

The following table shows the signals used by the CAN interfaces.

Table 24: FLEXCAN

Signal	Direction	Pin	Power domain
CAN1_RX	I	X3-4	VCC3V3_VLDO3
CAN1_TX	O	X3-6	
CAN2_RX	I	X3-3	
CAN2_TX	O	X3-5	

3.2.5.7 GPIO

Beside their interface function, most i.MX7 pins can also be configured as GPIO. All these GPIOs can trigger an interrupt.
Details are to be taken from the i.MX7 Reference Manuals (5), (6), and the i.MX7 Data Sheets (1), (2).
In addition, several pins are already marked as GPIO and are available on the TQMa7x connectors.

The following table shows the GPIO signals provided:

Table 25: GPIO

Signal	Pin	Power domain
GPIO1_IO09	X1-80	VCC3V3_VLDO3
GPIO2_IO28	X1-82	VCC3V3_VLDO4
GPIO2_IO29	X1-84	
GPIO2_IO30	X1-86	
GPIO2_IO31	X1-88	
GPIO4_IO03	X1-90	VCC3V3_V33
GPIO5_IO12	X1-92	
GPIO7_IO12	X1-94	VCC3V3_VLDO4
GPIO7_IO15	X1-96	

The electrical characteristics of the GPIOs are to be taken from the i.MX7 Data Sheets (1), (2).

3.2.5.8 I²C

The i.MX7 provides four I²C interfaces. I2C1, I2C2 and I2C3 are routed to the TQMa7x connectors as primary function. All signals are supplied by a 3.3 V power domain.

The following table shows the signals used by the I²C interfaces.

Table 26: I²C signals

Signal	Direction	Pin	Remark
I2C1_SCL	O	X1-27	2.2 kΩ PU to 3.3 V on TQMa7x
I2C1_SDA	I/O	X1-25	2.2 kΩ PU to 3.3 V on TQMa7x
I2C2_SCL	O	X1-33	–
I2C2_SDA	I/O	X1-31	–
I2C3_SCL	O	X1-39	–
I2C3_SDA	I/O	X1-37	–

The following table shows the I²C devices connected to the I2C1 bus on the TQMa7x.

Table 27: I²C address assignment

Component	Address	Remark
EEPROM M24C64	0x50 / 101 0000b	–
Temperature sensor SE97BTP	0x1E / 001 1110b	Temperature register
EEPROM SE97BTP	0x56 / 101 0110b	Normal Mode (RWP)
	0x36 / 011 0110b	Protected Mode (PWP)
RTC DS1339U	0x68 / 110 1000b	(Assembly option)
PMIC PF3000 / PF3001	0x08 / 000 1000b	Should not be altered

If more devices are connected to the I²C buses on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional Pull-Ups at the bus should be provided on the carrier board, if required.

3.2.5.9 LCD

The i.MX7 provides a parallel display interface. All signals are supplied by a 3.3 V power domain.
Information regarding supported displays and formats are to be taken from the i.MX7 Reference Manuals (5), (6).
The following table shows the signals used by the LCD interface.

Table 28: LCD interface

Signal	Direction	Pin	Remark
LCD_DATA23	O	X2-108	–
LCD_DATA22	O	X2-105	–
LCD_DATA21	O	X2-106	–
LCD_DATA20	O	X2-103	–
LCD_DATA19	O	X2-104	–
LCD_DATA18	O	X2-101	–
LCD_DATA17	O	X2-102	–
LCD_DATA16	O	X2-99	–
LCD_DATA15	O	X2-98	–
LCD_DATA14	O	X2-95	–
LCD_DATA13	O	X2-96	–
LCD_DATA12	O	X2-93	–
LCD_DATA11	O	X2-94	–
LCD_DATA10	O	X2-91	–
LCD_DATA09	O	X2-92	–
LCD_DATA08	O	X2-89	–
LCD_DATA07	O	X2-88	–
LCD_DATA06	O	X2-85	–
LCD_DATA05	O	X2-86	–
LCD_DATA04	O	X2-83	–
LCD_DATA03	O	X2-84	–
LCD_DATA02	O	X2-81	–
LCD_DATA01	O	X2-82	–
LCD_DATA00	O	X2-79	–
LCD_HSYNC	O	X2-76	–
LCD_VSYNC	O	X2-78	–
LCD_CLK	O	X2-72	–
LCD_ENABLE	O	X2-68	–
LCD_RESET#	O	X2-75	–

Display signals LCD_DATA[19:0] also serve as BOOT_CFG[19:0] signals, to load the boot configuration.
It has to be ensured, that displays connected to the carrier board do not interfere with the boot configuration loaded at these pins. Alternatively the Serial Downloader or the internal eFuses can be used.

Attention: Faulty boot process, malfunction	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been fully completed. The end of the power-up sequence is indicated by a high level of signal VCC3V3_MB_EN. Suitable precautions have to be implemented on the carrier board to avoid violations caused e.g. by a display connected at the boot configuration pins. It also has to be ensured that the circuitry at the boot configuration pins (e.g., Pull-Downs) does not interfere with the function of a display connected at these pins.

3.2.5.10 MIPI CSI

The i.MX7 provides a MIPI Camera Serial Interface (CSI), which is routed to the TQMa7x connectors.
The following table shows the signals used by the MIPI CSI:

Table 29: MIPI CSI

Signal	Direction	Pin	Power domain
CSI_CLK_P	I	X3-34	VDDA_PHY_1P8 (i.MX7-internally supplied from VDDA1P8_SW2)
CSI_CLK_N	I	X3-32	
CSI_D1_P	I	X3-28	
CSI_D1_N	I	X3-26	
CSI_D0_P	I	X3-40	
CSI_D0_N	I	X3-38	

3.2.5.11 MIPI DSI

The i.MX7 provides a MIPI Display Serial Interface (DSI), which is routed to the TQMa7x connectors.
The following table shows the signals used by the MIPI_DSI:

Table 30: MIPI DSI

Signal	Direction	Pin	Power domain
DSI_CLK_P	O	X3-37	VDDA_PHY_1P8 (i.MX7-internally supplied from VDDA1P8_SW2)
DSI_CLK_N	O	X3-35	
DSI_D1_P	O	X3-31	
DSI_D1_N	O	X3-29	
DSI_D0_P	O	X3-43	
DSI_D0_N	O	X3-41	

3.2.5.12 PCIe

The i.MX7D provides a PCIe interface, which is routed to the TQMa7x connectors. These pins are NC at the TQMa7S.
The following table shows the signals used by the PCIe interface.

Table 31: PCIe interface

Signal	Direction	Pin	Remark	Power domain
PCIE_TX_N	O	X3-70	Only available with TQMa7D NC with TQMa7S	VDDA_PHY_1P8 (i.MX7-internally supplied from VDDA1P8_SW2)
PCIE_TX_P	O	X3-72		
PCIE_RX_N	I	X3-69		
PCIE_RX_P	I	X3-71		
PCIE_REFCLK_IN_N	I	X3-75		
PCIE_REFCLK_IN_P	I	X3-77		
PCIE_REFCLK_OUT_N	O	X3-76		
PCIE_REFCLK_OUT_P	O	X3-78		

3.2.5.13 PWM

The i.MX7 provides several PWMs, of which four are routed to the TQMa7x connectors.
The following table shows the available PWM signals.

Table 32: PWM

Signal	Direction	Pin	Usage	Power domain
PWM4_OUT	O	X1-51	TQ-Linux-BSP: WDOG1#	VCC3V3_VLDO3
PWM3_OUT	O	X1-49	TQ-Linux-BSP: LCD_PWR_EN	
PWM2_OUT	O	X1-45	TQ-Linux-BSP: LCD_BLT_EN	
PWM1_OUT	O	X1-43	TQ-Linux-BSP: BACKLIGHT_PWM	

3.2.5.14 QSPI

The optional NOR flash on the TQMa7x is connected to the Quad-SPI bus of the i.MX7.
To provide more memory on the carrier board as an alternative, the interface is also routed to connector X3.
The following table shows the signals used by the QSPI interface.

Table 33: QSPI

Signal	Direction	Pin	Remark	Power domain
QSPI_DATA3	I/O	X2-118	–	VCC3V3_VLDO4
QSPI_DATA2	I/O	X2-116	–	
QSPI_DATA1	I/O	X2-114	–	
QSPI_DATA0	I/O	X2-112	–	
QSPI_SS0#	O	X2-113	–	
QSPI_SS1#	O	X2-115	–	
QSPI_RESET#	O	X2-117	–	
QSPI_SCLK	O	X2-109	22 Ω serial termination	

Attention: Malfunction or destruction	
	The QSPI interface may only be used as memory interface. To connect SPI devices the eCSPI interfaces should be used. The QSPI interface should not be connected on the carrier board if QSPI NOR flash is assembled on the TQMa7x, to avoid data transmission errors.

3.2.5.15 SAI

To connect an audio codec via e.g. I2S, the signals of the SAI1 are available from the three SAI interfaces on the TQMa7x connectors. The following table shows the used signals of the SAI interface:

Table 34: SAI interface

Signal	Direction [11]	Pin	Power domain
SAI1_MCLK	O	X2-39	VCC3V3_V33
SAI1_RX_DATA	I	X2-38	
SAI1_RX_BCLK	I	X2-40	
SAI1_RX_SYNC	I	X2-42	
SAI1_TX_DATA	O	X2-30	
SAI1_TX_BCLK	O	X2-32	
SAI1_TX_SYNC	O	X2-34	

3.2.5.16 SIM

The i.MX7 provides two SIM interfaces according to ISO7816 standard. One of these interfaces is available at the TQMa7x connectors to connect e.g. a smart card on the carrier board.
Depending on the type of card used, the supply voltage of 1.8 V, 3.3 V or 5 V has to be provided by the carrier board. Additional level converters are required for this. The wiring of smart cards is defined by the ISO7816 standard.
The following table shows the signals used by the SIM interface.

Table 35: SIM interface

Signal	Direction	Pin	Power domain
SIM_CLK	O	X2-73	VCC3V3_V33
SIM_PD	I	X2-71	
SIM_SVEN	O	X2-69	
SIM_RST#	O	X2-67	
SIM_TRXD	I/O	X2-65	

11: Direction depends on Codec mode.

3.2.5.17 SJC / JTAG

The i.MX7 can operate in two different JTAG modes. The pin JTAG_MOD defines the mode.
The following table shows both modes as well as the mode set on the TQMa7x.

Table 36: JTAG modes

JTAG_MOD	Name	Usage	Remark
0	Daisy Chain All	For common software debug	Default
1	SJC only	IEEE 1149.1 JTAG compliant mode	–

The following table shows the signals used by the JTAG interface.

Table 37: JTAG

Signal	Direction	Pin	Remark	Power domain
JTAG_TCK	I	X1-95	i.MX7-internal 47 kΩ PU	VCC3V3_VLDO3
JTAG_TMS	I	X1-87	i.MX7-internal 47 kΩ PU	
JTAG_TDI	I	X1-89	i.MX7-internal 47 kΩ PU	
JTAG_TDO	O	X1-91	i.MX7-internal 100 kΩ PU	
JTAG_TRST#	I	X1-85	i.MX7-internal 47 kΩ PU	
JTAG_MOD	I	X1-93	4.7 kΩ PD on TQMa7x + i.MX7-internal 100 kΩ PU	

3.2.5.18 TAMPER

The i.MX7 provides protection against unauthorised opening or manipulation of a device by tamper detection.
Ten TAMPER pins are available for this purpose at the TQMa7x connectors.
The following table shows the available signals:

Table 38: TAMPER

Signal	Direction	Pin	Power domain
TAMPER9	I	X1-100	VDD_VSNVS_CAP (i.MX7-internally supplied from VSNVS)
TAMPER8	I	X1-99	
TAMPER7	I	X1-102	
TAMPER6	I	X1-101	
TAMPER5	I	X1-104	
TAMPER4	I	X1-103	
TAMPER3	I	X1-106	
TAMPER2	I	X1-105	
TAMPER1	I	X1-108	
TAMPER0	I	X1-107	

Details about the function of the TAMPER pins are to be taken from the i.MX7 Data Sheets (1), (2), and the i.MX7 Reference Manuals (5), (6).

3.2.5.19 UART

The i.MX7 provides seven UART interfaces. UART3 to UART7, except UART5, provide handshake signals. UART3 to UART7 are available at the TQMa7x connectors as primary function.

The following table shows the signals used by the UART interfaces.

Table 39: UARTs

Signal	Direction	Pin	Remark	Power domain
UART3_RX	I	X1-60	–	VCC3V3_V33
UART3_TX	O	X1-62	–	
UART3_CTS#	O	X1-56	–	
UART3_RTS#	I	X1-58	–	
UART4_RX	I	X3-14	–	
UART4_TX	O	X3-16	–	
UART4_CTS#	O	X3-10	–	
UART4_RTS#	I	X3-12	–	
UART5_RX	I	X1-59	–	
UART5_TX	O	X1-61	–	
UART6_RX	I	X1-111	RS-232 on MBa7x	VCC3V3_VLDO4
UART6_TX	O	X1-113	RS-232 on MBa7x	
UART6_CTS#	O	X1-115	RS-232 on MBa7x	
UART6_RTS#	I	X1-117	RS-232 on MBa7x	
UART7_RX	I	X1-112	–	
UART7_TX	O	X1-114	–	
UART7_CTS#	O	X1-116	–	
UART7_RTS#	I	X1-118	–	

Note: RS-232 interface on the MBa7x	
	UART6 is used as RS-232 interface on the MBa7x.

3.2.5.20 USB

The i.MX7 provides a USB-Host as HSIC interface to connect an external USB-HSIC PHY.
Additionally the i.MX7D provides two, the i.MX7S one USB 2.0 OTG interface. Both interfaces can also be configured as Host.
The HSIC signals on the carrier board may have a maximum length of 50 mm.
The following table shows the signals used by the USB OTG1 interface.

Table 40: USB OTG1

Signal	Direction	Pin	Remark	Power domain
USB_OTG1_DP	I/O	X2-27	–	VCC3V3_V33
USB_OTG1_DN	I/O	X2-25	–	
USB_OTG1_ID	I	X2-26	Device Mode: Connect with Micro-USB connector Host Mode: Connect with Micro-USB connector and Ground	
USB_OTG1_CHD#	O	X2-24	100 kΩ PU to 3.3 V on TQMa7x	n.a.
USB_OTG1_PWR	O	X2-19	–	VCC3V3_VLDO3
USB_OTG1_OC	I	X2-17	–	
USB_OTG1_VBUS	P	X2-21	Connect to 5 V on carrier board	n.a.

The following table shows the signals used by the USB OTG2 interface.

Table 41: USB OTG2

Signal	Direction	Pin	Remark	Power domain
USB_OTG2_DP	I/O	X3-22	Only on TQMa7D. NC on TQMA7S.	VCC3V3_V33
USB_OTG2_DN	I/O	X3-20	Only on TQMa7D. NC on TQMA7S.	
USB_OTG2_ID	I	X3-13	Only on TQMa7D. NC on TQMA7S. Device Mode: Connect with Micro-USB connector Host Mode: Connect with Micro-USB connector and Ground	
USB_OTG2_PWR	O	X3-9	TQMa7S: GPIO1_IO07	VCC3V3_VLDO3
USB_OTG2_OC	I	X3-11	TQMa7S: GPIO1_IO06	
USB_OTG2_VBUS	P	X3-15	Connect to 5 V on carrier board. NC on TQMA7S.	n.a.

The following table shows the signals used by the USB HSIC interface.

Table 42: USB HSIC

Signal	Direction	Pin	Power domain
USB_HOST_DATA	I/O	X2-35	VDD_1P2_CAP (i.MX7-internal LDO from VDDA1P8_SW2)
USB_HOST_STROBE	I/O	X2-31	

Note: HSIC signal length	
	The maximum HSIC signal length on the carrier board is 50 mm, from the TQMa7x pin.

3.2.5.21 uSDHC

The i.MX7 uSDHC1 port is routed to the TQMa7x connectors to connect an MMC, SD or SDIO card.

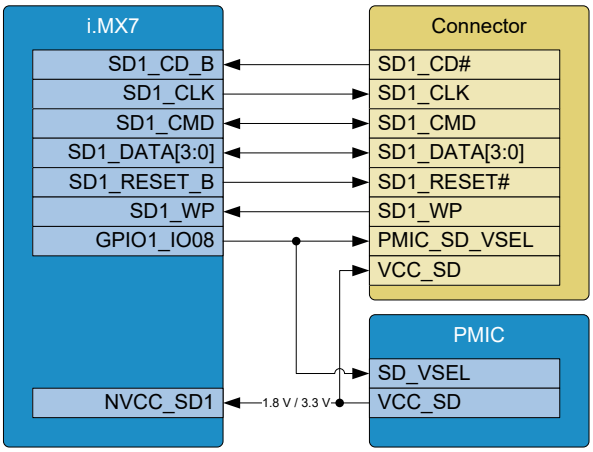


Figure 12: Block diagram SD card interface

The interface supports transfer rates of up to UHS-I mode (SDR104) with 208 MHz or 104 MB/s. The I/O voltage of the USDHC interface must be reduced from 3.3 V to 1.8 V to use the UHS-I mode. The TQMa7x-internal signal PMIC_SD_VSEL is used during card detection for this purpose. The signal is available as an output at the TQMa7x connectors.

PMIC_SD_VSEL is not required on the carrier board for the SD card function and should therefore be not connected.

The IO voltage must be switched by software as defined in the SD card specification.

It is not permitted to switch the voltage by feeding a voltage at pin PMIC_SD_VSEL.

The following table shows the signals used by the USDHC1 interface.

Table 43: uSDHC1

Signal	Direction	Pin	Remark
SD1_DATA7	I/O	X2-20	Multiplexed as eCSPI2, see 3.2.7.4
SD1_DATA6	I/O	X2-15	
SD1_DATA5	I/O	X2-18	
SD1_DATA4	I/O	X2-13	
SD1_DATA3	I/O	X2-10	–
SD1_DATA2	I/O	X2-7	–
SD1_DATA1	I/O	X2-8	–
SD1_DATA0	I/O	X2-5	–
SD1_CLK	O	X2-9	–
SD1_CMD	I/O	X2-6	–
SD1_CD#	I	X2-14	–
SD1_WP	I	X2-12	–
SD1_RESET#	O	X2-3	–
PMIC_SD_VSEL	O	X2-4	No SD card signal, treat as NC on carrier board

3.2.5.22 WDOG

The i.MX7 provides four Watchdog Timer. WDOG1 and WDOG2 are routed to the TQMa7x connectors.
The following table shows the signals used by the Watchdog Timers.

Table 44: WDOG

Signal	Direction	Pin	Remark
WDOG1#	O	X1-51	TQ-Linux-BSP: WDOG1#
WDOG2#	O	X2-43	See Trust-Zone feature in (1), (2)
WDOG2_RESET#	I	X2-45	

WDOG1# can be used to process Warm-Resets by software. In this case the output has to be connected to RESET_IN# on the carrier board as shown in the following block diagram.

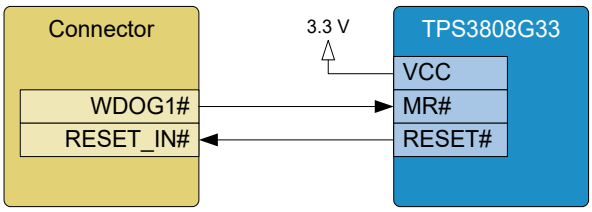


Figure 13: Block diagram Watchdog

3.2.6 Reset

Reset inputs or outputs are available at the TQMa7x connectors.
The following block diagram shows the reset signals wiring.

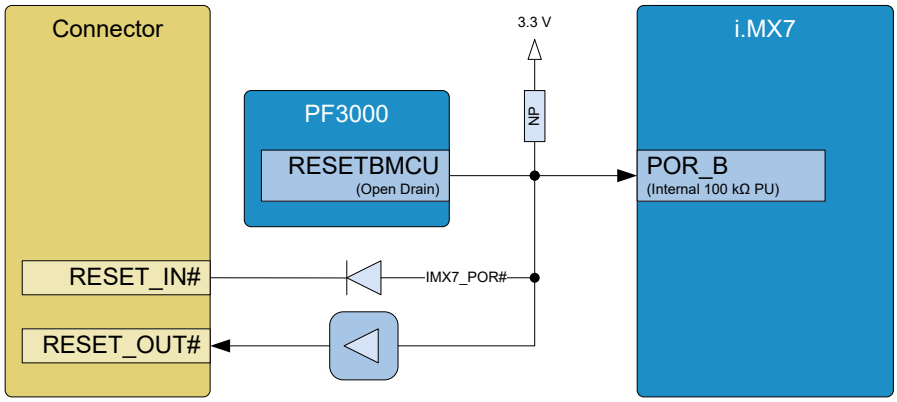


Figure 14: Block diagram Reset

The following table describes the reset signals available at the connectors.

Table 45: Reset

Signal	Direction	Pin	Remark
RESET_IN#	I	X1-22	• i.MX7 Reset input (POR_B) • Internal pull-up 100 kΩ • To deactivate: float or pull-up to max. 3.3 V • Low-active signal • Input for external supervisor to reset the watchdog
RESET_OUT#	O	X1-20	• Should be used to reset external periphery on the carrier board • Open drain, requires PU on carrier board

The pull-up at RESET_OUT# can be connected to voltages greater than 3.3 V. In any case the max. input current of 50 mA and the specification of the used output driver 74LVC1G07 from NXP must be observed.

3.2.7 Power supply

3.2.7.1 TQMa7x power supply

The TQMa7x only requires a single 5 V ±5 % supply. No other voltage is required.

In addition to the PMIC from NXP, another voltage converter (DCDC4V2) is used on the TQMa7x. This is used to generate the basic supply voltage of the PMIC. The following block diagram shows the TQMa7x power supply:

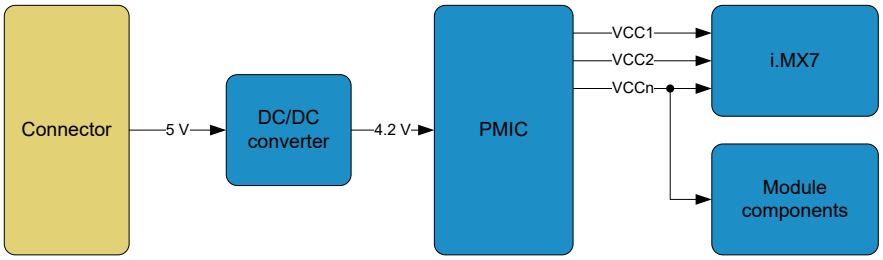


Figure 15: Block diagram TQMa7x power supply

The characteristics and functions of the pins and signals are to be taken from the PMIC Data Sheet (4) and the i.MX7 Data Sheets (1), (2).

3.2.7.2 Other TQMa7x supply inputs

In addition to VCC5V two more supply inputs are provided by the TQMa7x.

Table 46: TQMa7x Supply inputs

Voltage	Pin	Usage	V_{IN}	I_{IN}
VCC1V8_IN	X1-66	Supplies i.MX7 rails for temperature sensor and ADC Connect to VCC1V8_OUT or external supply voltage	1.71 V to 1.89 V, 1.8 V typ.	15 mA
LICELL	X1-19	RTC supply Connected to PMIC-LICELL or DS1339, if assembled	See PMIC Data Sheet (4) and DS1339 Data Sheet (9)	See 3.2.3

Attention: Malfunction or destruction	
	When using an external supply at VCC1V8_IN the power sequencing of the CPU must be respected. Therefore VCC1V8_OUT should be used as enable for the external supply.

3.2.7.3 Provided TQMa7x-internal voltages

Several voltages generated on the TQMa7x are routed to connector X1.

Table 47: Provided TQMa7x-internal voltages

Voltage	PMIC source	Pin	Usage	Max. load
VCC3V3_V33	V33	X1-13	Pull-Up voltage for BOOT_CFG[19:0]	30 mA
VCC3V3_VLDO3	VLDO3	X1-15	I/O voltage for GPIO banks 1 and 2 in LPSR mode, (12) Pull-Up voltage for BOOT_MODE[1:0]	25 mA
VCC1V8_OUT	SW2	X1-65	ADC reference voltage, see 3.2.7.2	150 mA
VCC_SD	VCC_SD	X1-14	I/O voltage for USDHC1 (1.8 V / 3.3 V), Depending on SD card mode switchable Pull-Up voltage for SD card signals	15 mA
VSNVS	VSNVS	X1-16	Supply voltage for Low-Power Standby devices (e.g. RTC)	50 µA
VCC3V3_MB_EN	VLDO2	X1-26	Enable voltage for 3.3 V regulator on carrier board, typ. 1.5 V	5 mA

Attention: Malfunction or destruction	
	All voltages mentioned above are supply voltages, do not feed voltage at these pins! Overload might cause functional instabilities of the TQMa7x.

3.2.7.4 TQMa7x power consumption

The given power consumption has to be seen as an approximate value.
The TQMa7x power consumption strongly depends on the application, the mode of operation and the operating system.
The following table shows power supply and TQMa7x power consumption parameters.

Table 48: Parameter TQMa7x power consumption @ 5 V

TQMa7x	Mode	Current consumption	Remark
TQMa7S (Solo)	Off-mode	6 mA	PMIC_PWRON = low
	Reset	26 mA	RESET_IN# = low
	U-Boot prompt, idle	115 mA	–
	Linux prompt, idle	95 mA	–
	Linux 100 % CPU load	200 mA	Higher current consumption must be expected when using additional interfaces in parallel
	Current consumption theoretical worst case	1.44 A	
TQMa7D (Dual)	Off-mode	6 mA	PMIC_PWRON = low
	Reset	21 mA	RESET_IN# = low
	U-Boot prompt, idle	130 mA	–
	Linux prompt, idle	100 mA	–
	Linux 100 % CPU load	220 mA	Higher current consumption must be expected when using additional interfaces in parallel
	Current consumption theoretical worst case	1.44 A	

Further information on power consumption and the energy savings options can be found in NXP Application Note AN5383 (8).

12: For Standby modes see i.MX7 Data Sheets (1), (2).

3.2.7.5 Voltage monitoring

The TQMa7x features a supervisor which monitors the input voltage (VCC5V).
If the input voltage is too low, the input regulator DCDC4V2 will not be activated or deactivated.
The following block diagram shows the monitoring circuitry wiring:

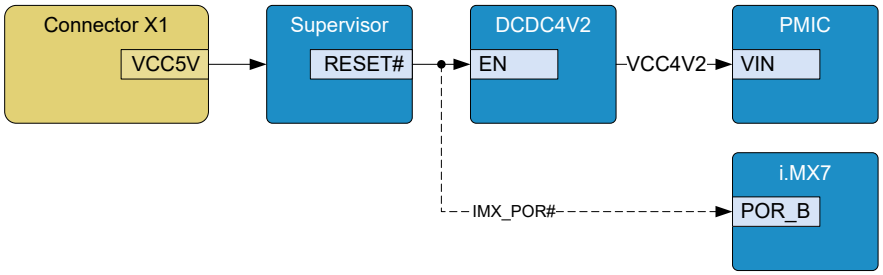


Figure 16: Block diagram Supervisor VCC5V

Alternatively, a placement option allows the supervisor to perform a reset instead of a power cycle via IMX_POR#. The Supervisor typically triggers at 4.45 V (min: 4.32 V / max: 4.59 V) and pulls RESET# low for 300 ms. The delay can be adjusted per placement options. Please contact TQ-Support in case a different delay is required.

Attention: Malfunction or destruction	
	The voltage monitoring does not detect overvoltage. Do not try to reprogram the PMIC since this may cause the i.MX7 or other peripherals on the TQMa7x to operate outside their specification. An excessively high input voltage can lead to malfunction, deterioration or destruction of the TQMa7x.

3.2.7.6 Power-Up sequence TQMa7x / carrier board

The TQMa7x meets the sequencing required by the i.MX7 (1), (2) through the pre-programmed PMIC (4).

The TQMa7x has to be supplied with 5 V, the 3.3 V I/O voltage of the i.MX7 signals is generated on the TQMa7x.
This leads to requirements for the carrier board design concerning the chronological order of the voltages generated on the carrier board.

The carrier board supply of 3.3 V is to be enabled exclusively by the module pin VCC3V3_MB_EN (X1-26).

The following block diagram shows how the 3.3 V supply on carrier board has to be enabled.

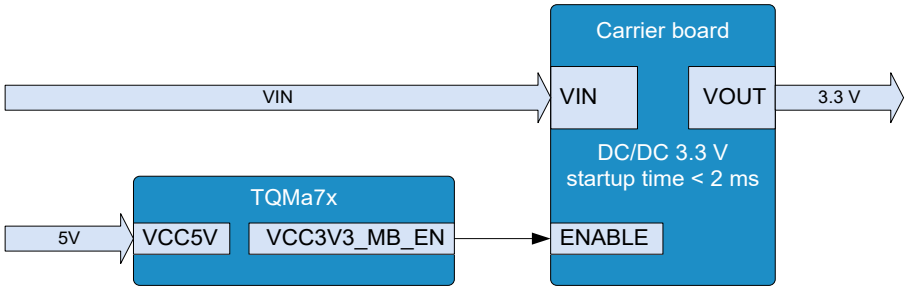


Figure 17: Block diagram 3.3 V supply on carrier board

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been fully completed. The end of the power-up sequence is indicated by a high level of signal VCC3V3_MB_EN.

Note: BOOT_MODE / BOOT.CFG	
	The BOOT_MODE and BOOT.CFG pins each have dedicated reference voltages, which are provided by the TQMa7x, see 3.2.9.3.

3.2.7.7 Standby

The i.MX7 supports in combination with the PMIC several Standby modes. Details can be found in the i.MX7 Data Sheets (1), (2) and the PMIC Data Sheet (4).

Note: Suspend to RAM	
	Suspend-to-RAM is not supported in LPSR mode. TQMa7x with discrete RTC (see 3.2.3) have to be supplied with 5 V, if the PMIC Standby feature has to be used, since the PMIC LICELL pin is not supplied.

3.2.7.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX7 Reference Manuals (5), (6) and the PMIC Data Sheet (4). The PMIC is connected to the I2C1 bus of the i.MX7.
The following block diagram shows the connection between PMIC and i.MX7.

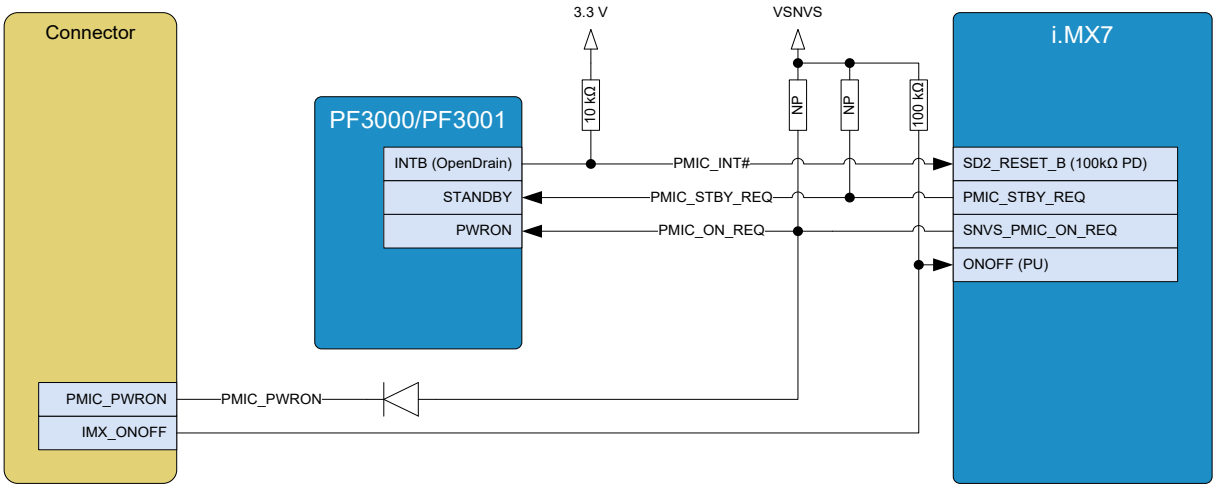


Figure 18: Block diagram PMIC interface

➢ The PMIC has I²C address `0x08 / 000 1000b`. The address can be altered by software.

The following two signals of PMIC and Power-Management are provided at the TQMa7x connectors:

Table 49: PMIC

Signal	Direction	Pin	Remark	Power domain
PMIC_PWRON	I	X1-21	• Switches the PMIC off when signal is active • Power cycle starts when signal is deactivated • Low active signal • To deactivate: Float or pull-up to 3.3 V	VSNVS (3.0 V)
IMX_ONOFF	I	X1-24	• Switches i.MX7 to Off- or SNVS mode • Depends on software and current i.MX7 Power Mode • See i.MX7 Data Sheets (1), (2)	

By using the pre-programmed PMIC type A1, no own configuration of the PMIC is necessary. The configuration can be taken completely from the data sheet (4).
According to the specification the PMIC can be configured via the I2C1 interface after the system start.

Attention: Malfunction or destruction	
	Improper PMIC programming may cause the i.MX7 or other peripherals on the TQMa7x to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa7x.

4. MECHANICS

4.1 Connectors

The TQMa7x is connected to the carrier board with 320 pins on three connectors.

The following table shows some connector details.

Table 50: Connectors assembled on the TQMa7x

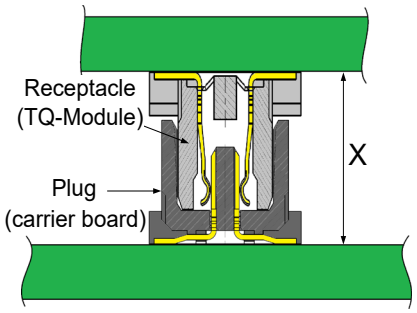
Manufacturer	Part number	Remark
TE connectivity	80-pin: 5177985-3 120-pin: 5-353999-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMa7x is held in the mating connectors with a retention force of approximately 32 N.
To avoid damaging the connectors of the TQMa7x as well as the connectors on the carrier board while removing the TQMa7x the use of the extraction tool MOZI8XXL is strongly recommended. See chapter 4.9 for further information.

Attention: Component placement on the carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa7x for the extraction tool MOZI8XXL.

The following table shows suitable mating plug connectors for the carrier board.

Table 51: Suitable carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	80-pin: 5177986-3 120-pin: 5177986-5	On MBa7x	5 mm	
	80-pin: 1-5177986-3 120-pin: 1-5177986-5	–	6 mm	
	80-pin: 2-5177986-3 120-pin: 2-5177986-5	–	7 mm	
	80-pin: 3-5177986-3 120-pin: 3-5177986-5	–	8 mm	

The pin assignment in Table 3, Table 4, Table 5, and Table 8 refer to the BSP provided by TQ-Systems.
Information regarding the I/Os in Table 3, Table 4, Table 5, and Table 8, refer to the i.MX7 pins.

4.2 TQMa7x dimensions

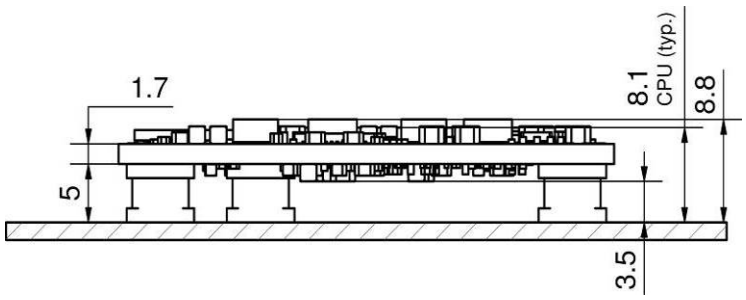


Figure 19: TQMa7x dimensions, side view

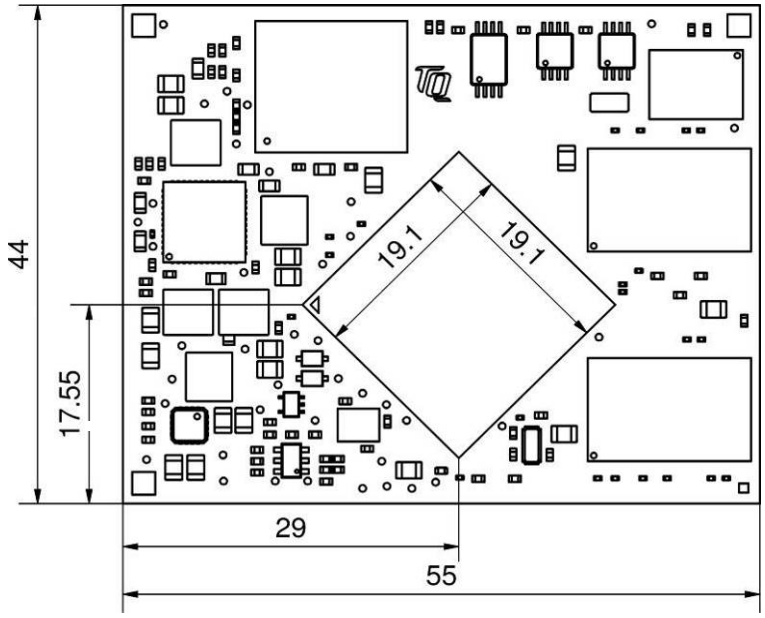


Figure 20: TQMa7x dimensions, top view

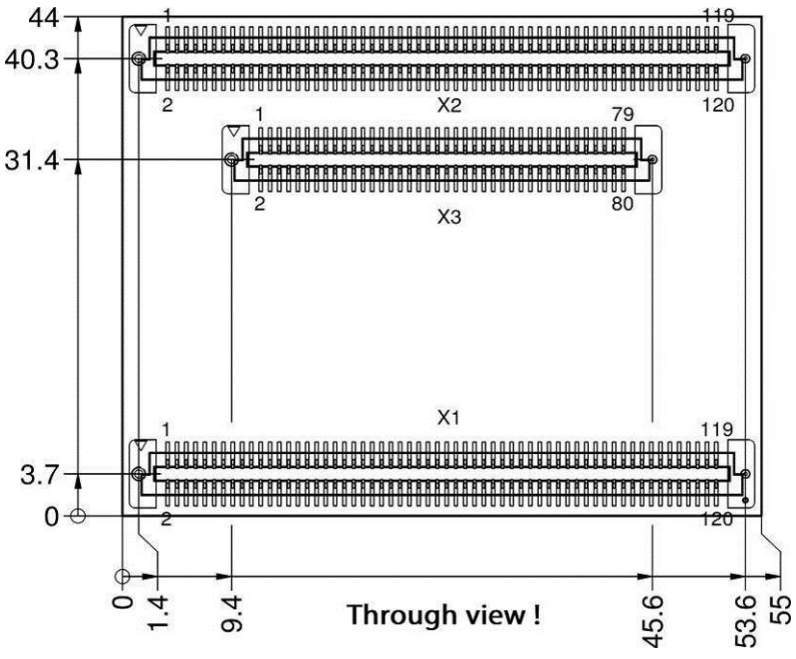


Figure 21: TQMa7x dimensions, top view **through** TQMa7x

4.3 TQMa7x component placement

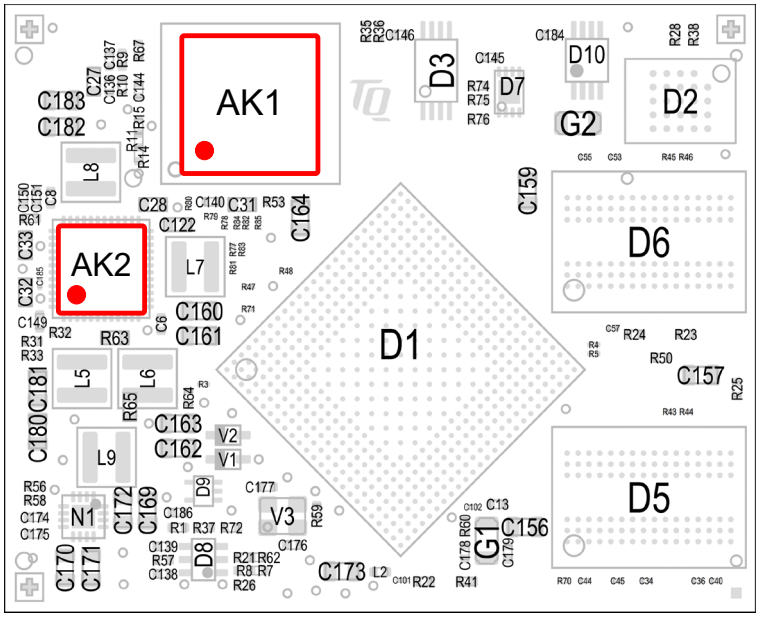


Figure 22: TQMa7x, component placement top, revision 02xx

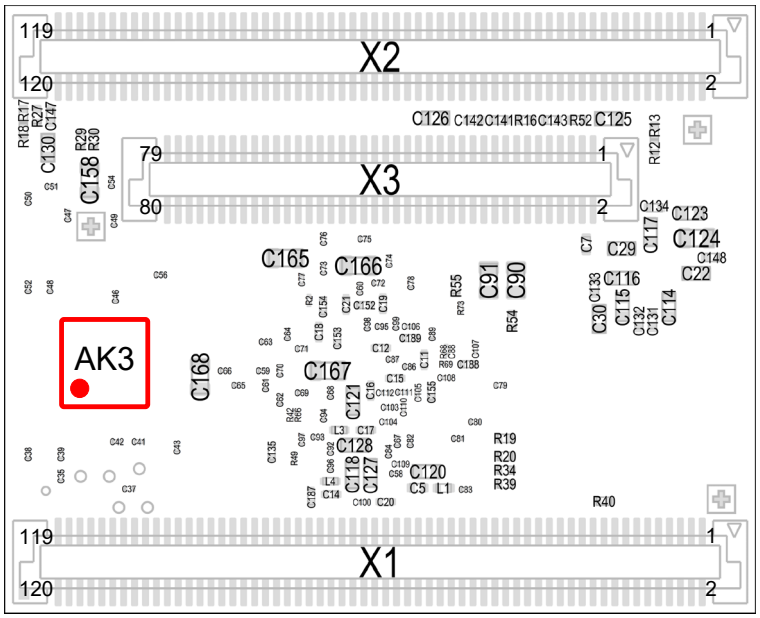


Figure 23: TQMa7x, component placement bottom, revision 02xx

The labels on the TQMa7x show the following information:

Table 52: Labels on TQMa7x revision 02xx

Label	Content
AK1	First MAC address plus one additional reserved consecutive MAC address, tests performed
AK2	TQMa7x version and revision
AK3	Serial number

4.4 Adaptation to the environment

The TQMa7x has overall dimensions (length × width) of 55 mm × 44 mm (± 0,1 mm).
The TQMa7x has a maximum height above the carrier board of approximately 8.8 mm.
The TQMa7x weighs approximately 17 g.

4.5 Protection against external effects

As an embedded module, the TQMa7x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa7x, a maximum of approximately 7.2 W must be dissipated, see Table 48 for peak currents. The power dissipation originates primarily in the CPU, the DDR3 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
For further information see PMIC Data Sheet (4) and chapter 3.2.7.2.

Attention: Malfunction or destruction, TQMa7x heat dissipation	
	The TQMa7x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX7 must be taken into consideration when connecting the heat sink, see (8). The i.MX7 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa7x and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa7x is held in the mating plug connectors by the retention force of the 320 pins. For high requirements with respect to vibration and shock firmness, an additional holder has to be provided in the final product to hold the TQMa7x in its position. As no heavy and big components are assembled, no further requirements are given.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa7x may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Component placement on the carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa7x for the extraction tool MOZI8XXL.

5. SOFTWARE

The TQMa7x is delivered with a preinstalled boot loader U-Boot and a BSP provided by TQ-Systems, which is configured for the combination of TQMa7x and MBa7x. The boot loader U-Boot provides module-specific as well as board-specific settings, e.g.:

- i.MX7 configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Pin multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted for other bootloaders. More information can be found in the TQMa7x Support Wiki (11).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa7x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the carrier board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked signals (e.g., clock) should be kept short; avoid interference of other signals by distance and / or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)
- Direct routing without stubs

Since the TQMa7x operates on an application-specific carrier board, EMC or ESD tests are only applicable for the whole device.
The TQMa7x was tested in combination with the MBa7x revision 0200 according to DIN EN 55022:2010, Limit Value Class A.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures are taken on the TQMa7x.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Reliability and service life

The theoretical MTBF of the TQMa7x is approximately 1,150,000 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa7x is designed to be insensitive to shock and vibration.
High quality industrial grade connectors are assembled on the TQMa7x.
Detailed information concerning the service life of the i.MX7 under different operational conditions is to be taken from the NXP Application Note (3).

6.5 Climate and operational conditions

The temperature range, in which the TQMa7x can operate, strongly depends on the installation situation (heat dissipation by heat conduction and convection); therefore no fixed value can be given for the whole assembly.
In general, a reliable operation is given when following conditions are met.

Table 53: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Ambient temperature	–20 °C to +70 °C	The values were determined under the following conditions: • i.MX7 load: 90 % to 100 % • Clock frequency: 800 MHz • rel. humidity: 50 %
T_J temperature i.MX7	–20 °C to +105 °C	–
T_J temperature PMIC	–40 °C to +125 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Storage temperature TQMa7x	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the i.MX7 is to be taken from the i.MX7 Data Sheets (1), (2).

Attention: Malfunction or destruction, TQMa7x heat dissipation	
	The TQMa7x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX7 must be taken into consideration when connecting the heat sink, see (8). The i.MX7 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa7x and thus malfunction, deterioration or destruction.

6.6 Shock and Vibration

Table 54: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 55: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa7x is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa7x was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly.

7.4 EuP

The guideline 2005/32/EC (EuP) only applies for quantities >200,000 p/a. The consideration of environmental requirements with the product design "creation appropriate for the environment" ("ecological design") with the aim to improve the environmental compatibility of the product during its whole life cycle should be taken into consideration. The guideline appropriate for the product (embedded PC) applies.

7.5 Battery

No batteries are assembled on the TQMa7x.

7.6 Packaging

The TQMa7x is delivered in reusable packaging.

7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa7x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa7x is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document.

Table 56: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CCM	Clock Control Module
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDR	Double Data Rate
DDR3L	DDR3 Low Voltage
DIN	Deutsche Industrienorm (German industry standard)
DSI	Display Serial Interface
eCSPI	enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIM	External Interface Module
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ENET	Ethernet
ESAI	Enhanced Serial Audio Interface
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
HRCW	Hard Reset Configuration Word
HSIC	High-Speed Inter-Chip
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
IPU	Input, Pull-Up
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LPSR	Low Power State Retention
LVDS	Low Voltage Differential Signalling
MAC	Media Access Control
MII	Media-Independent Interface
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MMDC	Multi-Mode DDR Controller
MMU	Memory Management Unit
MTBF	Mean (operating) Time Between Failures
n.a.	Not Applicable
NAND	Not-And
NC	Not Connected

8.1 Acronyms and definitions (continued)

Table 60: Acronyms (continued)

Acronym	Meaning
NOR	Not-Or
NP	Not Placed
OOD	Output, Open-Drain
OTG	On-The-Go
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	PCI Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor / Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SD card	Secure Digital Card
SD/eSD/SDXC	Secure Digital / enhanced Secure Digital / SD eXtended Capacity
SD/MMC	Secure Digital Multimedia Card
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input/Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SJC	System JTAG Controller
SMP	Sampling
SNVS	Secure Non-Volatile Storage
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
SW	Software
UART	Universal Asynchronous Receiver/Transmitter
U-Boot	Universal Bootloader
UHS	Ultra High Speed
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
VSNVS	Voltage (for) Secure Non-Volatile Storage
WC	Write-Control
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 57: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 7Dual Family of Applications Processors Data Sheet, IMX7DCEC	6.0, 03/2019	NXP
(2)	i.MX 7Solo Family of Applications Processors Data Sheet, IMX7SCEC	6.0, 03/2019	NXP
(3)	i.MX7 Dual/Solo Product Lifetime Usage, AN5334	1.0, 05/2017	NXP
(4)	Power Management integrated circuit for i.MX7 & i.MX 6SL/SX/UL, PF3000 PMIC	9.0, 08/2017	NXP
(5)	i.MX 7Dual Applications Processor Reference Manual, IMX7DRM	1.0, 01/2018	NXP
(6)	i.MX 7Solo Applications Processor Reference Manual, IMX7SRM	0.1, 08/2016	NXP
(7)	i.MX7S & i.MX7D, IMX7D_2N09P Mask Set Errata	1.0, 08/2017	NXP
(8)	i.MX 7DS Power Consumption Measurements, AN5383	1.0, 06/2019	NXP
(9)	DS1339U Data Sheet	3/15, 2015	Maxim
(10)	MBa7x User's Manual	– current –	TQ-Systems
(11)	TQMa7x Support-Wiki	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group I TQ-Group

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