# TQMa8XxS
# User's Manual

TQMa8XxS UM 0103
20.09.2022

# TABLE OF CONTENTS

# TABLE DIRECTORY

# FIGURE DIRECTORY



# REVISION HISTORY

| Rev. | Date | Name | Pos. | Modification |
|---|---|---|---|---|
| 0100 | 01.12.2021 | Kreuzer | All | Initial release |
| 0101 | 25.01.2022 | Kreuzer | 3.8.1, 3.8.1.1<br>Table 19, Figure 29 | Voltage input range VDD_IN corrected<br>Clearer wording |
| 0102 | 31.05.2022 | Kreuzer | Table 2<br>3.3.2 | Level for pin P64 changed; footnote added<br>Added note to level conversion USB0_OTG_ID |
| 0103 | 20.09.2022 | Kreuzer | Table 14 | Warning notice intensified |

# 1. ABOUT THIS MANUAL

## 1.1 Copyright and license expenses



This User's Manual may not be copied, reproduced, translated, changed or distributed, completely or partially in electronic, machine readable, or in any other form without the written consent of TQ-Systems GmbH.

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be calculated / declared separately.

## 1.2 Registered trademarks

TQ-Systems GmbH aims to adhere to copyrights of all graphics and texts used in all publications, and strives to use original or license-free graphics and texts.

All brand names and trademarks mentioned in this User's Manual, including those protected by a third party, unless specified otherwise in writing, are subjected to the specifications of the current copyright laws and the proprietary laws of the present registered proprietor without any limitation. One should conclude that brand and trademarks are rightly protected by a third party.

## 1.3 Disclaimer

TQ-Systems GmbH does not guarantee that the information in this User's Manual is up-to-date, correct, complete or of good quality. Nor does TQ-Systems GmbH assume guarantee for further usage of the information. Liability claims against TQ-Systems GmbH, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this User's Manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of TQ-Systems GmbH.

TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this User's Manual or parts of it without special notification.

**Important Notice:**

Before using the MB-SMARC-2 or parts of the schematics of the MB-SMARC-2, you must evaluate it and determine if it is suitable for your intended application. You assume all risks and liability associated with such use. TQ-Systems GmbH makes no other warranties including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. Except where prohibited by law, TQ-Systems GmbH will not be liable for any indirect, special, incidental or consequential loss or damage arising from the usage of the MB-SMARC-2 or schematics used, regardless of the legal theory asserted.

## 1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
**D-82229 Seefeld**

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

## 1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

## 1.6 Symbols and typographic conventions

Table 1: Terms and conventions

| Symbol | Meaning |
|---|---|
|  | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|  | This symbol indicates the possible use of voltages higher than 24 V.<br>Please note the relevant statutory regulations in this regard.<br>Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component. |
|  | This symbol indicates a possible source of danger.<br>Ignoring the instructions described can cause health damage, or damage the hardware. |
|  | This symbol represents important details or aspects for working with TQ-products. |
| `Command` | A font with fixed-width is used to denote commands, contents, file names, or menu items. |

## 1.7 Handling and ESD tips

General handling of your TQ-products

| | |
|---|---|
|  | The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.<br>A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.<br>Violation of this guideline may result in damage / destruction of the TQMa8XxS and be dangerous to your health.<br>Improper handling of your TQ-product would render the guarantee invalid. |

Proper ESD handling

| | |
|---|---|
|  | The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).<br>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices. |

## 1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

## 1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MB-SMARC-2 circuit diagram
- MB-SMARC-2 User's Manual
- i.MX 8X Data Sheet
- i.MX 8X Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8XxS

# 2. BRIEF DESCRIPTION

This User's Manual describes the hardware of TQMa8XxS revision 03xx in combination with the MB-SMARC-2 and refers to some software settings. The MB-SMARC-2 serves as an evaluation board for the TQMa8XxS. A certain TQMa8XxS derivative does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP i.MX 8X Reference Manual (2). The CPU derivatives provide dual, and quad ARM® Cortex®-A35 cores, and up to two Dual ARM® Cortex®-M4 co-processors. In addition, the CPUs include an OpenGL ES 3.0 or 3.1 GPU as well as a VPU supporting up to 4K h.265 decoder.

The TQMa8XxS is a universal Minimodule based on these NXP ARM® Cortex®-A35 i.MX 8X CPUs, see also Table 3.

An i.MX 8X Cortex®-A35 core typically operates at 1.2 GHz.

## 2.1 Block diagram i.MX 8X

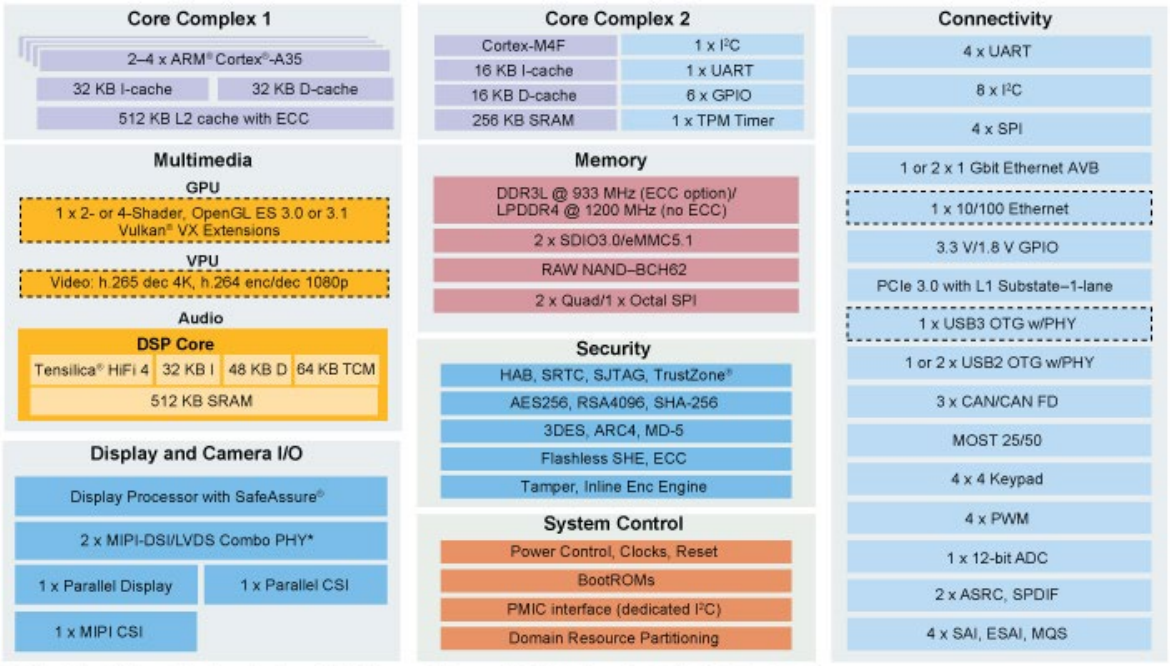


Figure 1: Block diagram i.MX 8X CPU
(Source: NXP)

## 2.2 Key functions and characteristics

The TQMa8XxS extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 8X derivative (i.MX 8DualX, i.MX 8DualXPlus or i.MX 8QuadXPlus) can be selected for each requirement.

The signals are routed to the card edge connector according to SMARC 2.0. All essential components like CPU, LPDDR4 SDRAM, eMMC, and power management are already integrated on the TQMa8XxS. The main features of the TQMa8XxS are:

- 64-bit NXP i.MX 8X CPU with up to 4 × ARM® Cortex®-A35 and 1 × ARM® Cortex®-M4F
- Derivatives: i.MX 8DualX / i.MX 8DualXPlus / i.MX 8QuadXPlus
- Standard form factor according to SMARC 2.0 (82 mm x 50 mm)
- Up to 4 GByte LPDDR4 SDRAM (32 bit)
- Up to 32 Gbyte eMMC NAND flash
- Up to 256 Mbyte QSPI NOR flash (optional)
- 64 kbit EEPROM
- EEPROM + temperature sensor
- DSI-to-eDP bridge
- PCIe clock generator
- NXP Power Management, “ASIL B” ready
- RTC (optional)
- Trust Secure Element (optional)
- Temperature sensor
- Interface compatibility according to SMARC 2.0
- Boot mode selection on TQMa8XxS
- 3.3 V fixed supply voltage (optional: extended voltage range of 3.0 V to 5.25 V)
- Form factor 82 mm x 50 mm

The IO voltage of most interfaces is set to 1.8 V by the SMARC standard. Signals for differential high-speed interfaces have different standardized IO levels.

# 3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8XxS, and the BSP provided by TQ-Systems GmbH, see also section 5.

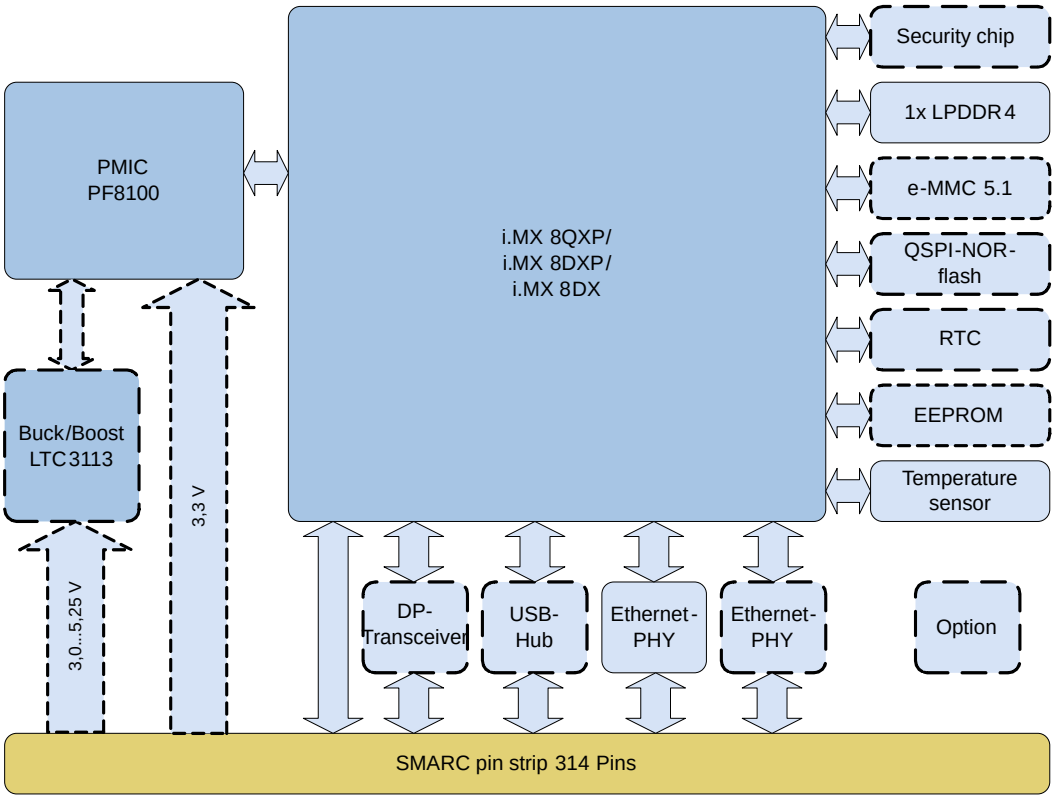


Figure 2: Block diagram TQMa8XxS

## 3.1 Interfaces to other systems and devices

The TQMa8XxS has a SMARC pin strip with a total of 314 pins, divided between the top and bottom of the board, via which it is connected to the baseboard. Furthermore, the module has four holes with which it can be fixed to the carrier board by means of screws.

### 3.1.1 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
The pin assignment listed in Table 2 refers to the corresponding BSP provided by TQ-Systems GmbH in combination with the MB-SMARC-2.
The electrical and pin characteristics are to be taken from the i.MX 8X Data Sheet (1), the i.MX 8X Reference Manual (2), and the PMIC Data Sheet (6).
Some signals are not present on the TQMa8XxS with i.MX 8X Dual CPU or they have different functions.

| Attention: Destruction or malfunction | |
|---|---|
|  | Depending on the configuration, many i.MX 8X balls can provide several different functions.<br>Please take note of the information in the i.MX 8X Reference Manual (2), and the i.MX 8X Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board.<br>Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8XxS.<br><br>The meanings given in the following tables must be observed:<br>RFU: Reserved pins without function.<br>To support future TQMa8XxS versions, these pins must not be connected.<br>DNC: These pins must not be connected, they have to be left open. |

### 3.1.2 SMARC connector X1

Table 2: Pinout SMARC connector X1

| Ball | Dir. | Level | Group | Signal | Pin | | Signal | Group | Level | Dir. | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | S1 | MIPI_CSI_I2C0_SCL | CSI1 | 1.8 V | O | AP26 |
| G35 | I | 1.8 V | CONFIG | SMB_ALERT# | P1 | S2 | MIPI_CSI_I2C0_SDA | CSI1 | 1.8 V | I/O | AM24 |
| – | – | 0 V | Power | GND | P2 | S3 | GND | Power | 0 V | – | – |
| AR21 | O | 1.8 V | CSI1 | MIPI_CSI_CLKP | P3 | S4 | RFU | – | – | – | – |
| AN21 | O | 1.8 V | CSI1 | MIPI_CSI_CLKN | P4 | S5 | DNC | – | – | – | – |
| – | – | – | – | DNC | P5 | S6 | MIPI_CSI_MCLK | CSI1 | 1.8 V | – | AN25 |
| – | I/O | 3.3 V | GBE0 | GBE0_SDP | P6 | S7 | DNC | – | – | – | – |
| AP22 | I | 1.8 V | CSI1 | MIPI_CSI_DP0 | P7 | S8 | DNC | – | – | – | – |
| AM22 | I | 1.8 V | CSI1 | MIPI_CSI_DN0 | P8 | S9 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P9 | S10 | GND | Power | 0 V | – | – |
| AP20 | I | 1.8 V | CSI1 | MIPI_CSI_DP1 | P10 | S11 | DNC | – | – | – | – |
| AM20 | I | 1.8 V | CSI1 | MIPI_CSI_DN1 | P11 | S12 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P12 | S13 | GND | Power | 0 V | – | – |
| AR23 | I | 1.8 V | CSI1 | MIPI_CSI_DP2 | P13 | S14 | DNC | – | – | – | – |
| AN23 | I | 1.8 V | CSI1 | MIPI_CSI_DN2 | P14 | S15 | DNC | – | – | - | – |
| – | – | 0 V | Power | GND | P15 | S16 | GND | Power | 0 V | – | – |
| AR19 | I | 1.8 V | CSI1 | MIPI_CSI_DP3 | P16 | S17 | GBE1_MDI_P0 | GBE1 | – | A | – |
| AN19 | I | 1.8 V | CSI1 | MIPI_CSI_DN3 | P17 | S18 | GBE1_MDI_N0 | GBE1 | – | A | – |
| – | – | 0 V | Power | GND | P18 | S19 | DNC | – | – | – | – |
| – | A | – | GBE0 | GBE0_MDI_N3 | P19 | S20 | GBE1_MDI_P1 | GBE1 | – | A | – |
| – | A | – | GBE0 | GBE0_MDI_P3 | P20 | S21 | GBE1_MDI_N1 | GBE1 | – | A | – |
| – | – | – | – | DNC | P21 | S22 | GBE1_LINK1000# | GBE1 | 3.3 V | O | – |
| – | O | 3.3 V | GBE0 | GBE0_LINK1000# | P22 | S23 | GBE1_MDI_P2 | GBE1 | – | A | – |
| – | A | – | GBE0 | GBE0_MDI_N2 | P23 | S24 | GBE1_MDI_N2 | GBE1 | – | A | – |
| – | A | – | GBE0 | GBE0_MDI_P2 | P24 | S25 | GND | Power | 0 V | – | – |
| – | O | 3.3 V | GBE0 | GBE0_LINK_ACT# | P25 | S26 | GBE1_MDI_P3 | GBE1 | – | A | – |
| – | A | – | GBE0 | GBE0_MDI_N1 | P26 | S27 | GBE1_MDI_N3 | GBE1 | – | A | – |
| – | A | – | GBE0 | GBE0_MDI_P1 | P27 | S28 | DNC | – | – | – | – |
| – | – | – | – | DNC | P28 | S29 | DNC | – | 1.8 V | I | AR29 |
| – | A | – | GBE0 | GBE0_MDI_N0 | P29 | S30 | DNC | – | 1.8 V | I | AL27 |
| – | A | – | GBE0 | GBE0_MDI_P0 | P30 | S31 | GBE1_LINK_ACT# | GBE1 | 3.3 V | O | – |
| M32 | O | 1.8 V | SPI1 | SPI1_CS1 | P31 | S32 | DNC | – | 1.8 V | O | AM26 |
| – | – | 0 V | Power | GND | P32 | S33 | DNC | – | 1.8 V | I | AK26 |
| D24 | I | 3.3 V | SDIO | SD1_WP | P33 | S34 | GND | Power | 0 V | – | – |
| C25 | I/O | 1.8 V / 3.3 V | SDIO | SD1_CMD | P34 | S35 | USB4_P | USB4 | – | I/O | – |
| E23 | I | 3.3 V | SDIO | SD1_CD# | P35 | S36 | USB4_N | USB4 | – | I/O | – |
| G23 | O | 1.8 V / 3.3 V | SDIO | SD1_CLK | P36 | S37 | USB_OTG2_VBUS | USB3 | 5 V | I | H16 |
| B24 | O | 3.3 V | SDIO | SDIO_PWR_EN | P37 | S38 | MCLK_OUT0 | CLK | 1.8 V | O | L29 |
| – | – | 0 V | Power | GND | P38 | S39 | SAI1_TXFS | I2C | 1.8 V | O | N35 |
| A27 | I/O | 1.8 V / 3.3 V | SDIO | SD1_DATA0 | P39 | S40 | SAI1_TXD | I2C | 1.8 V | O | AA33 |
| B26 | I/O | 1.8 V / 3.3 V | SDIO | SD1_DATA1 | P40 | S41 | SAI1_RXD | I2C | 1.8 V | I | AA35 |
| D26 | I/O | 1.8 V / 3.3 V | SDIO | SD1_DATA2 | P41 | S42 | SAI1_TXC | I2C | 1.8 V | O | L35 |
| E25 | I/O | 1.8 V / 3.3 V | SDIO | SD1_DATA3 | P42 | S43 | QSPI_ALERT0# | eSPI | 1.8 V | I | AE33 |
| M34 | O | 1.8 V | SPI1 | SPI1_CS0 | P43 | S44 | DNC | – | – | – | – |
| L33 | O | 1.8 V | SPI1 | SPI1_SCK | P44 | S45 | RFU | – | – | – | – |
| J35 | I | 1.8 V | SPI1 | SPI1_SDI | P45 | S46 | RFU | – | – | – | – |
| K34 | O | 1.8 V | SPI1 | SPI1_SDO | P46 | S47 | GND | Power | 0 V | – | – |
| – | – | 0 V | Power | GND | P47 | S48 | I2C0_SCL_1V8 | I2C | 1.8 V | O | AR25 |
| – | – | – | – | DNC | P48 | S49 | I2C0_SDA_1V8 | I2C | 1.8 V | I/O | AP24 |
| – | – | – | – | DNC | P49 | S50 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P50 | S51 | DNC | – | – | – | – |
| – | – | – | – | DNC | P51 | S52 | DNC | – | – | – | – |
| – | – | – | – | DNC | P52 | S53 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P53 | S54 | DNC | – | – | – | – |

### 3.1.2 SMARC connector X1 (continued)

Table 2: Pinout SMARC connector X1 (continued)

| Ball | Dir. | Level | Group | Signal | Pin | | Signal | Group | Level | Dir. | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AH10 | O | 1.8 V | eSPI | QSPIB_SS0# | P54 | S55 | DNC | – | – | – | – |
| AJ9 | O | 1.8 V | eSPI | QSPIB_SS1# | P55 | S56 | QSPIB_DATA2 | eSPI | 1.8 V | I/O | AJ11 |
| AR11 | O | 1.8 V | eSPI | QSPIB_SCLK | P56 | S57 | QSPIB_DATA3 | eSPI | 1.8 V | I/O | AM8 |
| AL9 | I/O | 1.8 V | eSPI | QSPIB_DATA1 | P57 | S58 | QSPI_RESET# | eSPI | 1.8 V | O | R35 |
| AM10 | I/O | 1.8 V | eSPI | QSPIB_DATA0 | P58 | S59 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P59 | S60 | DNC | – | – | – | – |
| D18 | I/O | – | USB0 | USB_OTG1_DP | P60 | S61 | GND | Power | 0 V | – | – |
| E19 | I/O | – | USB0 | USB_OTG1_DN | P61 | S62 | USB3_SS_TX_P | USB3_SS | 1.0 V | O | – |
| G15 | I/O | 3.3 V | USB0 | USB_OTG1_OC | P62 | S63 | USB3_SS_TX_N | USB3_SS | 1.0 V | O | – |
| H18 | I | 5 V | USB0 | USB_OTG1_VBUS | P63 | S64 | GND | Power | 0 V | – | – |
| G17 | I | 1.8 V[1] | USB0 | USB_OTG1_ID | P64 | S65 | USB3_SS_RX_P | USB3_SS | 1.0 V | I | – |
| – | I/O | – | USB1 | USB1_P | P65 | S66 | USB3_SS_RX_N | USB3_SS | 1.0 V | I | – |
| – | I/O | – | USB1 | USB1_N | P66 | S67 | GND | Power | 0 V | – | – |
| – | I/O | 3.3 V | USB1 | USB1_EN_OC# | P67 | S68 | USB3_P | USB3 | – | I/O | – |
| – | – | 0 V | Power | GND | P68 | S69 | USB3_N | USB3 | – | I/O | – |
| – | I/O | – | USB2 | USB2_P | P69 | S70 | GND | Power | 0 V | – | – |
| – | I/O | – | USB2 | USB2_N | P70 | S71 | USB2_SS_TX_P | USB2_SS | 1.0 V | O | – |
| – | I/O | 3.3 V | USB2 | USB2_EN_OC# | P71 | S72 | USB2_SS_TX_N | USB2_SS | 1.0 V | O | – |
| – | – | – | – | RFU | P72 | S73 | GND | Power | 0 V | – | – |
| – | – | – | – | RFU | P73 | S74 | USB2_SS_RX_P | USB2_SS | 1.0 V | I | – |
| – | I/O | 3.3 V | USB3 | USB3_EN_OC# | P74 | S75 | USB2_SS_RX_N | USB2_SS | 1.0 V | I | – |
| | | | | | Key | | | | | | |
| H10 | O | 3.3 V | PCIE | PCIE_PERST# | P75 | S76 | DNC | – | – | – | – |
| – | I/O | 3.3 V | USB4 | USB4_EN_OC# | P76 | S77 | DNC | – | – | – | – |
| – | – | – | – | RFU | P77 | S78 | DNC | – | – | – | – |
| – | – | – | – | RFU | P78 | S79 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P79 | S80 | GND | Power | 0 V | – | – |
| – | – | – | – | DNC | P80 | S81 | DNC | – | – | – | – |
| – | – | – | – | DNC | P81 | S82 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P82 | S83 | GND | Power | 0 V | – | – |
| – | O | 1.0 V | PCIE | PCIE_REFCLK_P | P83 | S84 | DNC | – | – | – | – |
| – | O | 1.0 V | PCIE | PCIE_REFCLK_N | P84 | S85 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P85 | S86 | GND | Power | 0 V | – | – |
| A13 | I | 1.0 V | PCIE | PCIE_RX_P | P86 | S87 | DNC | – | – | – | – |
| B12 | I | 1.0 V | PCIE | PCIE_RX_N | P87 | S88 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P88 | S89 | GND | Power | 0 V | – | – |
| B10 | O | 1.0 V | PCIE | PCIE_TX_P | P89 | S90 | DNC | – | – | – | – |
| A9 | O | 1.0 V | PCIE | PCIE_TX_N | P90 | S91 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P91 | S92 | GND | Power | 0 V | – | – |
| – | – | – | – | DNC | P92 | S93 | DP0_LANE0_P | DP | 1.2 V | O | – |
| – | – | – | – | DNC | P93 | S94 | DP0_LANE0_N | DP | 1.2 V | O | – |
| – | – | 0 V | Power | GND | P94 | S95 | DP0_AUX_SEL | DP | 0 V | – | – |
| – | – | – | – | DNC | P95 | S96 | DP0_LANE1_P | DP | 1.2 V | O | – |
| – | – | – | – | DNC | P96 | S97 | DP0_LANE1_N | DP | 1.2 V | O | – |
| – | – | 0 V | Power | GND | P97 | S98 | DP0_HPD | DP | 5 V | I | – |
| – | – | – | – | DNC | P98 | S99 | DNC | – | – | – | – |
| – | – | – | – | DNC | P99 | S100 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P100 | S101 | GND | Power | – | – | – |
| – | – | – | – | DNC | P101 | S102 | DNC | – | – | – | – |
| – | – | – | – | DNC | P102 | S103 | DNC | – | – | – | – |
| – | – | 0 V | Power | GND | P103 | S104 | USB_OTG2_ID | USB3 | 3.3 V | I | F16 |
| – | – | – | – | DNC | P104 | S105 | DP0_AUX_P | DP | 1.2 V | I/O | – |
| – | – | – | – | DNC | P105 | S106 | DP0_AUX_N | DP | 1.2 V | I/O | – |

[1] Type according to SMARC standard CMOS 3.3V. Therefore level conversion on base board necessary.

### 3.1.2 SMARC connector X1 (continued)

Table 2: Pinout SMARC connector X1 (continued)

| Ball | Dir. | Level | Group | Signal | Pin | | Signal | Group | Level | Dir. | Ball |
|---|---|---|---|---|---|---|---|---|---|---|---|
| – | – | – | – | DNC | P106 | S107 | LCD1_BKLT_EN | LVDS / DSI | 1.8 V | O | P28 |
| – | – | – | – | DNC | P107 | S108 | MIPI_DSI1_CLKP | LVDS / DSI | 1.8 V | O | AP16 |
| P30 | I/O | 1.8 V | GPIO | GPIO1_IO04 | P108 | S109 | MIPI_DSI1_CLKN | LVDS / DSI | 1.8 V | O | AM16 |
| P34 | I/O | 1.8 V | GPIO | GPIO1_IO05 | P109 | S110 | GND | Power | 0 V | – | – |
| R31 | I/O | 1.8 V | GPIO | GPIO1_IO06 | P110 | S111 | MIPI_DSI1_DP0 | LVDS / DSI | 1.8 V | O | AR15 |
| R33 | I/O | 1.8 V | GPIO | GPIO1_IO08 | P111 | S112 | MIPI_DSI1_DN0 | LVDS / DSI | 1.8 V | O | AN15 |
| V34 | I/O | 1.8 V | GPIO | GPIO1_IO13 | P112 | S113 | DNC | – | – | – | – |
| L31 | I/O | 1.8 V | GPIO | GPIO0_IO22 | P113 | S114 | MIPI_DSI1_DP1 | LVDS / DSI | 1.8 V | O | AR17 |
| H34 | I/O | 1.8 V | GPIO | GPIO0_IO21 | P114 | S115 | MIPI_DSI1_DN1 | LVDS / DSI | 1.8 V | O | AN17 |
| U35 | I/O | 1.8 V | GPIO | GPIO1_IO10 | P115 | S116 | LCD1_VDD_EN | LVDS / DSI | 1.8 V | O | P32 |
| U33 | I/O | 1.8 V | GPIO | GPIO1_IO09 | P116 | S117 | MIPI_DSI1_DP2 | LVDS / DSI | 1.8 V | O | AP14 |
| V32 | I/O | 1.8 V | GPIO | GPIO1_IO12 | P117 | S118 | MIPI_DSI1_DN2 | LVDS / DSI | 1.8 V | O | AM14 |
| V30 | I/O | 1.8 V | GPIO | GPIO1_IO11 | P118 | S119 | GND | Power | 0 V | – | – |
| – | – | – | – | DNC | P119 | S120 | MIPI_DSI1_DP3 | LVDS / DSI | 1.8 V | O | AP18 |
| – | – | 0 V | Power | GND | P120 | S121 | MIPI_DSI1_DN3 | LVDS / DSI | 1.8 V | O | AM18 |
| AJ35 | O | 1.8 V | I2C | PMIC_I2C_SCL | P121 | S122 | MIPI_DSI1_PWM | LVDS / DSI | 1.8 V | O | AD30 |
| AH32 | I/O | 1.8 V | I2C | PMIC_I2C_SDA | P122 | S123 | RFU | – | – | – | – |
| – | I | 1.8 V | BOOT | BOOT_SEL0# | P123 | S124 | GND | Power | 0 V | – | – |
| – | I | 1.8 V | BOOT | BOOT_SEL1# | P124 | S125 | MIPI_DSI0_DP0 | LVDS / DSI | 1.8 V | O | AK22 |
| – | I | 1.8 V | BOOT | BOOT_SEL2# | P125 | S126 | MIPI_DSI0_DN0 | LVDS / DSI | 1.8 V | O | AJ21 |
| – | O | 1.8 V | CONFIG | RESET_OUT# | P126 | S127 | LCD0_BKLT_EN | LVDS / DSI | 1.8 V | O | N31 |
| – | I | 1.8 V | CONFIG | RESET_IN# | P127 | S128 | MIPI_DSI0_DP1 | LVDS / DSI | 1.8 V | O | AK18 |
| AH28 | I | 1.8 V | CONFIG | IMX_ONOFF | P128 | S129 | MIPI_DSI0_DN1 | LVDS / DSI | 1.8 V | O | AJ17 |
| AA29 | O | 1.8 V | SER | UART0_TX | P129 | S130 | GND | Power | 0 V | – | – |
| AB32 | I | 1.8 V | SER | UART0_RX | P130 | S131 | MIPI_DSI0_DP2 | LVDS / DSI | 1.8 V | O | AK24 |
| Y34 | O | 1.8 V | SER | UART0_RTS# | P131 | S132 | MIPI_DSI0_DN2 | LVDS / DSI | 1.8 V | O | AJ23 |
| Y32 | I | 1.8 V | SER | UART0_CTS# | P132 | S133 | LCD0_VDD_EN | LVDS / DSI | 1.8 V | O | R29 |
| – | – | 0 V | Power | GND | P133 | S134 | MIPI_DSI0_CLKP | LVDS / DSI | 1.8 V | O | AK20 |
| AH30 | O | 1.8 V | SER | SCU_UART_TX | P134 | S135 | MIPI_DSI0_CLKN | LVDS / DSI | 1.8 V | O | AJ19 |
| AF28 | I | 1.8 V | SER | SCU_UART_RX | P135 | S136 | GND | Power | 0 V | – | – |
| – | – | – | – | DNC | P136 | S137 | MIPI_DSI0_DP3 | LVDS / DSI | 1.8 V | O | AK16 |
| – | – | – | – | DNC | P137 | S138 | MIPI_DSI0_DN3 | LVDS / DSI | 1.8 V | O | AJ15 |
| – | – | – | – | DNC | P138 | S139 | MIPI_DSI0_I2C0_SCL | I2C | 1.8 V | O | AC31 |
| – | – | – | – | DNC | P139 | S140 | MIPI_DSI0_I2C0_SDA | I2C | 1.8 V | I/O | AB28 |
| – | – | – | – | DNC | P140 | S141 | MIPI_DSI0_PWM | LVDS / DSI | 1.8 V | O | AD32 |
| – | – | – | – | DNC | P141 | S142 | RFU | – | – | – | – |
| – | – | 0 V | Power | GND | P142 | S143 | GND | Power | 0 V | – | – |
| AC35 | O | 1.8 V | CAN | CAN1_TX | P143 | S144 | DNC | – | – | – | – |
| AD34 | I | 1.8 V | CAN | CAN1_RX | P144 | S145 | WDT_TIME_OUT# (SCU_WDOG_OUT) | CONFIG | 1.8 V | O | AD28 |
| AA31 | O | 1.8 V | CAN | CAN2_TX | P145 | S146 | PCIE_WAKE# | PCIE | 3.3 V | I | A11 |
| AB34 | I | 1.8 V | CAN | CAN2_RX | P146 | S147 | VDD_RTC | POWER | 3.0 V | P | – |
| – | P | – | Power | VDD_IN | P147 | S148 | LID# | CONFIG | 1.8 V | I | E35 |
| – | P | – | Power | VDD_IN | P148 | S149 | SLEEP# | CONFIG | 1.8 V | I | H32 |
| – | P | – | Power | VDD_IN | P149 | S150 | VIN_PWR_BAD# | CONFIG | VDD_IN | I | – |
| – | P | – | Power | VDD_IN | P150 | S151 | CHARGING# | CONFIG | 1.8 V | I | F34 |
| – | P | – | Power | VDD_IN | P151 | S152 | CHARGER_PRSNT# (CHG_PRSNT#) | CONFIG | 1.8 V | I | G33 |
| – | P | – | Power | VDD_IN | P152 | S153 | CARRIER_STBY# | CONFIG | 1.8 V | O | AG29 |
| – | P | – | Power | VDD_IN | P153 | S154 | CARRIER_PWR_ON | CONFIG | 1.8 V | O | – |
| – | P | – | Power | VDD_IN | P154 | S155 | FORCE_RECOV# | BOOT | 1.8 V | I | – |
| – | P | – | Power | VDD_IN | P155 | S156 | BATLOW# | CONFIG | 1.8 V | I | J31 |
| – | P | – | Power | VDD_IN | P156 | S157 | TEST# | CONFIG | 1.8 V | – | – |
| – | – | – | – | – | – | S158 | GND | Power | 0 V | – | – |

The pins assignment listed in Table 2 refers to the corresponding BSP provided by TQ-Systems GmbH.
For information regarding I/O pins in Table 2 refers to the i.MX 8X Data Sheet (1).

## 3.2 System components

### 3.2.1 i.MX 8X CPU

#### 3.2.1.1 i.MX 8X derivatives

Depending on the TQMa8XxS version, one of the following i.MX 8X derivatives is assembled.

Table 3: i.MX 8X derivatives

| TQMa8XxS variant | CPU derivative | Cortex®-A35 clock | Cortex®-M4 clock | $T_J$, temperature range |
|---|---|---|---|---|
| TQMa8XDS-xx | i.MX 8DualX | 1.2 GHz | 264 MHz | –40 °C to +125 °C |
| TQMa8XDPS-xx | i.MX 8DualXPlus | 1.2 GHz | 264 MHz | –40 °C to +125 °C |
| TQMa8XQPS-xx | i.MX 8QuadXPlus | 1.2 GHz | 264 MHz | –40 °C to +125 °C |

#### 3.2.1.2 i.MX 8X errata

| Attention: Malfunction | |
|---|---|
|  | Please take note of the current i.MX 8X errata (3). |

### 3.2.1.3 Boot modes

After the release of RESET_IN# / IMX_POR# the system controller (SCU) boots from the internal ROM. Depending on the OPT fuses (eFuse) and the boot mode settings of the system controller the system boots from the selected boot source. The following interfaces are available as boot source:

- eMMC
- QSPI-NOR flash
- SD card

The SMARC standard requires, depending on the selected boot mode, a defined wiring of the SMARC connector pins BOOT_SEL[2:0]. These are converted with a CPLD to the boot mode pins BOOT_MODE[3:0].

The FORCE_RECOV# signal is used to switch to the "Force Recovery" mode or the "Serial Downloader", see (1) and (6).

More information about boot interfaces and its configuration is to be taken from the i.MX 8X Data Sheet (1) and the i.MX 8X Reference Manual (2). Alternatively, an image can be loaded into the internal RAM via serial downloader.

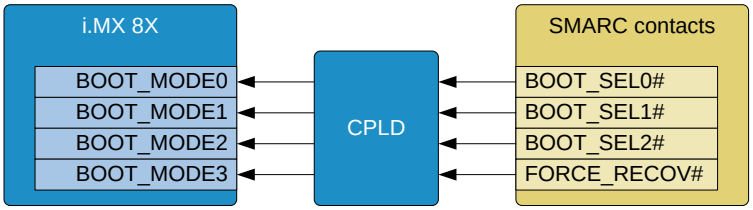


Figure 3: Block diagram Boot-Mode

The following boot media are provided according to the SMARC standard:

Table 4: Boot sources

| i.MX 8X BOOT_MODE[3:0] | FORCE_RECOV# | BOOT_SEL[2:0]# [2] | Boot Source |
|---|---|---|---|
| 0000 | 1 | 101 | Remote / Internal eFuses. Defined as Boot from eFuses, since the i.MX 8X does not define a remote mode. |
| 0001 | 0 | xxx | Recovery-Mode / Serial-Downloader |
| 0010 | 1 | 110 | eMMC |
| 0011 | 1 | 001 | SD card |
| 0110 | 1 | 100 | QSPI NOR flash |

| Note: Field software updates | |
|---|---|
|  | When designing a carrier board, it is recommended to have a redundant update concept for field software updates. |

2: Floating inputs are taken as "1" due to the pull-up on the TQMa8XxS.

### 3.2.2 Memory

#### 3.2.2.1 LPDDR4 SDRAM

LPDDR4 SDRAM with an effective memory bandwidth of 32 bits is used on the TQMa8XxS. The fifth byte lane of the i.MX 8X CPU is unused.

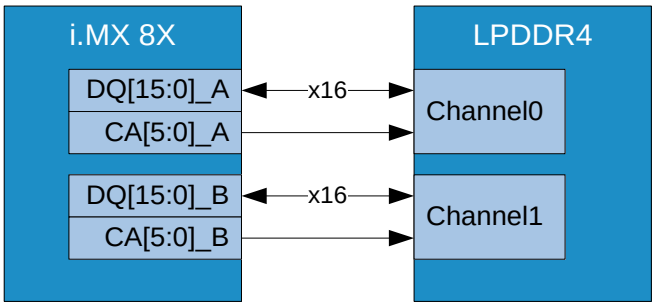


Figure 4: Block diagram LPDDR4

The interface timing corresponds to the JEDEC standard LPDDR4-2400 with a max. clock rate of 1200 MHz.
The use of LPDDR4 memory eliminates the ECC feature of the RAM controller. However, special ECC memories can be used that protect the memory content via ECC independently of the controller. Through correspondingly fewer refresh cycles of the cells, the power consumption is thereby reduced or the memory is used energy neutral (compared to use without ECC) at higher temperatures.

The IO voltage of the LPDDR4 is 1.1 V.

The standard memory size of the TQMa8XxS is 2 GByte. Variants with 1 GByte and 4 GByte are available.

| Attention: Malfunction | |
|---|---|
|  | The TQMa8XxS uses a specially developed RAM timing. Each memory expansion level required its own LPDDR4 configuration. |

The standard memory for TQMa8XxS is Samsungs K4F6E3S4HM-GFCL03V (LPDDR4-1866 2048Mx32).

#### 3.2.2.2 eMMC NAND flash

An eMMC is available on the TQMa8XxS as non-volatile memory for programs and data (e.g. bootloader, operating system, application). The following figure shows the interface of the eMMC to the i.MX 8X:

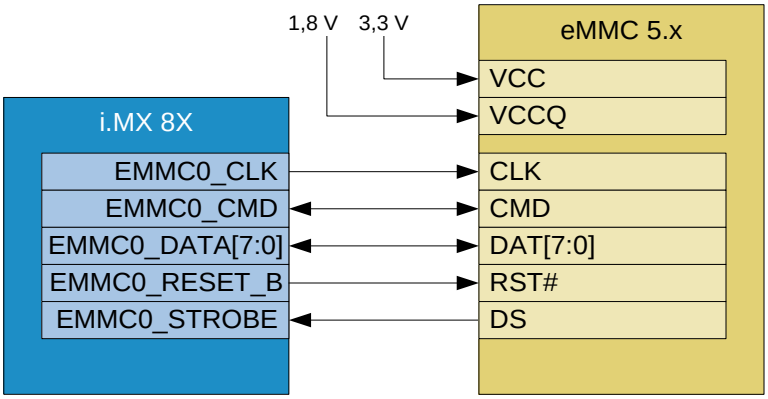


Figure 5: Block diagram eMMC

The i.MX 8X supports MMC card transmission modes up to the current eMMC standard v5.
The I/O voltage is 1.8 V to support the maximum clock rate of 200 MHz. This allows a data rate of up to 400 Mbyte/s in DDR mode (HS400).

The eMMC can be used as boot medium. The boot configuration is described in 3.2.1.3.

Additional series terminations are inserted in the data and clock signals to influence the driver strength starting from the eMMC.

The standard eMMC size is 8 GByte. Variants with 4 GByte, 16 GByte, 32 GByte, 64 GByte and without eMMc are available. The standard eMMC ist SanDisks SDINBDG4-8G-T (8 GByte/5.1/SLC).

#### 3.2.2.3 QSPI NOR flash

The i.MX 8X provides two QSPI interfaces, which can be combined to an Octal-SPI or Twin-Quad-SPI on the TQMa8XxS.
In addition, both interfaces feature a data strobe signal with a maximum clock rate of up to 200 MHz, which however, is only used with QSPI_A. The second QSPI interface is also available on SMARC pins.

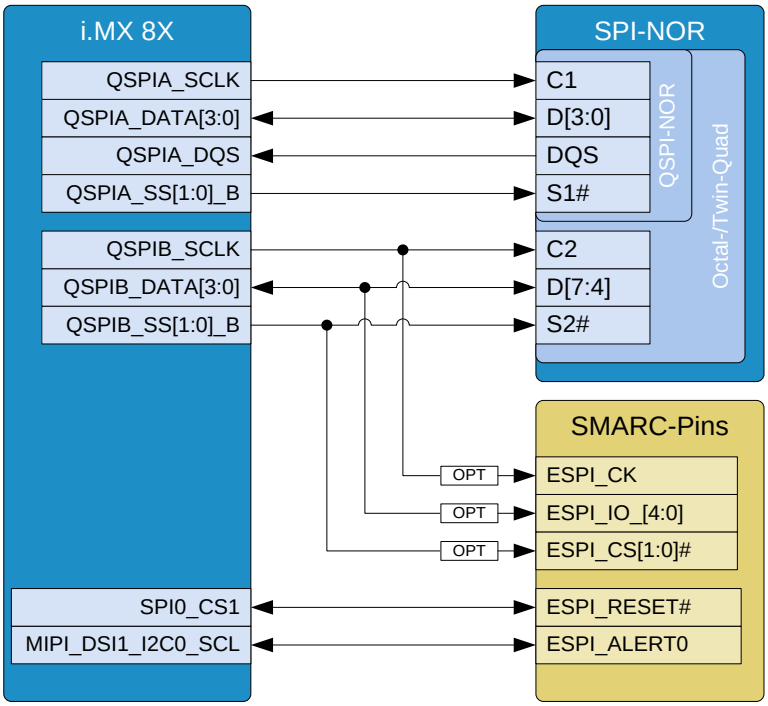


Figure 6: Block diagram QSPI

Different types of serial NOR-Flashes can be used on the TQMa8XxS, which use one or both QSPI interfaces depending on the type. The following types can be used:

- QSPI Flash - Simple NOR-Flashes use only one of the two QSPI interfaces. The remaining balls of the second interface are not connected internally and can be used via the module connectors on the mainboard.
- Octal-SPI / Twin-Quad-SPI - These NOR Flashes represent a dual die Flash, which uses additional pins for the second QSPI interface compared to the single NOR Flash. The latter cannot be used on the mainboard in this case. All signals of the QSPIB interface are to be treated as NC in this case.
- Hyperflash / Xccela Flash - The modern serial Flash devices are connected similar to an Octal-SPI / Twin-Quad-SPI, but have a DQS signal (RX clock) to increase the transfer rate. Thus, up to 400 MB/s can be achieved. Also in this case, the QSPIB interface cannot be used on the mainboard.

#### 3.2.2.4 EEPROM

For non-volatile storage of e.g. module characteristics or customer specific parameters, a serial EEPROM is optionally available, which is connected to the I2C0 bus of the i.MX 8X via a level translator.
The write protection (WP) of the EEPROM is not available.

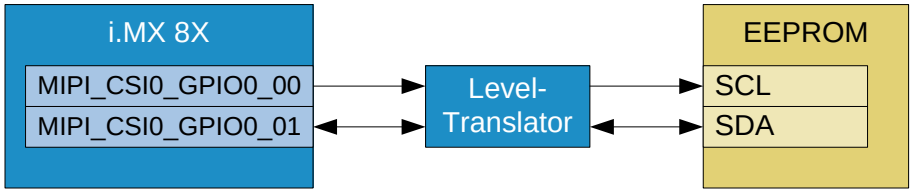


Figure 7: Block diagram 24LC64T EEPROM

The following table shows details of the EEPROM.

Table 5: 24LC64T EEPROM

| Manufacturer | Part number | Size | Temperature range |
|---|---|---|---|
| Microchip | 24LC64T-I/MC MCH | 64 Kbit | –45 °C to +85 °C |

- The EEPROM has I²C address `0x50 / 101 0000b`

#### 3.2.2.5 SE97B EEPROM with temperature sensor

A serial EEPROM including temperature sensor, controlled by the I2C1 bus, is assembled.
The lower 128 bytes (address 00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. The upper 128 bytes (address 80h to FFh) are not write protected and can be used for general purpose data storage.
The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa8XxS.
The following table shows details of the SE97B EEPROM.

Table 6: SE97BT EEPROM

| Manufacturer | Part number | Size | Temperature range |
|---|---|---|---|
| NXP | SE97B,547 | 2 × 128 bytes | –45 °C to +85 °C |

- The device has the following I²C addresses:
  - EEPROM (normal): `0x53 / 101 0011b`
  - EEPROM (Protection Command): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

The EEPROM with temperature sensor (D7) is assembled on the bottom side of the TQMa8XxS, see Figure 30.
The temperature sensor is connected to the I2C0 bus of the processor via a level translator.
The overtemperature output of the sensor is connected to the i.MX 8X ball QSPI0A_SS1#.

The following table shows details of the SE97B temperature sensor.

Table 7: SE97B temperature sensor

| Manufacturer | Part number | Resolution | Accuracy | Temperature range |
|---|---|---|---|---|
| NXP | SE97B,547 | 11 bits | Max. ±3 °C | –40 °C to +125 °C |

### 3.2.3 RTC

In addition to the i.MX 8X-internal RTC, the TQMa8XxS provides a discrete RTC PCF85063 as assembly option.

Table 8: RTC variants

| TQMa8XxS variant | Function |
|---|---|
| TQMa8XxS without discrete RTC | VDD_RTC supplies via VSNVS controller of the PMIC the SNVS domain of the i.MX 8X |
| TQMa8XxS with discrete RTC (standard) | VDD_RTC supplies external RTC PCF85063.<br>SNVS domain of i.MX 8X only supplied if module supply 3.3 V available. |

| Note: Power supply for i.MX 8X-internal RTC | |
|---|---|
|  | The i.MX 8X-internal RTC can always be used in ON mode, but resets itself at variants with equipped PCF85063 when the module supply (3.3 V) fails, since the SNVS domain of the i.MX 8X is then no longer supplied. |

#### 3.2.3.1 i.MX 8X internal RTC

The i.MX 8X has an internal RTC which has to be powered by the power domain (SNVS).

The accuracy of the RTC is primarily determined by the characteristics of the quartz used. The type FC-135 used on the TQMa8XxS has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. −0.04 x $10^{-6}$ / °$C^2$)

The RTC power domain SNVS of the CPU is supplied by the PMIC through the internal controller VSNVS. This is supplied either from the module input voltage V_VDD_IN or from V_VDD_RTC at the PMIC pin LICELL. LICELL supports simple Coin Cells and SuperCaps. Charging methods and electrical properties of the LICELL pin can be found in the PMIC data sheet (4). Note that the typical charging current is only 60 µA.

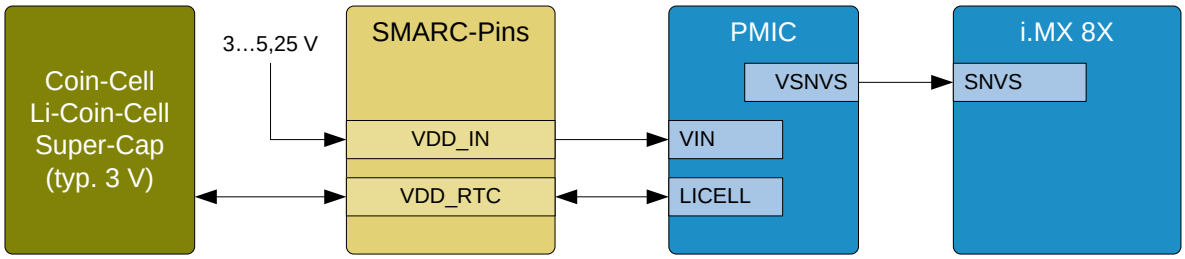


Figure 8: Block diagram i.MX 8X internal RTC supply (TQMa8XxS without discrete RTC)

| Note: SNVS domain supply | |
|---|---|
|  | For module variants with equipped external RTC, the LICELL pin of the PMIC is not connected to VDD_RTC. The SNVS domain of the i.MX 8X is therefore only supplied in on-mode. |

The following table shows the current consumption at the LICELL pin for TQMa8XxS variants without discrete RTC:

Table 9: Current consumption LICELL with i.MX 8X internal RTC

| Voltage LICELL | Current consumption LICELL | Remark |
|---|---|---|
| 3.2 V | typ. 4,125 µA | VCC5V = typ. 0 V<br>$T_{amb}$ = +25 °C |
| 3.0 V | typ. 4,026 µA | |
| 2.4 V | typ. 3,818 µA | |

It is recommended to use the RTC PCF85063 due to the high current consumption of the SNVS domain, see section 3.2.3.

#### 3.2.3.2 RTC PCF85063

In addition to the i.MX 8X-internal RTC, TQMa8XxS variants with discrete RTC at I2C0 are available, see Table 8.
The accuracy of the RTC is primarily determined by the characteristics of the quartz used. The type CM7V used on the TQMa8XxS has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. −0.04 x $10^{-6}$ / °C$^2$)
The RTC PCF85063 is only supplied directly by LICELL when the PMIC is switched off or the module supply is switched off. During runtime the PMIC takes over the supply via the module supply with 3.3 V.

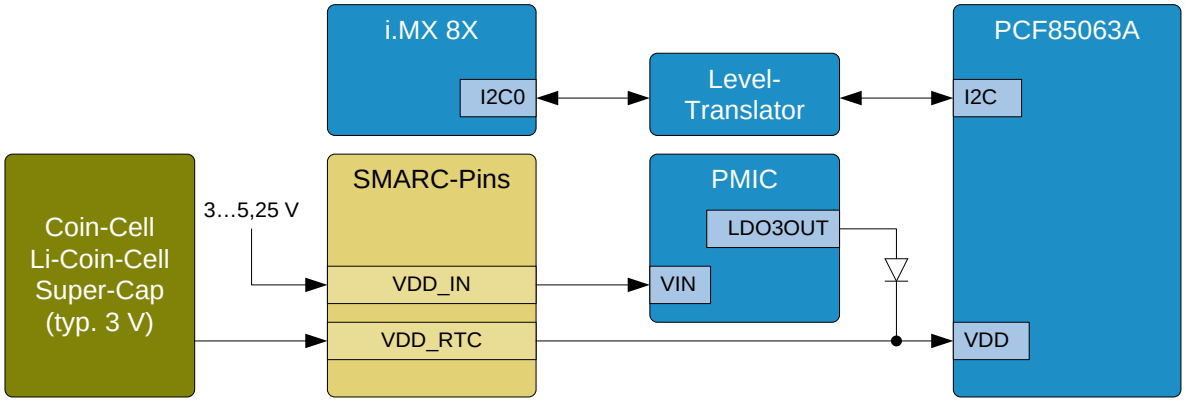


Figure 9: Block diagram RTC supply (TQMa8XxS with discrete RTC)

| Note: SNVS domain supply | |
|---|---|
| | The SNVS domain is not buffered by LICELL for TQMa8XxS variants with assembled discrete RTC.<br>The SNVS functions of the i.MX 8X can therefore only be used when the TQMa8XxS supply is present.<br>The charging function of the PMIC at pin LICELL is not available for TQMa8XxS variants with assembled discrete RTC. |

The following table shows the current consumption at the LICELL pin for TQMa8XxS variants with discrete RTC:

Table 10: Current consumption V_VDD_RTC with discrete RTC

| Voltage LICELL | Current consumption LICELL | Remark |
|---|---|---|
| 3.25 V | typ. 0,173 µA; max. 0,450 µA | V_3V3_IN = typ. 0 V<br>$T_{amb}$ = +25 °C |
| 3.00 V | typ. 0,171 µA; max. 0,450 µA | |
| 2.40 V | typ. 0,164 µA ; max. 0,450 µA | |

➢ The RTC PCF85063 has I$^2$C address `0x51 / 101 0001b`

The interrupt of the RTC (RTC_INT#) is routed to the i.MX 8X pin MIPI_DSI1_GPIO0_01.

## 3.3 TQMa8XxS interfaces

To ensure flexible use of all i.MX 8X functions, all i.MX 8X pins or interfaces are routed to the module headers where possible and are thus available on the base board. Besides some pins that are not available due to module-internal functions like LPDDR4 and for technical reasons, there are minor restrictions in the availability of i.MX 8X pins, which are shown in the following table (only functional pins mentioned):

| Interface i.MX 8X | Quantity | Chapter | Note |
|---|---|---|---|
| EMMC0 | 1 | 3.2.2.2 | Use for optional e-MMC, 8 bit |
| QSPI0A | 1 | 3.2.2.3 | Use for optional SPI-NOR flash |
| DDR | 1 | 3.2.2.1 | Use for LPDDR4, 32 bit |

### 3.3.1 Gigbit Ethernet

Two Gigabit Ethernet interfaces (GBE0, GBE1) are provided at the SMARC connector of the TQMa8XxS.
These are implemented with two independent PHYs. The LED signals are defined as 3.3 V tolerant open-drain outputs for a current of at least 24 mA each.

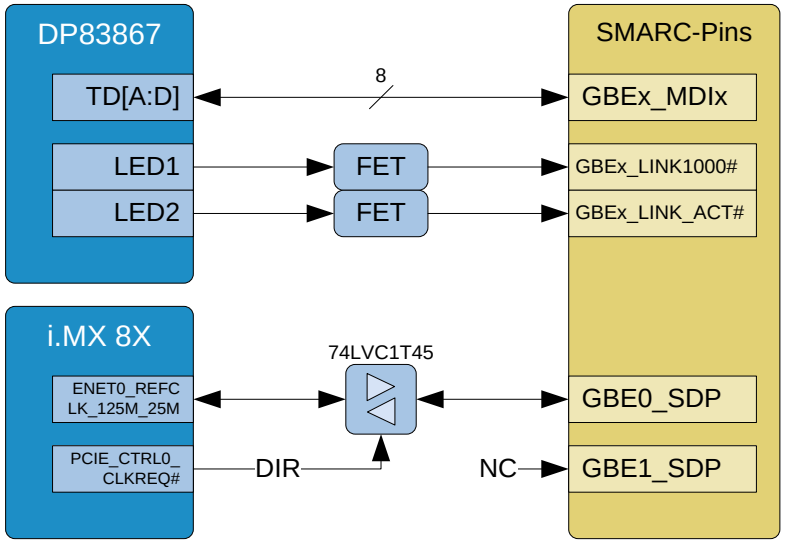


Figure 10: Block diagram Ethernet

Only one of the IEEE 1588 signals GBE[1:0]_SDP is realized. Both ENET controllers of the i.MX 8X have one trigger signal (PPS) each, but this signal is only multiplexable at the CPU ball F28. For the SDP signal, a bidirectional level converter from 1.8 V to 3.3 V is required. The SN74LVC1T45 from TI is used for this purpose. Since the data direction is application dependent, the signal of the CPU ball PCIE_CTRL0_CLKREQ# configured as GPIO is used for direction control.

The GPIO pins of the PHY have internal pull-down resistors for strap configuration, which are switched off after power-up. Thus, the data direction of the SDP signals is defined as input, but this affects the strap configuration. Since the input level of the SDP signals is unknown, the corresponding strap configuration is undefined. For this reason it is mandatory that the corresponding configuration registers are set by software. By default, the SDP signals are defined as input.

According to the SMARC standard, the Ethernet PHYs are part of the SMARC module, so that only the magnatics are implemented on the carrier. Since the single-gigabit PHY DP83867ISRGZ has already proven itself several times, it is used on the basis of the MBa8Xx. The connection to the CPU is done via RGMII.

Since the second PHY is optional, the provision of an IEEE 1588 trigger signal is only done at the SMARC GBE0_SDP pin, which is connected to the CPU ball ENET0_REFCLK_125M_25M (see chapter 3.1.3.1).

The control of the activity LEDs is done by the LED-GPIOs of the respective PHYs.

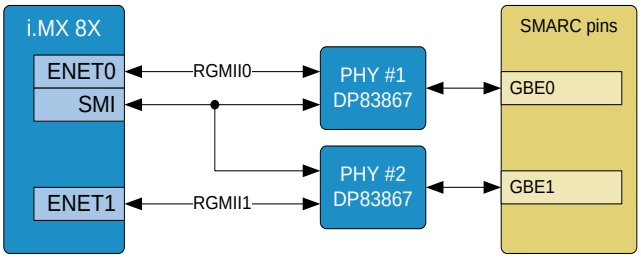


Figure 11: Block diagram Ethernet PHYs

### 3.3.2 USB

The SMARC standard defines a total of six USB ports, which are wired as shown in the following table. USB2 and USB3 can be used for USB 3.0, so they have the additional differential superspeed signals (TX/RX).

Both OTG ports of the i.MX 8X can be used for the serial downloader.

Furthermore, due to the USB architecture in the i.MX 8X, USB OTG2 is used together with USB SS3 for USB 3.0 functionality.

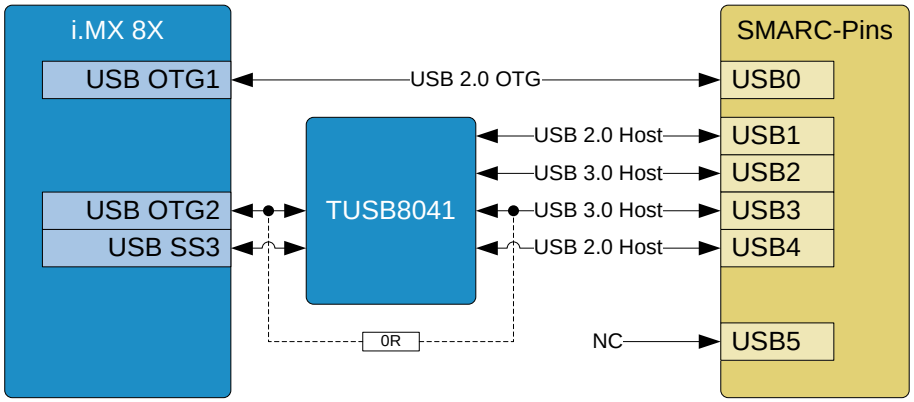


Figure 12: Block diagram USB interfaces

At port USB0 the USB OTG1 port of the CPU is connected, because the SMARC standard defines the force recovery function at this port. For the signal USB_OTG1_ID (USB0_OTG_ID / P64) a level conversion from 3.3 V to 1.8 V has to be provided on the base board, since the CPU operates at this pin with 1.8 V only.

The second USB OTG port (OTG2) of the i.MX 8X is used for the USB hub. Since the USB hub is a placement option, OTG2 can be applied directly to USB3 of the SMARC pins via 0R bridges. USB3 was chosen because the signals OTG2_VBUS and OTG2_ID are also available there.

The connection of the control signals of USB0 and USB3 is shown in figure below. The signal USB0_EN_OC# is realized by means of an open-drain buffer and connected to the corresponding pins of the USB-OTG1 port of the i.MX 8X.

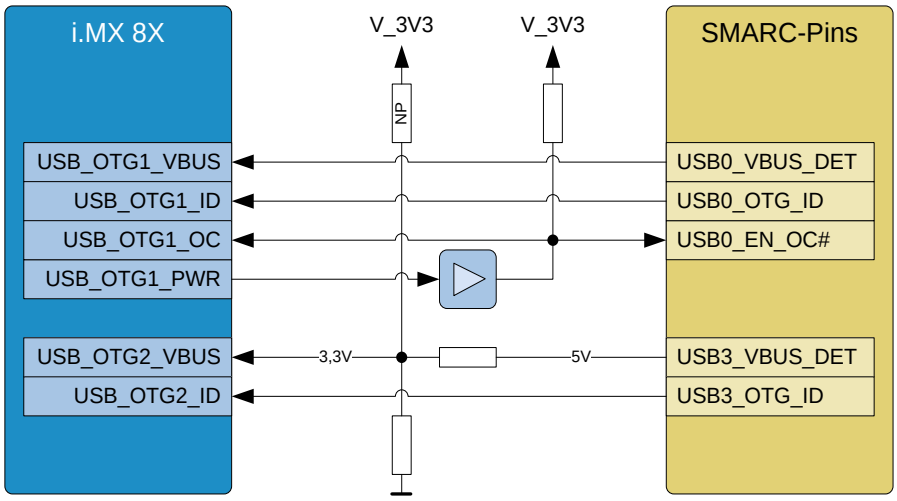


Figure 13: Connection of control signals USB0 and USB3

Table 11: USB ports

| SMARC port | Provided by | Remark |
|---|---|---|
| USB0 (2.0 OTG) | i.MX 8X OTG1 | Force Recovery Function (USB Serial Downloader) |
| USB1 (2.0) | USB-Hub Port 1 | – |
| USB2 (3.0) | USB-Hub Port 2 | Usable as host only |
| USB3 (3.0) | USB-Hub Port 3 | Can only be used as host; optional i.MX 8X OTG2 (USB 3.0 not provided) |
| USB4 (2.0) | USB-Hub Port 4 | – |
| USB5 (2.0) | Not used | – |

Apart from USB5, all USB interfaces of the SMARC standard are provided. The TUSB8041 USB hub from TI is used for this, which is an assembly option and is connected to the OTG2 port of the i.MX 8X. If the hub is not populated, OTG2 can optionally be provided on the SMARC pins.

The SMARC signals USB[5:1]_EN_OC# are bidirectional multifunction signals. The hub has separate pins for these functions. To bring them together, two small CPLDs with specific programming are provided on the module. The pull-up resistors to be placed on the module according to the SMARC standard are integrated in the CPLDs (10 kΩ).

For the signal USB3_EN_OC# a placement option is provided as described in the following table:

Table 12: Assembly option USB3_EN_OC#

| Signal | Option with USB hub | Option without USB hub |
|---|---|---|
| USB3_EN_OC# | Connection via CPLD to USB hub pins PWRCTL3 and OVERCUR3#. | Connection via CPLD to i.MX 8X pins OTG2_PWR and OTG2_OC |

The USB[4:1]_EN_OC# signals are provided by CPLDs. Since the CPU ball USB_OTG2_VBUS has only 3.3 V instead of 5 V level, a voltage divider is used for this signal.

| Attention: USB3 | |
|---|---|
|  | Since the USB hub does not support Dual-Role, the USB3 port can only be used as host! Users of the USB 3.0 OTG connector of the MB-SMARC-2 mainboard have to pay attention to this. |

### 3.3.3 LVDS / DSI / Display-Port

In addition to LVDS, the SMARC standard also specifies HDMI or DisplayPort. The Display Port signals are provided by MIPI_DSI0 via DSI-to-DP bridge. If DisplayPort is not used, both MIPI-DSI interfaces of the CPU can be connected to the SMARC LVDS/DSI pins.

The MIPI_DSI0 data and clock signals are connected to the SMARC pins with 0-Ω bridges. When equipping the DisplayPort bridge to use the DisplayPort, these 0-Ω bridges are not assembled. Thus, these DSI0 signals are then no longer available at the SMARC pins.

The MIPI_DSI0_I2C0 interface of the CPU is used to provide the I2C_LCD signals. The enable signals for VDD and backlight are multiplexed as GPIO signals to the SPI2 pins of the CPU. The backlight PWM signals are multiplexed to the GPIO0_00 pins of the DSI interfaces.

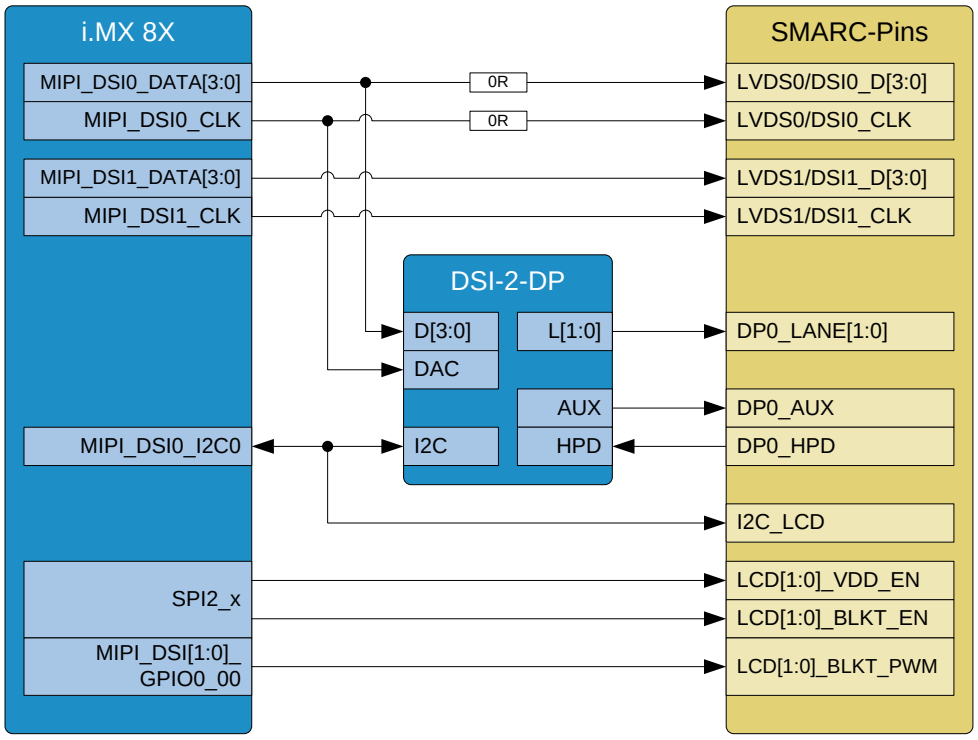


Figure 14: Block diagram LVDS / DSI / Display-Port

Due to the use of DisplayPort 1.1a, only two of the four data lanes provided in the SMARC standard (DP0_LANE0 & DP0_LANE1) are used. Lane 2 and 3 remain unconnected.

The LVDS and DSI signals are also routed out on SMARC pins, but can only be used if DisplayPort is not used.

### 3.3.4 Camera Serial Interface (CSI)

The CSI of the i.MX 8X is directly connected to the SMARC connector, including the I²C bus provided for this purpose.

Since only two lanes are available at port CSI0, CSI1 is used instead. At CSI1 all four data lanes of the CPU are made available.

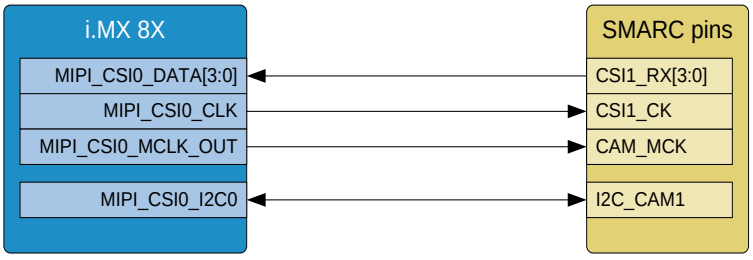


Figure 15: Block diagram CSI

The parallel CSI interface of the i.MX 8X is optionally provided at the CSI0 pins (not SMARC-compliant).

### 3.3.5 SDIO card interface

The SDIO Card interface is provided by the USDHC1 interface of the i.MX 8X. In contrast to the TQMa8Xx, the CPU supply pin "VDD_USDHC1_VSELECT_1P8_3P3" is supplied with 3.3V instead of 1.8V. Thus the otherwise necessary level converters for the signals SDIO_CD#, SDIO_WP and SDIO_PWR_EN can be omitted. The SDIO_PWR_EN signal is used to switch on the SD supply voltage on the carrier. To be able to boot from SD card, a high level must be applied to the signal at boot time. However, SDIO_PWR_EN is low by default.

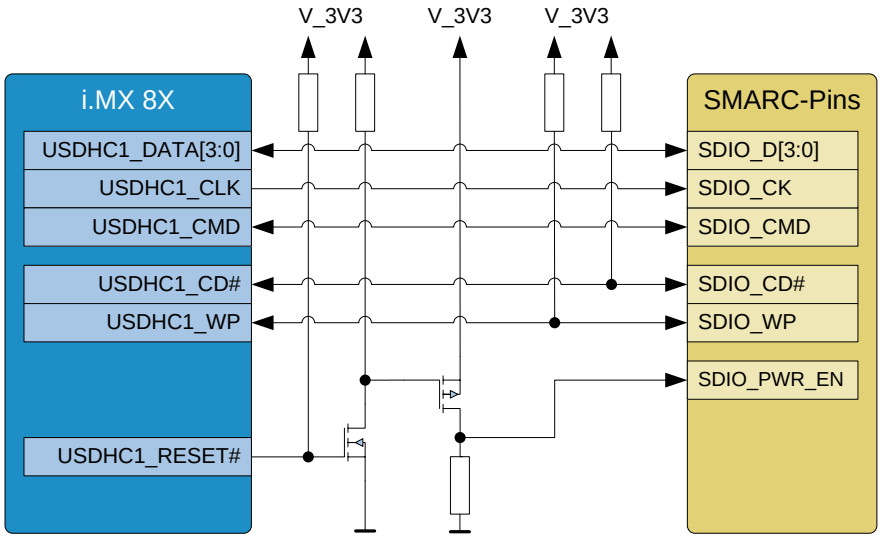


Figure 16: Block diagram SDIO

### 3.3.6 Audio

The I2S0 interface at the SMARC pins is provided by a part of the SAI1 interface as well as by the FLEXCAN1 interface of the i.MX 8X. The AUDIO_MCLK signal is connected to MCLK_OUT0 of the CPU.

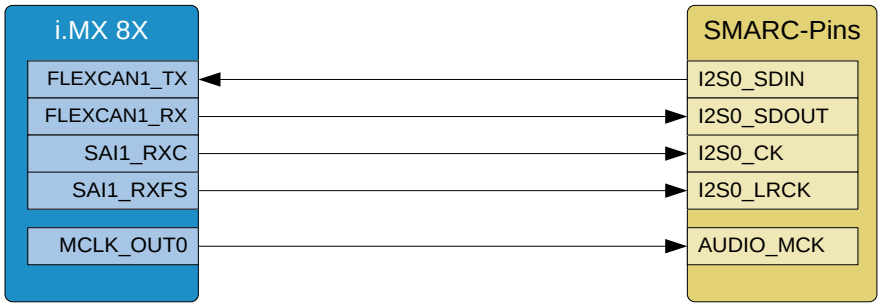


Figure 17: Block diagram Audio

### 3.3.7 SPI

For the SPI0 interface of the SMARC pins, the SAI0 balls of the i.MX 8X are used. For the provision of the second chip select signal, however, a SAI1 ball of the CPU is used.


Figure 18: Block diagram SPI

### 3.3.8 eSPI

The QSPI0B interface of the i.MX 8X is connected to the eSPI pins. The signals are only routed to the outside if the optional NOR Flash is not assembled. Since this is a memory interface and not an eSPI interface according to Intel standard, functional restrictions are to be expected if other devices than QSPI memory are connected. The signals ESPI_RESET# and ESPI_ALERT0# are realized with GPIOs of the CPU. ESPI_ALERT1# is not used.

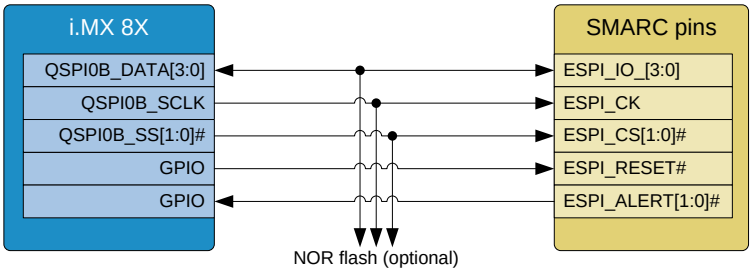


Figure 19: Block diagram eSPI

### 3.3.9 Serial ports

Two UART interfaces of the i.MX 8X may be used due to multiplexing. UART0 of the CPU is provided including CTS and RTS signals at the SER0 pins. The SCU-UART interface of the i.MX 8X is connected to SER1. The UART interfaces can be used by the software to output boot messages. The SER2 and SER3 interfaces are not used. Instead of SCU_UART also UART3 or M4_UART0 can be multiplexed to these pins.

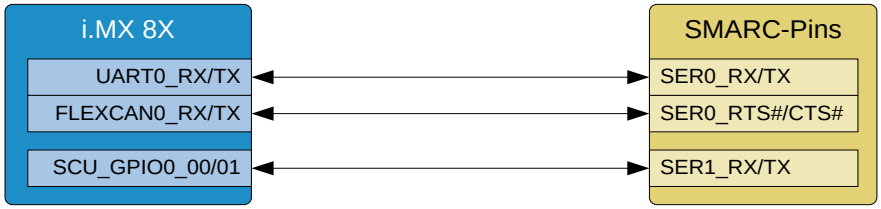


Figure 20: Block diagram Serial Ports

### 3.3.10 CAN bus

Both CAN interfaces are provided at the SMARC pins. CAN0 of the SMARC pins is connected to the UART2 balls of the CPU. The CAN1 pins use FLEXCAN2 of the CPU.

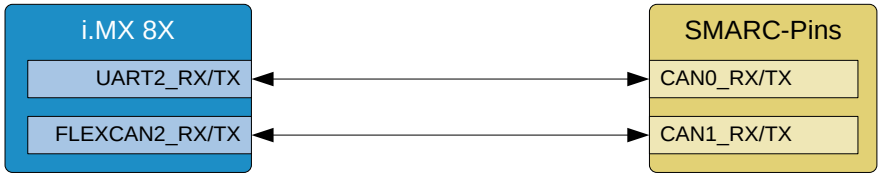


Figure 21: Block diagram CAN

### 3.3.11 PCI Express

A total of four PCIe interfaces are provided in the SMARC standard, of which only PCIE_A is provided by the i.MX 8X. PCIE_[D:B] are not provided. PCIE_WAKE# has a pull-up to 3.3 V on the module.

Furthermore, a clock driver is equipped on the module, since SMARC defines the pins for the clock as outputs and a commissioning with the CPU-internal reference clock has not succeeded so far. The 9FGV0241AKILF from IDT is used for this purpose, which can be configured via I2C0.

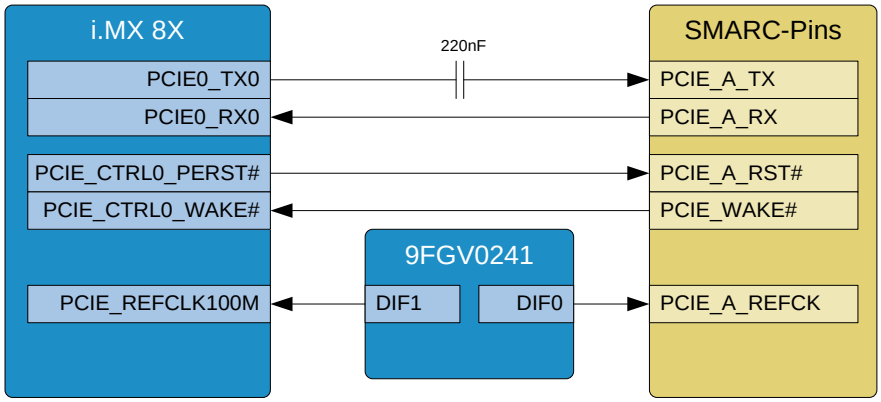


Figure 22: Block diagram PCI Express

### 3.3.12 I²C

The I²C interfaces of the CPU are provided at the SMARC connector as follows:

Table 13: I²C interface

| SMARC pins | i.MX 8X interface | Pull-up resistors |
|---|---|---|
| I2C_GP | I2C0 | 2,49 kΩ |
| I2C_PM | PMIC_I2C | 1,5 kΩ |
| I2C_LCD | MIPI_DSI0_I2C0 | 2,49 kΩ |
| I2C_CAM1 | MIPI_CSI0_I2C0 | 2,49 kΩ |

Standard-compliant pull-up resistors are provided on all I²C signals on the TQMa8XxS.

The following table shows the addresses of the I²C devices used on the TQMa8XxS:

Table 14: I²C addresses

| Bus | Device | Function | Address | Remark |
|---|---|---|---|---|
| I2C0 (I2C_GP) | 24LC64 | EEPROM | 0x50 / 101 0000b | – |
| | PCF85063 | RTC | 0x51 / 101 0001b | – |
| | SE050 | TSE | 0x48 / 100 1000b | |
| | SE97BTP | Temperature sensor | 0x1B / 001 1011b | Access to temperature registers |
| | | EEPROM | 0x53 / 101 0011b | R/W access in Normal Mode |
| | | EEPROM | 0x33 / 011 0011b | R/W access in Protected Mode |
| | | PCIe clock driver | 0x6A / 110 1010b | |
| PMIC_I2C (I2C_PM) | PF8x00 | PMIC | 0x08 / 000 1000b | Communication Interface to TQMa8XxS PMIC only, not useable for general purpose. |
| DSI0_I2C (I2C_LCD) | | DisplayPort-Bridge | 0x0F / 000 1111b | |

### 3.3.13 GPIO

The SMARC standard specifies a total of 12 GPIOs. The standard recommends to use GPIO0...5 preferably as output and GPIO6...11 preferably as input. The i.MX 8X GPIOs can be used in both directions. GPIO11 cannot be used as GPIO because it is not connected on the module.

A special alternative use is provided for GPIO5 and GPIO6, which are intended as PWM output or tachometer input. These two signals are therefore connected to CPU balls, which can be used as GPIO or as PWM output or timer capture input.

Some of the GPIO pins used can be multiplexed as ADC input. The ADC reference voltage of the i.MX 8X is connected to 1.8 V by default. The reference voltage can also be applied externally through the GPIO0 pin using the placement option.

Additional interfaces are available at the GPIO pins used for multiplexing. The following table lists the connected default GPIOs and their possible alternative functions.

Table 15: GPIO pins and alternative functions

| SMARC pin | GPIO (default) | ADC | SPI | I²C / UART | Other |
|---|---|---|---|---|---|
| GPIO0 | GPIO1_IO04 | VREF [3] | SPI0_SCK | M4_I2C0_SCL | M4_GPIO0_IO00 |
| GPIO1 | GPIO1_IO05 | – | SPI0_SDI | – | M4_TPM0_CH0 |
| GPIO2 | GPIO1_IO06 | – | SPI0_SDO | M4_I2C0_SDA | M4_GPIO0_IO01 |
| GPIO3 | GPIO1_IO08 | – | SPI0_CS0 | – | M4_TPM0_CH1 |
| GPIO4 | GPIO1_IO13 | ADC_IN5 | – | – | M4_GPIO0_IO05 |
| GPIO5 | GPIO0_IO22 | – | – | UART1_RX | PWM1_OUT |
| GPIO6 | GPIO0_IO21 | – | – | UART1_TX | GPT0_CAPTURE |
| GPIO7 | GPIO1_IO10 | ADC_IN0 | – | M4_I2C0_SCL | M4_GPIO0_IO00 |
| GPIO8 | GPIO1_IO09 | ADC_IN1 | – | M4_I2C0_SDA | M4_GPIO0_IO01 |
| GPIO9 | GPIO1_IO12 | ADC_IN2 | – | M4_UART0_RX | M4_GPIO0_IO02 |
| GPIO10 | GPIO1_IO11 | ADC_IN3 | – | M4_UART0_TX | M4_GPIO0_IO03 |
| GPIO11 | NC | – | – | – | – |

3: Placement option.

The SMARC specification allows the use of chip-internal pull-up configurations instead of discrete pull-up resistors. Therefore, in order not to influence the possible alternative functions, discrete resistors are not used, instead internal pull-ups of the i.MX 8X are to be used. In addition, after reset on the CPU balls, the internal pull-down resistors are active, which must be switched off during boot. At the same time the internal pull-up resistors can be enabled.

### 3.3.14 Boot Select

The Boot Select signals and FORCE_RECOV# are logically linked by a CPLD and converted into the corresponding BOOT_MODE signals for the i.MX 8X. For further details see section 3.2.1.3.

### 3.3.15 Watchdog

The watchdog signal SCU_WDOG0_WDOG_OUT of the i.MX 8X is connected to the watchdog input of the PMIC and to the SMARC pin WDT_TIME_OUT#. Both can be disconnected via 0R jumper.

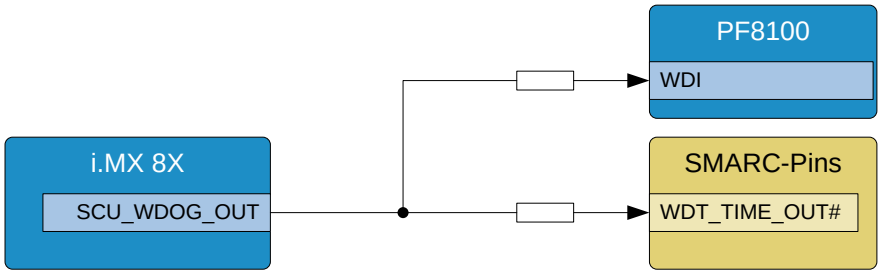


Figure 23: Block diagram Watchdog

### 3.3.16 JTAG

The JTAG interface of the i.MX 8X is provided on an optional connector X2 on the TQMa8XxS. In addition, test points are provided at the JTAG signals. The optional connector and the pin assignment are defined in the SMARC specification (6).

Table 16: Pin assignment JTAG connector

| Pin | Name (SMARC spec.) | I/O | Signal (CPU ball) |
|---|---|---|---|
| 1 | VDD_JTAG_IO | P | V_1V8 |
| 2 | JTAG_TRST# | - | NC |
| 3 | JTAG_TMS | I | JTAG_TMS (AG35) |
| 4 | JTAG_TDO | O | JTAG_TDO (AF32) |
| 5 | JTAG_TDI | I | JTAG_TDI (AH34) |
| 6 | JTAG_TCK | I | JTAG_TCK (AE31) |
| 7 | JTAG_RTCK | I | NC |
| 8 | GND | P | GND |
| 9 | MFG_MODE# | I | NC |
| 10 | GND | P | GND |

## 3.4 Management pins

The SMARC standard provides a large number of control signals, which can be roughly divided into two categories. The following table shows an overview of the SMARC pins that are connected to the CPU (6):

Table 17: Management pins

| Signal | I/O | Level | Description | Usage |
|---|---|---|---|---|
| CARRIER_STBY# | O | 1.8 V | Standby status | SCU_PMIC_STANDBY from i.MX 8X to PMIC (low-active), linked to CARRIER_PWR_ON (see Figure 24) |
| POWER_BTN# | I | 1.8 V | i.MX 8X ON/OFF | i.MX 8X ON_OFF_BUTTON |
| SLEEP# | I | 1.8 V | Carrier Sleep Status | i.MX 8X GPIO0_IO13 (Debouncing via RC element and Schmitt Trigger) |
| LID# | I | 1.8 V | Enclosure status | i.MX 8X GPIO0_IO12 (Debouncing via RC element and Schmitt Trigger) |
| BATLOW# | I | 1.8 V | Low battery voltage | i.MX 8X GPIO0_IO16 |
| CHARGING# | I | 1.8 V | Status Charging | i.MX 8X GPIO0_IO14 |
| CHARGER_PRSNT# | I | 1.8 V | Status Charging voltage | i.MX 8X GPIO0_IO15 |
| TEST# | I | 1.8 V | Test functions | NC; 10k Pull-up to V_1V8 |
| SMB_ALERT_1V8# | I | 1.8 V | SMBus interrupt | i.MX 8X GPIO0_IO19 (Alt: MCLK_IN0) |

In order for the signal CARRIER_STBY# to correspond to the default from SMARC Power Sequencing, it is logically AND-linked to the signal CARRIER_PWR_ON. In sequencing, the high edge at CARRIER_STBY# must not occur before the high edge at CARRIER_PWR_ON. The PMIC pin STANDBY must be configured as high-active since the CPU actively drives the signal low.

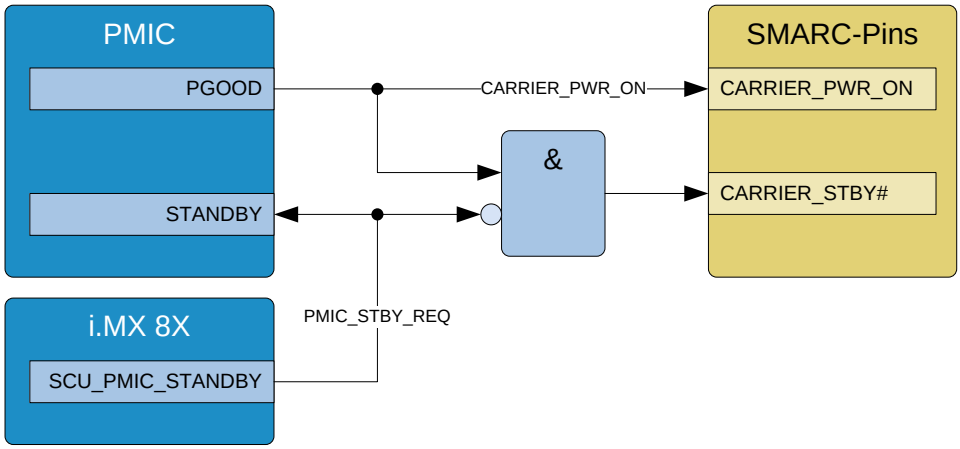


Figure 24: Block diagram CARRIER_STBY#

Another part of the signals is used to control the PMIC.

## 3.5 Trust Secure Element

Depending on the module variant, a Trust Secure Element (TSE) is available on the TQMa8XxS. This is connected to the I2C0 bus of the i.MX 8X via a level translator.

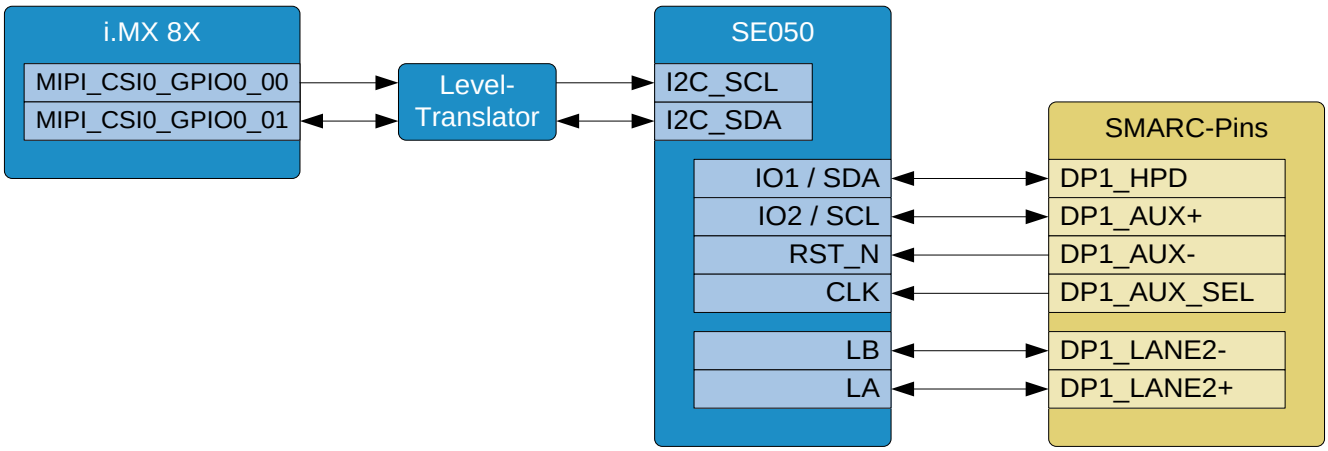


Figure 25: Block diagram Trust Secure Element

The selected chip SE050 from NXP provides additional smartcard interfaces according to ISO14443 and ISO7816 besides the I2C interface. The connection of the antenna for ISO 14443 or the sensor for ISO 7816 must be made on the base board.
Since the SMARC standard does not provide any pins for the smartcard interfaces, the signals for the interfaces according to ISO14443 and ISO7816 are connected to unused SMARC pins.

If the SE050 is equipped as an option, but no ISO14443 and ISO7816 devices are to be operated, the signals on the main board are to be wired as follows:

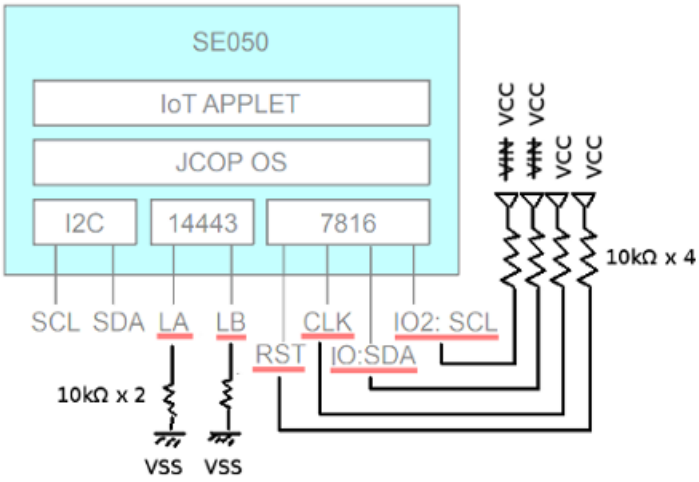


Figure 26: Connecting the NC-Pins
(Source: NXP)

## 3.6 Unused CPU signals

CPU signals, which are not yet used by other functions and interfaces, are made available for optional use at unused SMARC pins. Among other things, the complete parallel CSI interface is led out. The signals do not conform to the SMARC specification and are therefore connected by optional 0-Ω bridges. The 0-Ω bridges are not equipped as standard.

| Note: Alternative functions of CPU signals | |
|---|---|
|  | These signals and their use do not comply with the SMARC specification and are therefore not connected to the SMARC connector of any standard TQMa8XxS. For customized TQMa8XxS and indicating that they are not covered by the SMARC standard, these signals can be made available to SMARC connector through 0 Ω bridges. |

Table 18: Optional CPU signals

| SMARC pin | Signal i.MX 8X | Alternative function |
|---|---|---|
| CSI0_TX+ / I2C_CAM0_CK | CSI_D00 | TAMPER_OUT0 |
| CSI0_TX– / I2C_CAM0_DAT | CSI_D01 | TAMPER_OUT1 |
| CSI0_CK+ | CSI_D02 | TAMPER_OUT2 |
| CSI0_CK– | CSI_D03 | TAMPER_OUT3 |
| CSI0_RX0+ | CSI_D04 | TAMPER_OUT4 |
| CSI0_RX0– | CSI_D05 | TAMPER_IN0 |
| CSI0_RX1+ | CSI_D06 | TAMPER_IN1 |
| CSI0_RX1– | CSI_D07 | TAMPER_IN2 |
| PCIE_D_TX+ | CSI_HSYNC | TAMPER_IN4 |
| PCIE_D_TX– | CSI_VSYNC | TAMPER_IN3 |
| PCIE_D_RX+ | CSI_MCLK | GPIO3_IO01 |
| PCIE_D_RX– | CSI_PCLK | GPIO3_IO00 |
| HDA_SYNC / I2S2_LRCK | CSI_EN | GPIO3_IO02 |

## 3.7 CPLD

A CPLD is used to implement the boot configuration so that specification changes can be addressed flexibly. Instead of a redesign of the digital logic, only a software change (CPLD configuration) is then necessary.

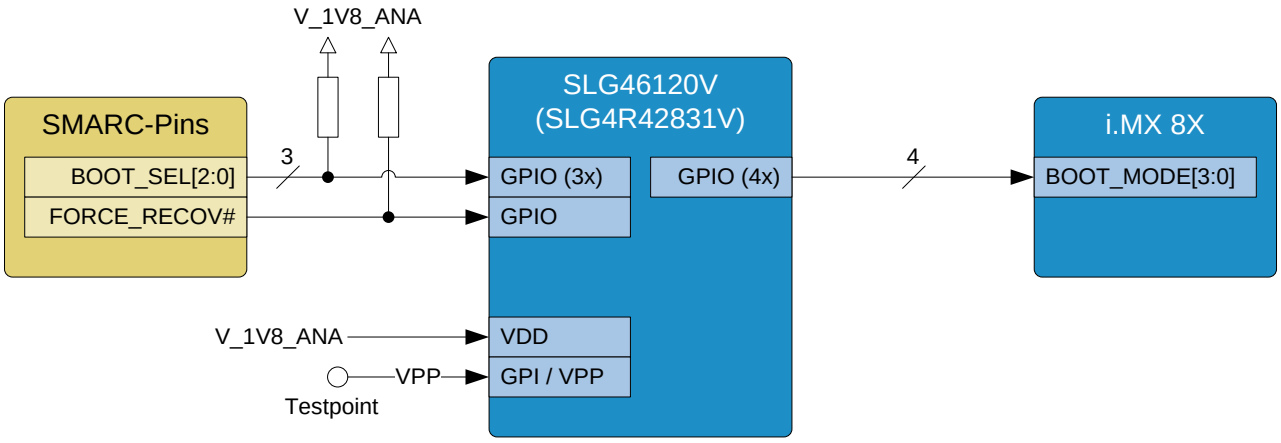


Figure 27: Block diagram CPLD

The input signals BOOT_SEL[2:0] and FORCE_RECOV# as well as the output signals BOOT_MODE[3:0] are connected to programmable IO pins of the CPLD. Since due to the PMIC sequencing the CPU reset signal is strongly delayed (>100 ms), it is ensured that valid output signals are present at the CPLD until the BOOT_MODE pins are sampled by the CPU. The SLG46120V has a startup time of only 310 µs.
The CPLD is obtained and assembled already pre-programmed. Programming in the board after manufacturing or during functional test is not necessary. However, test points are provided on the programming pins for development purposes. The signals are assigned so that only external signals (SMARC pins) are applied to the programming pins. The customer-specific programming gives the chip the designation SLG4R42831V.

## 3.8 Power

### 3.8.1 Power supply rails

The TQMa8XxS only requires a single power supply of 3.0 V to 5.25 V (wide range input). All supply voltages required by the CPU are generated by the PMIC on the module.

The following block diagram shows the power rails of the TQMa8XxS:

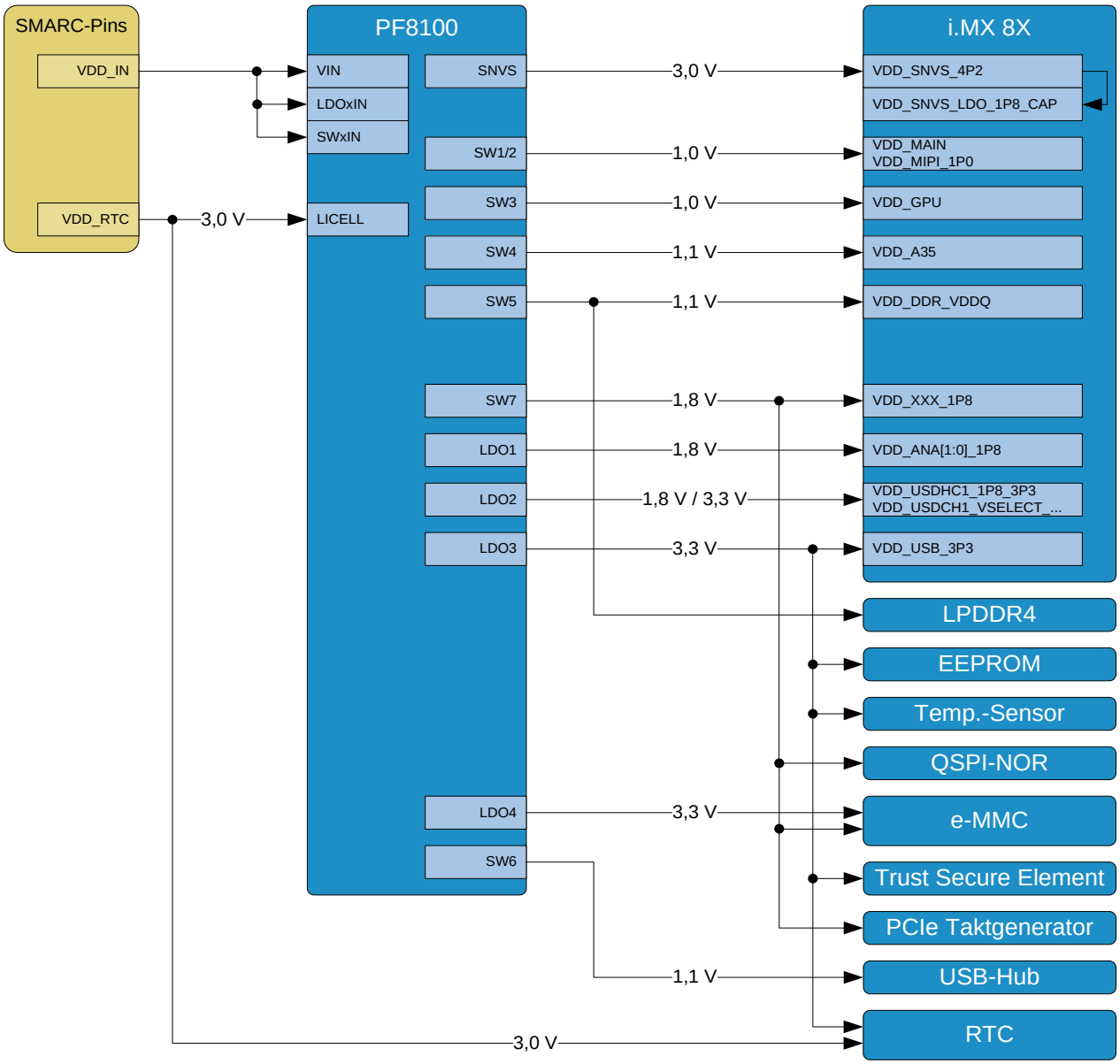


Figure 28: Block diagram PMIC power rails

#### 3.8.1.1 V_VDD_IN

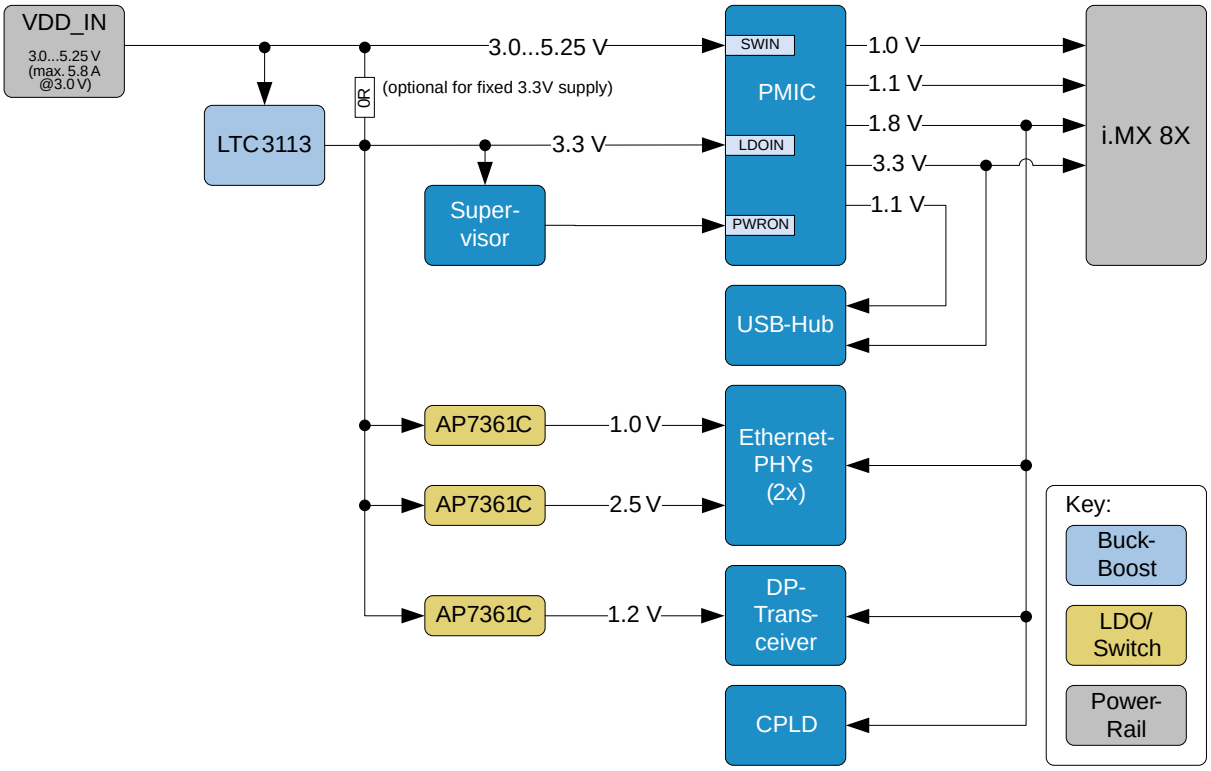


Figure 29: Block diagram module supply

The power consumption of the TQMa8XxS strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values. Further information about power consumption and savings can be found in the application note AN12338 from NXP.

The following table shows the power consumption values of the TQMa8XxS at supply voltages of 3.3 V and 5.0 V:

Table 19: TQMa8XxS power consumption with different supply voltages

| Parameter | @3.3 V supply | @5.0 V supply | Note |
|---|---|---|---|
| Supply voltage V_VDD_IN | 3.135 V to 3.465 V | 4.75 to 5.25 V | typ. ± 5 % |
| TQMa8XQPS | | | |
| Current consumption Off-mode | 17 mA | 17 mA | PMIC_PWRON = low |
| Current consumption Reset | 561 mA | 389 mA | RESET_IN# = low |
| Current consumption theoretical worst case | 4,95 A | 3,12 A | In buck-boost mode at 3.0 V |
| Current consumption U-Boot-Idle | 599 mA | 418 mA | |
| Current consumption Linux-Idle | 718 mA | 495 mA | |
| Current consumption stress app test | 1269 mA | 850 mA | Higher current consumption must be expected when using additional interfaces in parallel |

No measurements have yet been performed for modules with i.MX 8DualXPlus and i.MX 8DualX.

#### 3.8.1.2 V_VDD_RTC

The SMARC pin VDD_RTC allows the connection of a coin cell. Depending on the module variant, either the SNVS domain of the i.MX 8X or the external RTC is supplied via the V_VDD_RTC voltage connected to it.

| Note: Functional scope of RTC | |
|---|---|
|  | Depending on the TQMa8XxS variant, the range of functions in battery mode (only VDD_RTC supplied) is reduced, since no SNVS function of the i.MX 8X is available when using the PCF85063.<br><br>For TQMa8XxS variants without external RTC, the voltage range of the SMARC pin is limited to 2.4 V to 3.25 V by the VSNVS rail of the PMIC. The SMARC standard, however, requires 2.0 V to 3.25 V and is therefore not met. |

#### 3.8.1.3 USB_OTG[2:1]_VBUS

The voltage inputs USB_OTG1_VBUS and USB_OTG2_VBUS are used to detect the USB-VBUS voltage. While USB_OTG1_VBUS is 5 V tolerant, USB_OTG2_VBUS has only a 3.3 V level.

### 3.8.2 Voltage monitoring

The 3.3 V input voltage is monitored on the TQMa8XxS.
If the input voltage is too low, a reset is triggered until the input voltage is within the defined range again.

| Attention: Malfunction or destruction | |
|---|---|
|  | The voltage monitoring does not detect an exceedance of the maximum permitted input voltage.<br>An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa8XxS. |

### 3.8.3 Power-Up sequence TQMa8XxS / carrier board

Since the TQMa8XxS can be operated with a supply voltage of 3.0 V to 5.25 V and all voltages of the CPU signals are generated on the TQMa8XxS, there are requirements for the mainboard design concerning the time behavior of the voltages generated on the mainboard. The mainboard voltages are to be released exclusively by the SMARC pin CARRIER_PWRON. This is connected to the PMIC signal PGOOD.

The following figure shows the voltage regulator control of a carrier board:

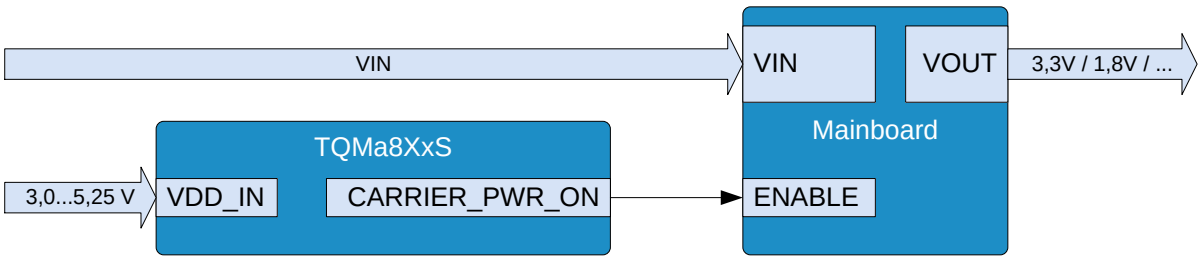


Figure 30: Block diagram power supply carrier board

The following figure shows the switch-on sequence of the controllers, as well as the enable signal:

PF8x00 Power Sequencing

| Regulator | Voltage | Sequence |
|---|---|---|
| VSNVS | 3,0 V | 0 |
| SW1/2 | 1,0 V | 1 |
| LDO1 | 1,8 V | 1 |
| SW3 | 1,0 V | 3 |
| SW4 | 1,1 V | 3 |
| SW7 | 1,8 V | 4 |
| LDO2 | 1,8 / 3,3 V | 4 |
| LDO3 | 3,3 V | 4 |
| LDO4 | 3,3 V | 4 |
| SW6 | 1,1 V | 4 |
| SW5 | 1,1 V | 5 |
| **Signal** | | **Sequence** |
| PGOOD | | 7 |
| RESETMCU | | 254 |

Figure 31: Power-up sequenz PMIC

| Attention: Power-Up sequence | |
|---|---|
|  | To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed.<br>The end of the power-up sequence is indicated by a high level of signal V_1V8.<br>To ensure a correct power-up, the following sequence must be met on the carrier board:<br>The supply voltage of 3.3 V for the TQMa8XxS is present and the carrier board supply of 3.3 V is activated with TQMa8XxS voltage V_1V8. |

### 3.8.4 PMIC

The PF8100 with TQ-specific OTP programming is used on the TQMa8XxS as standard. The PMIC is connected to a dedicated I2C bus of the processor for power management (PMIC_I2C).

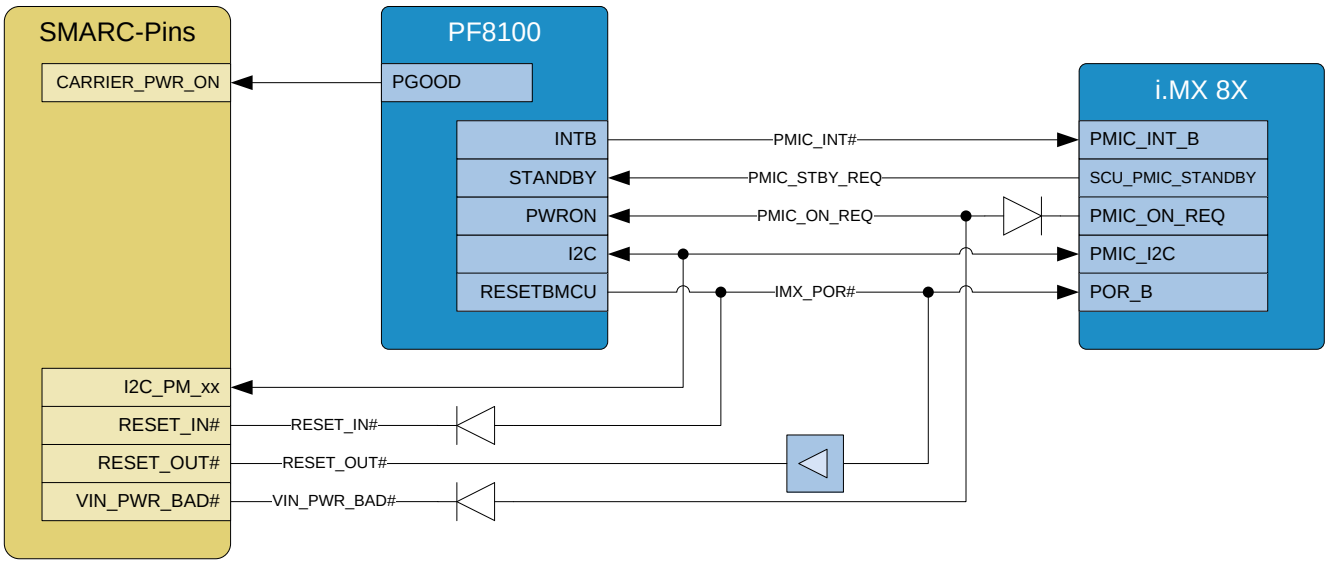


Figure 32: Block diagram PMIC signals

A part of the control signals between PMIC and CPU is also available at the SMARC pins. A more detailed signal description can be found in the following table:

Table 20: Provided PMIC signals

| SMARC-Pin | I/O | Power domain | Remark |
|---|---|---|---|
| RESET_IN# | I | V_1V8_ANA | • reset input of the i.MX 8X via diode to POR_B of the CPU (pull-up to module); low active |
| RESET_OUT# | O | V_1V8_ANA | • reset output of the PMIC (pull-down to module) |
| I2C_PM_CK<br>I2C_PM_DAT | I/O | V_1V8_ANA | • dedicated PMIC interface<br>• can be used for further power management on mainboard<br>• see I2C interfaces |
| CARRIER_PWR_ON | O | V_1V8_ANA | • enable signals of the power supply on carrier<br>• output of the PMIC power monitor<br>• has pull-up on module<br>• see data sheet PMIC |
| VIN_PWR_BAD# | I | VDD_IN | • status module voltage supply from Carrier<br>• enable signal for PMIC (high-active), buck-boost and linear regulator<br>• is activated by default when V_3V3_IN is switched on<br>• to activate: float or connect to 3.3 V<br>• to deactivate: connect to GND |

The properties and functions of the pins and signals are described in the data sheets res. reference manuals of the PMIC (4) and the CPU (1)(2).

PMICs in die revision C1 are used, which use module-specific OTP programming. The program data was created with the tool "OTP-Request-Form" from NXP.

According to the specification, the PMIC can be configured via the PMIC_I2C interface after the boot of the system.

| Attention: Malfunction or destruction | |
|---|---|
|  | The PMIC can be controlled via the dedicated i.MX 8X I²C bus (PMIC_I2C).<br>Improper PMIC programming may cause the i.MX 8X or other peripherals on the TQMa8XxS to operate outside their specification.<br>This can lead to malfunction, deterioration or destruction of the TQMa8XxS. |

# 4. MECHANICS

## 4.1 Connector

The TQMa8XxS is connected to the carrier board through 314 PCB contacts.

The following table shows some suitable mating connectors for the carrier board.

Table 21: TQMa8XxS mating connectors

| Manufacturer | Part | Connector height | Board-To-Board |
|---|---|---|---|
| JAE | MM70 Series | 4.3 mm, 6.7 mm | 1.5 mm, 3.0 mm |
| Nexus Components | 5242 Series | 7.5 mm | 5.0 mm |
| EFCO | 30470 Series | 2.7 mm, 5 mm, 11.1 mm | 5.2 mm, 7.5 mm, 13.6 mm |

## 4.2 Dimensions

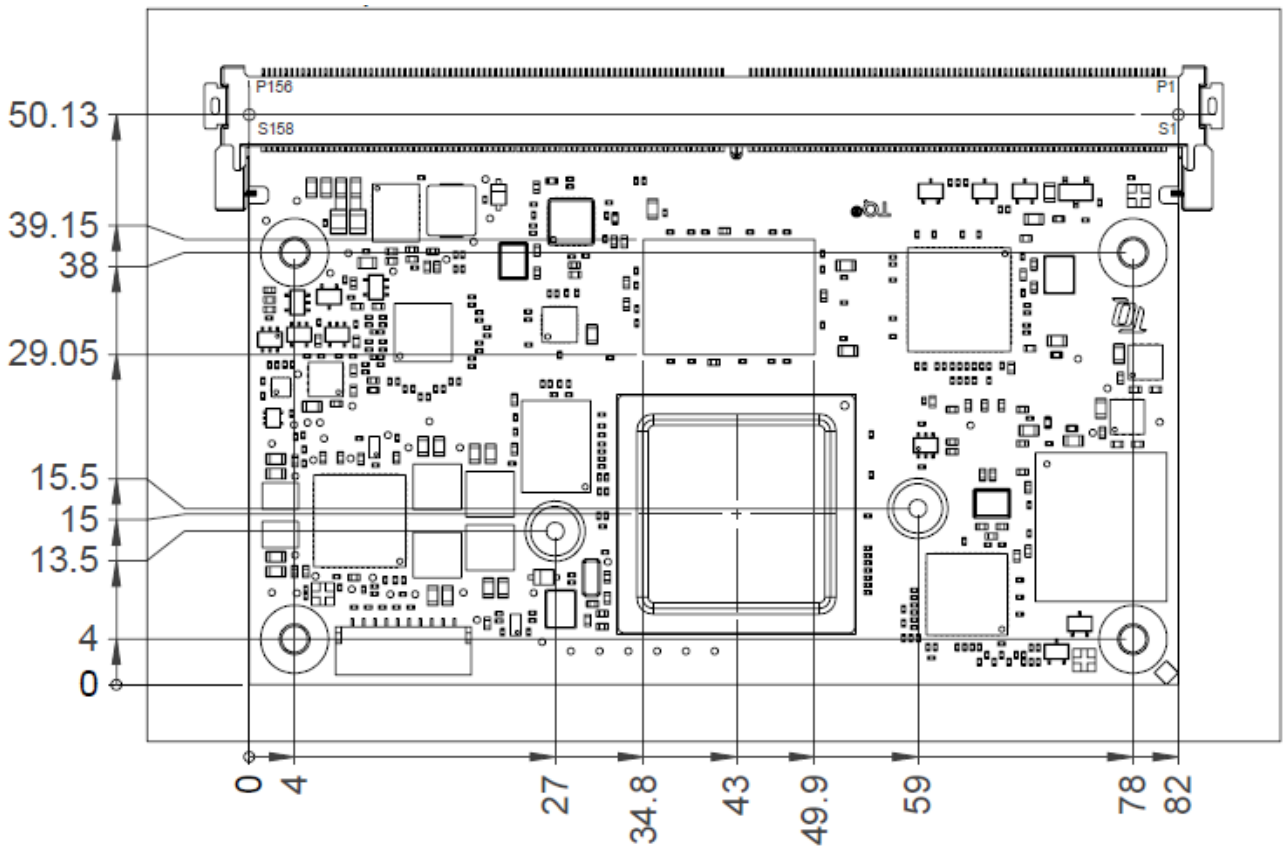


Figure 33: TQMa8XxS dimensions

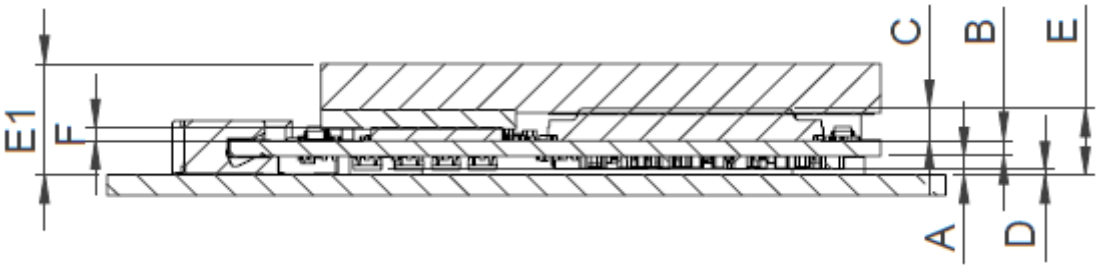


Figure 34: TQMa8XxS heights with heatspreader

Table 22: Heights

| Property | Value | Tolerance | Unit | Remark |
|---|---|---|---|---|
| A | 1,55 | ±0,15 | mm | Board to board distance |
| B | 1,20 | ±0,12 | mm | Printed circuit board thickness |
| C | 2,27 | ±0,15 | mm | Processor height (typically highest component) |
| D | 0,43 | ±0,09 | mm | Installation space under the module |
| E | 5,02 | ±0,20 | mm | Total height from top edge of base board to CPU surface |
| E1 | 8,75 | ±0,24 | mm | Total height from top edge of baseboard to surface of heatspreader |
| F | 1,09 | ±0,10 | mm | Height LPDDR4 |

## 4.3 Component placement

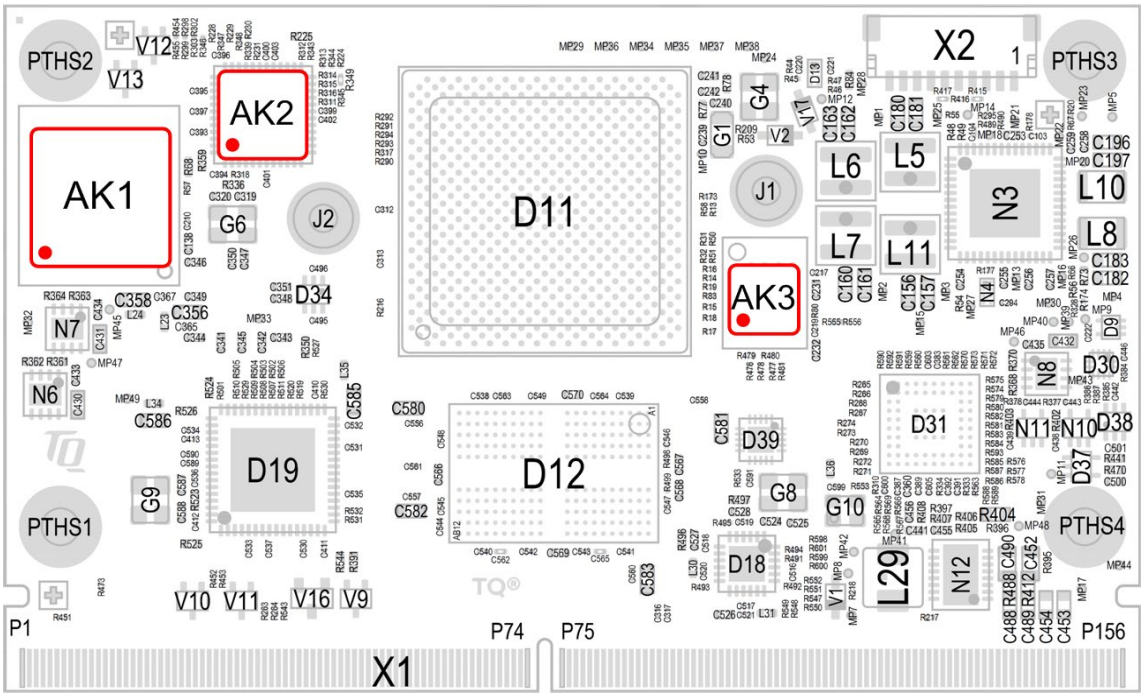


Figure 35: TQMa8XxS, component placement top

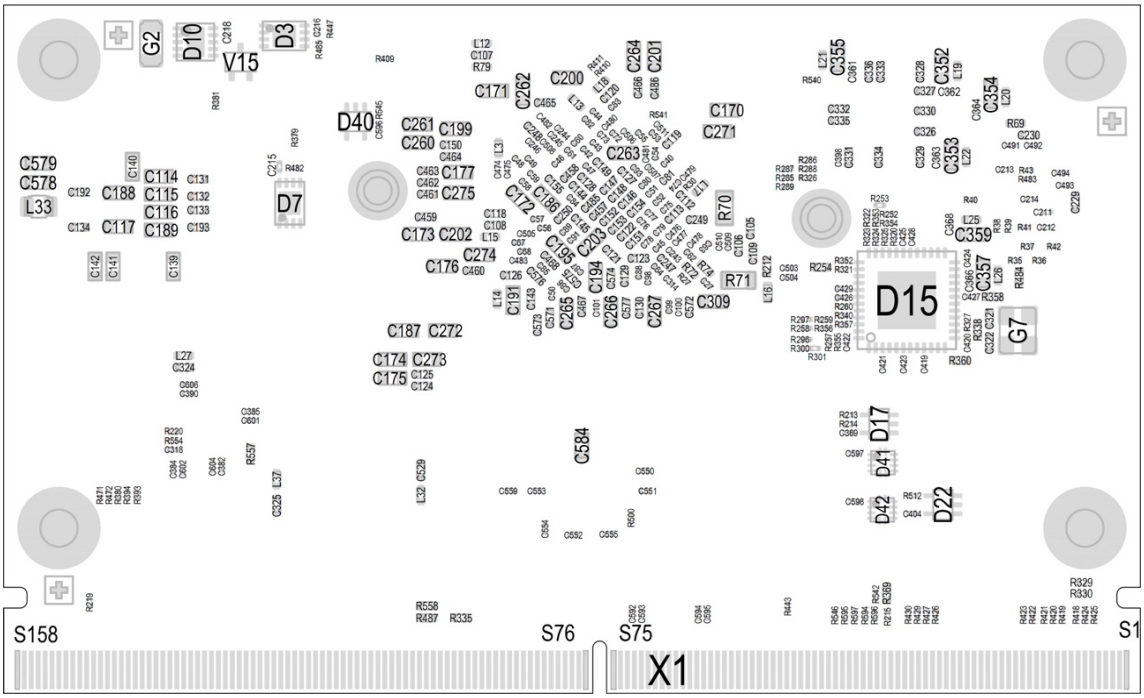


Figure 36: TQMa8XxS, component placement bottom

The labels on the TQMa8XxS show the following information:

Table 23: Labels on TQMa8XxS

| Label | Content |
|---|---|
| AK1 (on D4) | First MAC address plus one additional reserved consecutive MAC address, tests performed |
| AK2 (on D14) | TQMa8XxS version and revision |
| AK3 (on D2) | Serial number |

## 4.4 Adaptation to the environment

The TQMa8XxS has overall dimensions (length × width) of 82 mm × 50 mm (± 0,1 mm).
The TQMa8XxS has a minimum height above the carrier board of 5.02 mm (± 0,2 mm) (depends on connector on carrier board).
The TQMa8XxS weighs approximately 17 g.

## 4.5 Protection against external effects

As an embedded module, the TQMa8XxS is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

## 4.6 Thermal management

To cool the TQMa8XxS, a maximum of approximately 4 watts must be dissipated, see Table 17 for peak currents.
The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 8X, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 8X Data Sheet (1) for further information.

| Attention: Destruction or malfunction, TQMa8XxS heat dissipation | |
|---|---|
|  | The TQMa8XxS belongs to a performance category in which a cooling system is essential.<br>It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8X must be taken into consideration when connecting the heat sink.<br>The i.MX 8X is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8XxS and thus malfunction, deterioration or destruction. |

### 4.7 Structural requirements

The TQMa8XxS has a low retention force and has to be mounted / secured according to customer requirements.
The superior system is defined by the customer depending on the usage of the TQMa8XxS.

## 5. SOFTWARE

The TQMa8XxS is delivered with a preinstalled boot loader U-Boot and the BSP provided by TQ-Systems GmbH, which is tailored for the MB-SMARC-2.
The boot loader U-Boot provides TQMa8XxS-specific as well as board-specific settings, e.g.:

- i.MX 8X configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the TQ-Support Wiki for the TQMa8XxS.

# 6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

## 6.1 EMC

The TQMa8XxS was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display).

As part of the development, an EMC test was performed with the starter kit MB-SMARC-2 REV.02xx in accordance with EN55022:2010 Class A limits.

## 6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa8XxS.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

## 6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

## 6.4 Climate and operational conditions

The operating temperature range for the TQMa8XxS strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8XxS.

The TQMa8XxS is available in three different variants with different temperature ranges. In general, a reliable operation is given when following conditions are met:

Table 24: Climate and operational conditions industrial temperature range

| Parameter | | Range | Remark |
|---|---|---|---|
| Ambient temperature | | –25 °C to +60 °C | – |
| $T_J$ i.MX 8X | | -40 °C to 105 °C | – |
| $T_J$ PMIC | | -40 °C to 150 °C | – |
| Case temperature SDRAM | | -40 °C to 85 °C | – |
| Case temperature other ICs | Variant C | 0 °C to 85 °C | Consumer |
| | Variant E | -25 °C to 85 °C | Extended (Standard) |
| | Variant I | -40°C to 85 °C | Industrial |
| Relative humidity (operating / storage) | | 10 % to 90 % | Not condensing |

| Attention: Destruction or malfunction, TQMa8XxS heat dissipation | |
|---|---|
|  | The TQMa8XxS belongs to a performance category in which a cooling system is essential.<br>It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8X must be taken into consideration when connecting the heat sink.<br>The i.MX 8X is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8XxS and thus malfunction, deterioration or destruction. |

## 6.5 Reliability and service life

The theoretical MTBF of the TQMa8XxS is approximately 610.860 h @ +40 °C ambient temperature, Ground, Benign.

The TQMa8XxS is designed to be insensitive to shock and vibration.

# 7. ENVIRONMENT PROTECTION

## 7.1 RoHS

The TQMa8XxS is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

## 7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa8XxS was designed to be recyclable and easy to repair.

## 7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

## 7.4 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa8XxS must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa8XxS enable compliance with EuP requirements for the TQMa8XxS.

## 7.5 Battery

No batteries are assembled on the TQMa8XxS.

## 7.6 Packaging

The TQMa8XxS is delivered in reusable packaging.

## 7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8XxS, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa8XxS is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

# 8. APPENDIX

## 8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 25: Acronyms

| Acronym | Meaning |
|---|---|
| ADC | Analog/Digital Converter |
| ARM® | Advanced RISC Machine |
| ASIL | Automotive Safety Integrity Level |
| BGA | Ball Grid Array |
| BIOS | Basic Input/Output System |
| BSP | Board Support Package |
| CAN | Controller Area Network |
| CPLD | Complex Programmable Logic Device |
| CPU | Central Processing Unit |
| CSI | Camera Serial Interface |
| DDR | Double Data Rate |
| DDR3L | DDR3 Low voltage |
| DNC | Do Not Connect |
| DP | DisplayPort |
| DSI | Display Serial Interface |
| ECC | Error-Correcting Code |
| eDP | embedded DisplayPort |
| EEPROM | Electrically Erasable Programmable Read-only Memory |
| EMC | Electromagnetic Compatibility |
| eMMC | embedded Multimedia Card |
| ESD | Electrostatic Discharge |
| eSPI | enhanced Serial Peripheral Interface |
| EU | European Union |
| EuP | Energy using Products |
| FR-4 | Flame Retardant 4 |
| GPIO | General-Purpose Input/Output |
| GPMC | General-Purpose Memory Controller |
| GPO | General-Purpose Output |
| GPU | Graphics Processing Unit |
| I/O | Input/Output |
| I²C | Inter-Integrated Circuit |
| I²S | Inter-IC Sound |
| IC | Integrated Circuit |
| IEEE® | Institute of Electrical and Electronics Engineers |
| IP00 | Ingress Protection 00 |
| JEDEC | Joint Electronic Device Engineering Council |
| JTAG® | Joint Test Action Group |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LVDS | Low-Voltage Differential Signalling |
| MAC | Media Access Control |
| MCASP | Multichannel Audio Serial Port |
| MIPI | Mobile Industry Processor Interface |
| MMC | Multimedia Card |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| MTBF | Mean (operating) Time Between Failures |

## 8.1 Acronyms and definitions (continued)

Table 22: Acronyms (continued)

| Acronym | Meaning |
|---|---|
| NAND | Not-And |
| NOR | Not-Or |
| OD | Open-drain |
| OTG | On-The-Go |
| OTP | One-Time Programmable |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect |
| PCIe | Peripheral Component Interconnect Express |
| PCMCIA | People Can't Memorize Computer Industry Acronyms |
| PHY | Physical (layer of the OSI model) |
| PMIC | Power Management Integrated Circuit |
| PRU | Programmable Real-Time Unit |
| PWM | Pulse-Width Modulation |
| PWP | Permanent Write Protected |
| QSPI | Quad Serial Peripheral Interface |
| R/W | Read/Write |
| RAM | Random Access Memory |
| REACH® | Registration, Evaluation, Authorisation (and restriction of) Chemicals |
| RF | Radio Frequency |
| RFU | Reserved for Future Usage |
| RGB | Red Green Blue |
| RGMII | Reduced Gigabit Media-Independent Interface |
| RoHS | Restriction of (the use of certain) Hazardous Substances |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| RWP | Reversible Write Protected |
| SAI | Serial Audio Interface |
| SCU | System Control Unit |
| SD | Secure Digital |
| SDIO | Secure Digital Input/Output |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SMARC | Smart Mobile ARChitecture |
| SMBus | System Management Bus |
| SPI | Serial Peripheral Interface |
| TBD | To Be Determined |
| TSE | Trust Secure Element |
| UART | Universal Asynchronous Receiver / Transmitter |
| UM | User's Manual |
| USB | Universal Serial Bus |
| VPU | Video Processing Unit |
| WDT | Watchdog Timer |
| WEEE® | Waste Electrical and Electronic Equipment |
| WP | Write Protect |

## 8.2 References

Table 26: Further applicable documents

| No. | Name | Rev., Date | Company |
|---|---|---|---|
| (1) | i.MX8QuadXPlus/8DualXPlus Applications Processor Datasheet | Version 2, 02.06.2016 | NXP |
| (2) | Reference Manual of i.MX 8QuadXPlus and 8DualXPlus | Rev. 0, 05/2020 | NXP |
| (3) | i.MX 8X Mask Set Errata for Mask 0N99Z | 1, 20.05.2020 | NXP |
| (4) | PF8100/PF8200 PMIC Datasheet | Rev. 11, 02/2021 | NXP |
| (5) | i.MX8 QM/i.MX8 QXP Hardware Developer's Guide | V1.0, 01/2020 | NXP |
| (6) | SMARC Hardware Specification V200 | Version 2, June 2, 2016 | SGET |
| (7) | MB-SMARC-2 User's Manual | – current – | TQ-Systems |
| (8) | TQMa8XxS Support-Wiki | – current – | TQ-Systems |

**TQ-Systems GmbH**
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

Technology in Quality