MBaRZG2x
User's Manual

MBaRZG2x UM 0102
12.05.2023

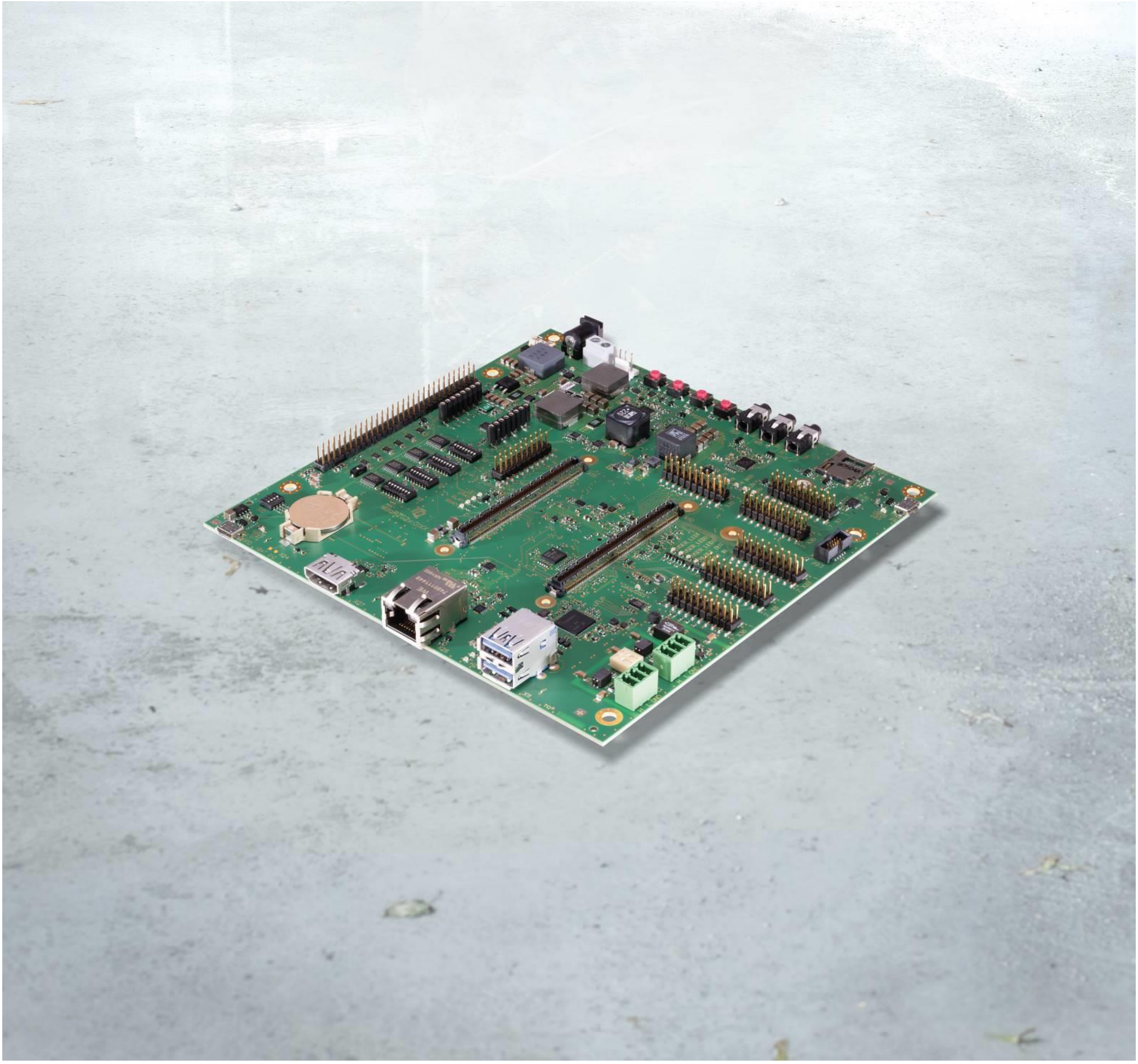

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	05.05.2021	Petz		First edition
0101	03.01.2022	Kreuzer	Table 7	Correction: MD15 must be set to 1 (High) for booting
0102	12.05.2023	Kreuzer	Table 5 Figure 20	3.3 V tolerance added (HDMI_SCL/SDA) Adjusted to new board revision

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Ignoring or acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBaRZG2x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBaRZG2x circuit diagram
- TQMaRZG2x User's Manual
- RZ/G2x User's Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: TQMaRZG2x Support Wiki

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBaRZG2x as of revision 0101.

The MBaRZG2x is designed as a carrier board for the TQMaRZG2x.

All TQMaRZG2x interfaces, which can be used, are available on the MBaRZG2x, thus the features of the CPU RZ/G2x can be evaluated and software development for a TQMaRZG2x-based project can be started directly.

The MBaRZG2x supports TQMaRZG2x modules with an RZ/G2H, RZ/G2M, or RZ/G2N CPU.

2.1 MBaRZG2x block diagram

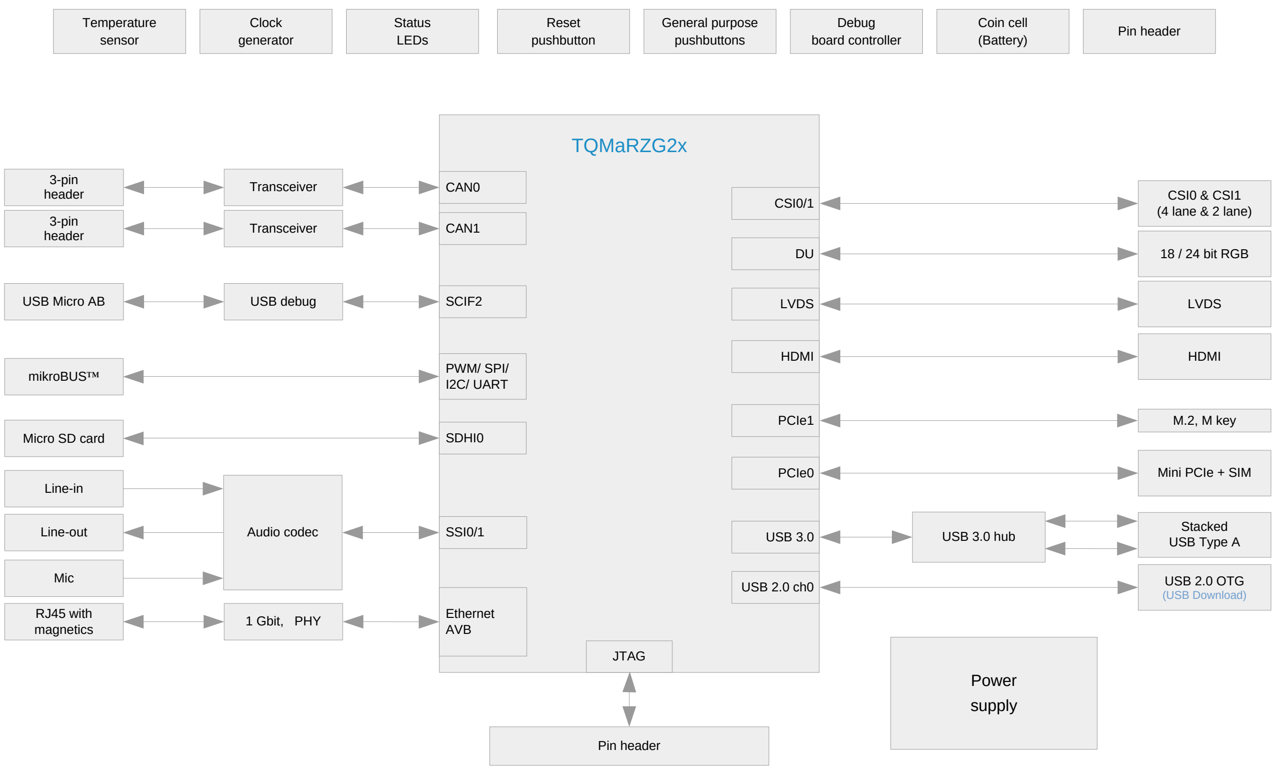


Figure 1: Block diagram MBaRZG2x

2.2 MBaRZG2x interfaces, overview

The following interfaces and functions are provided on the MBaRZG2x:

Table 2: Data interfaces

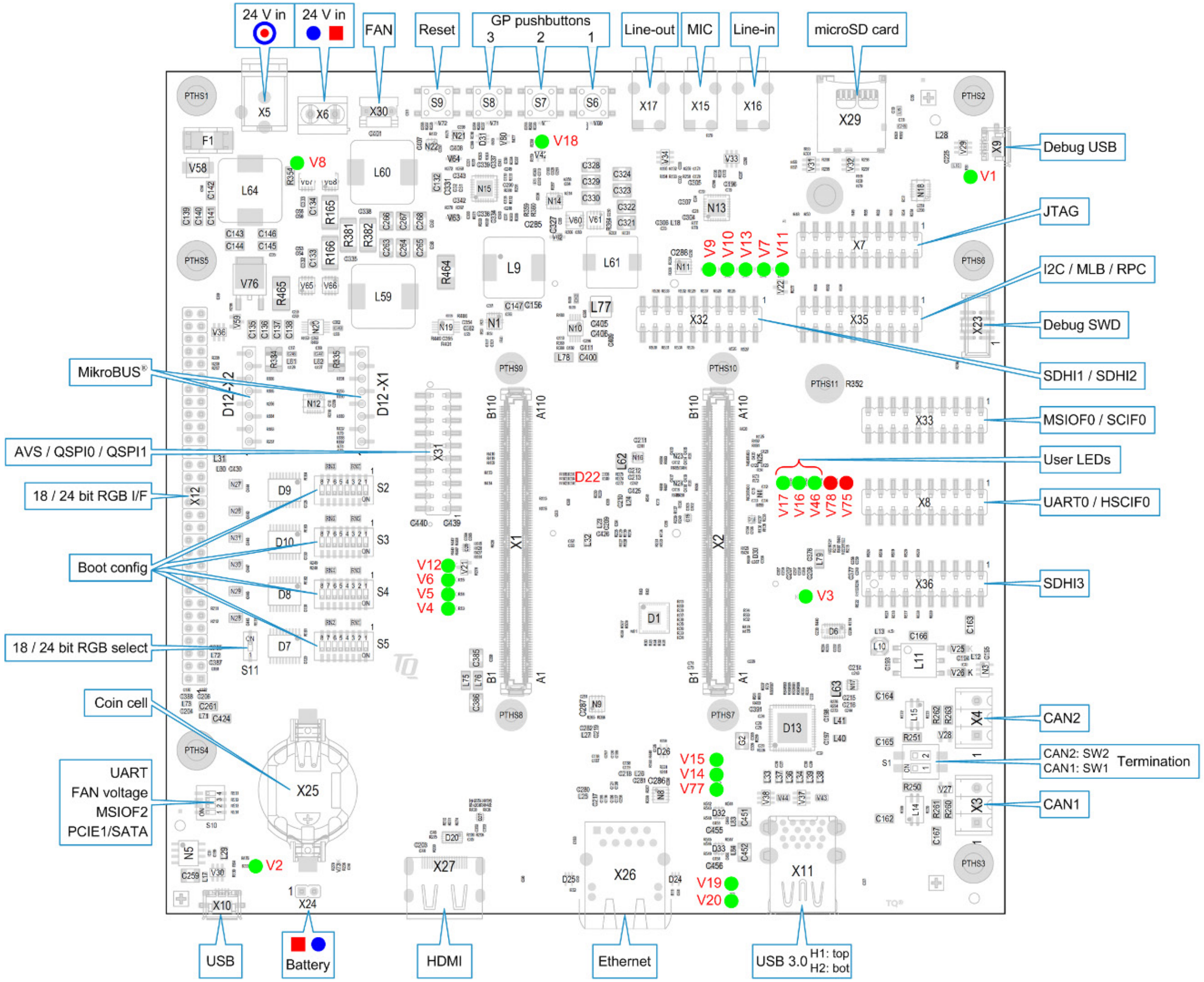
Interface	Connector	Type	Remark
Audio	X15, X16, X17	3 × 3.5 mm jack	MIC, Line-in, Line-out
CAN	X3, X4	MC 1,5/ 3-G-3,5	X3: CAN1 | X4: CAN2
External battery	X24	2-pin header, 100 mil	(NP) Backup supply for RTC on TQMaRZG2x
Coin cell	X25	CR2032	–
Eth 1000 Base-T	X26	RJ-45	Jack with integrated magnetics
FAN	X30	3-pin header, 100 mil	With friction lock
HDMI	X27	HDMI	–
Header	X8, X31, X32, X33, X35, X36	6 × 20-pin header, 100 mil	TQMaRZG2x signals
JTAG	X7	20-pin header, 100 mil	JTAG
Debug SWD	X23	10-pin header, 50 mil	System controller
LVDS data	X19	30-pin, DF19G	ZIF connector
LVDS control	X20	20-pin, DF19G	ZIF connector
M.2, M key	X22	67-pin, M.2	PCIe / SATA, 2242 or 2280 (default)
mikroBUS™	D12-X1, D12-X2	3 × 8-pin header, 100 mil	mikroBUS™ standard
Mini PCIe	X28	52-pin mPCIe	PCIe + USB 2.0
MIPI CSI	X21	60-pin, 0.8 mm	CSI1 and CSI2
Power-in	X5	2.5 / 5.5 mm DC jack	Jack socket
	X6	2-pin, 5 mm pitch	Block terminal
RGB	X12	60-pin header, 100 mil	18 bit or 24 bit selection with S11
microSD card	X29	microSD card	Optional boot source
SIM card	X37	SIM card holder	SIM card slot
USB 2.0	X9	Type Micro AB	SCIF0 and SCIF2, Debug UARTs
USB 2.0	X10	Type Micro AB	USB 2.0, Hi-Speed OTG, serial downloader
USB 3.0	X11	Stacked Type A	USB 3.0 H1: top, USB 3.0 H2: bot

The MBaRZG2x provides the following status and user interfaces:

Table 3: Status and user interfaces

Interface	Reference	Component	Remark
Status LEDs	V19, V20, V2, V1	4 × Green LED	2 × VBUS USB host, 1 × VBUS USB OTG, 1 × USB debug
	X26	2 × Green / Yellow	Ethernet activity / speed
	V17, V16, V46	3 × Green LED	General purpose LEDs
	V3	1 × Green LED	M.2 device activity
	V4, V5, V6	3 × Green LED	mPCIe: WWAN, WLAN, WPAN
	V18	1 × Green LED	PGOOD signal from TQMaRZG2x
	V75, V78	2 × Red LED	Reset-in / Reset-out
	See Figure 2	10 × Green LED	Voltages on MBaRZG2x
Temperature sensor	D22	1 × SE97BTP	Digital I²C temperature sensor + EEPROM
Reset	S9	1 × Pushbutton	TQMaRZG2x reset
GP button	S6, S7, S8	3 × Pushbutton	General purpose pushbuttons
Boot mode	S2, S3, S4, S5	4 × 8-fold DIP switch	Boot device selection
CAN termination	S1	1 × 2-fold DIP switch	120 Ω termination for each CAN interface

2.3 MBaRZG2x interfaces, position



V1:	Debug USB
V2:	USB: V_5V0_VBUS_OTG
V3:	M.2 mPCIe SATA
V4:	WWAN
V5:	WLAN
V6:	WPAN
V7:	V_3V3
V8:	V_24V
V9:	V_12V
V10:	V_5V0
V11:	V_1V8
V12:	V_1V5
V13:	V_5V0_MOD
V14:	V_1V1
V15:	V_1V0
V16:	User LED 2
V17:	User LED 1
V18:	PGOOD
V19:	USB: V_5V0_VBUS_H1
V20:	USB: V_5V0_VBUS_H2
V46:	User LED 3
V75:	Reset RST_IN#
V77:	V_2V5
V78:	Reset RST_OUT#

Figure 2: MBaRZG2x interfaces top

2.3 MBaRZG2x interfaces, position (continued)

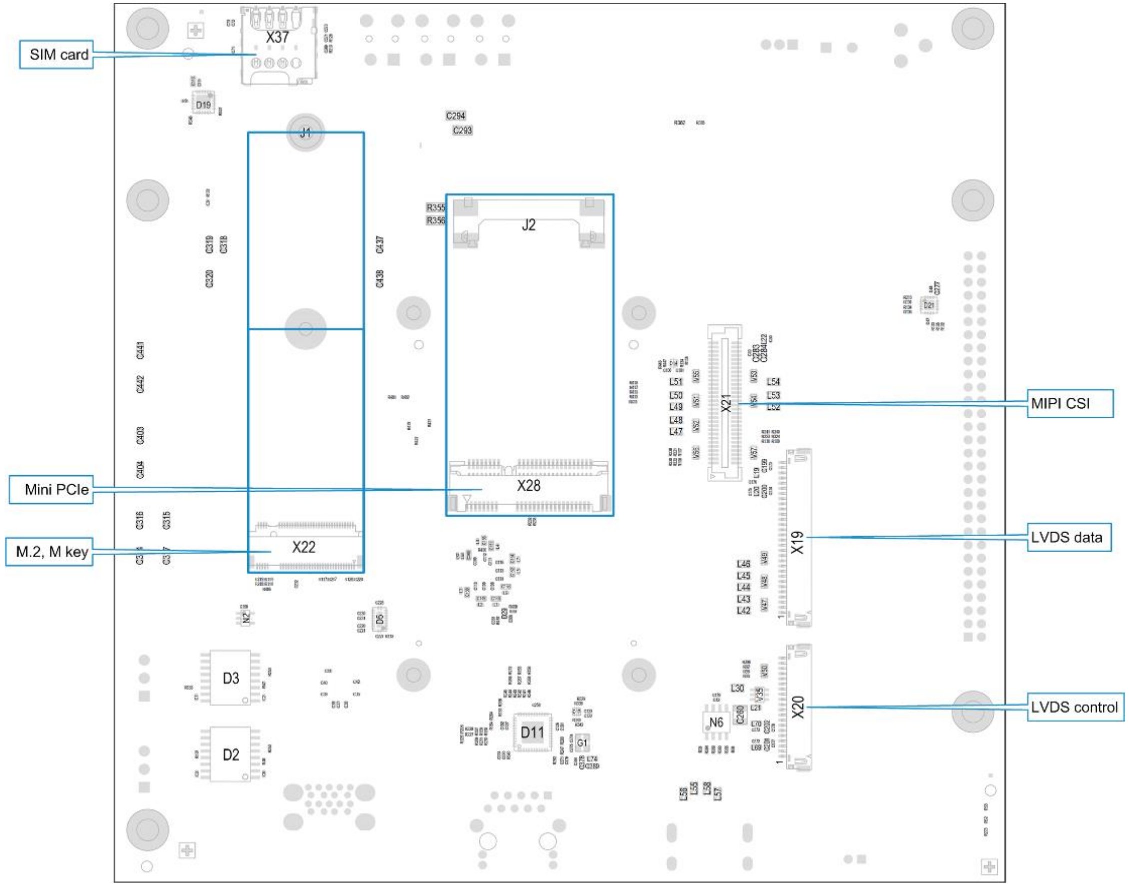


Figure 3: MBaRZG2x interfaces bottom

3. ELECTRONICS

3.1 MBaRZG2x functional groups

3.1.1 TQMaRZG2x

The TQMaRZG2x with its RZ/G2x CPU is the central system component. It provides LPDDR4 SDRAM, eMMC, NOR flash and an EEPROM. All TQMaRZG2x internal voltages are derived from the 5 V supply voltage. Further information can be found in the TQMaRZG2x User's Manual. The available signals are routed to the MBaRZG2x on two connectors. On the MBaRZG2x the interfaces provided by the TQMaRZG2x are routed to industry standard connectors. Furthermore the MBaRZG2x provides all power supplies and configurations required for the operation of the TQMaRZG2x. The MBaRZG2x supports all TQMaRZG2x with an RZ/G2H, RZ/G2M, or RZ/G2N CPU.

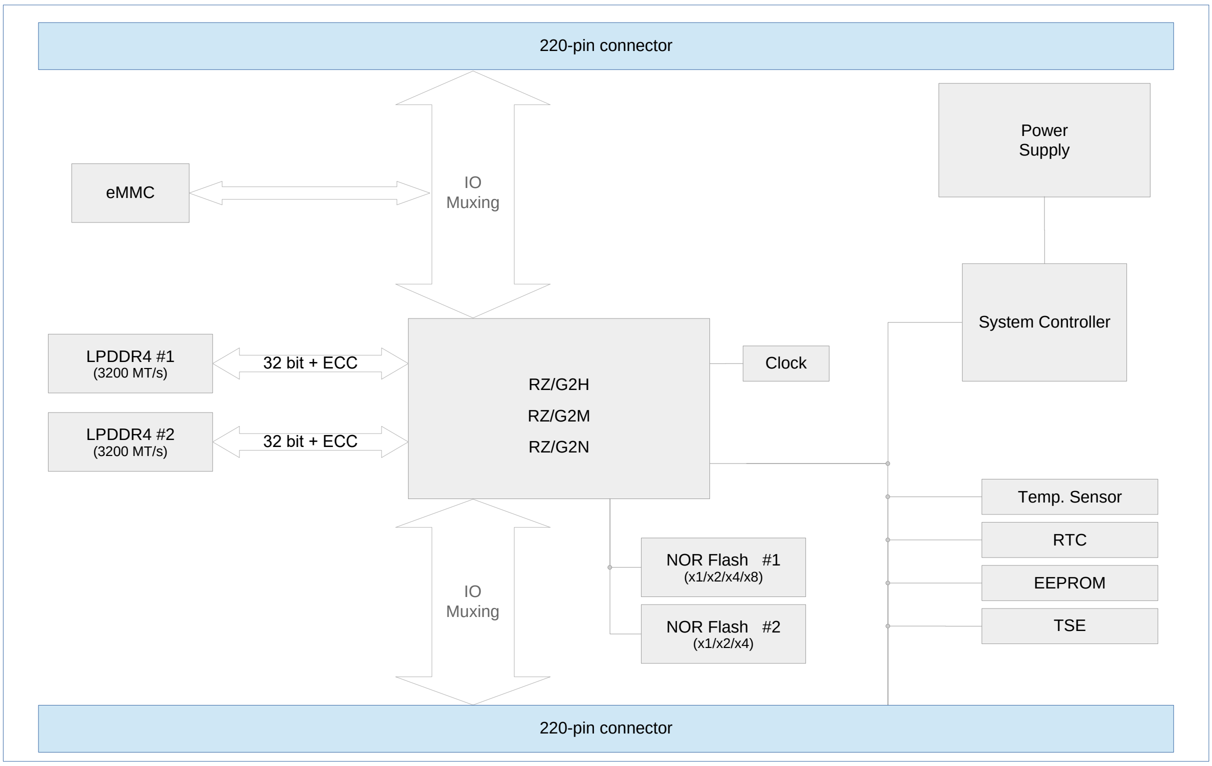


Figure 4: Block diagram TQMaRZG2x

3.1.2 TQMaRZG2x mating connectors

The TQMaRZG2x is connected to the MBaRZG2x with two 220-pin connectors. To avoid damaging the connectors of the MBaRZG2x during extraction, the use of the extraction tool MOZIaRZG2x is strongly recommended.

The following table shows suitable carrier board mating connectors.

Table 4: Carrier board mating connectors

Manufacturer	Stack height	Part number	Remark
EPT	5 mm	401-51101-51	On MBaRZG2x
	8 mm	401-55101-51	–

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMaRZG2x for the extraction tool MOZIaRZG2x.

3.1.3 TQMaRZG2x pinout

All available TQMaRZG2x signals are accessible at two connectors on the MBaRZG2x.

More detailed information is to be taken from the TQMaRZG2x User's Manual (2).

Note: Available interfaces, signal direction	
	➢ Depending on the RZ/G2x derivative not all interfaces are available. Detailed information on the available interfaces can be found in the User's Manual of the RZ/G2x. ➢ The following tables show the signal direction as seen from the TQMaRZG2x.

3.1.3 TQMaRZG2x pinout (continued)

Table 5: Pinout connector X1

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
I	5 V	Power	V_5V_IN	A2	B2	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A3	B3	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A4	B4	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A5	B5	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A6	B6	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A7	B7	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A8	B8	V_5V_IN	Power	5 V	I
–	0 V	Ground	DGND	A9	B9	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A10	B10	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A12	B12	DGND	Ground	0 V	–
O	1.8 V	Power	V_1V8	A13	B13	V_3V3	Power	3.3 V	O
O	1.8 V	Power	V_1V8	A14	B14	V_3V3	Power	3.3 V	O
–	0 V	Ground	DGND	A15	B15	DGND	Ground	0 V	–
O	1.8 V	HDMI	HDMI0_TMDS_DATA2_P	A16	B16	HDMI0_TMDS_DATA1_P	HDMI	1.8 V	O
O	1.8 V	HDMI	HDMI0_TMDS_DATA2_N	A17	B17	HDMI0_TMDS_DATA1_N	HDMI	1.8 V	O
–	0 V	Ground	DGND	A18	B18	DGND	Ground	0 V	–
O	1.8 V	HDMI	HDMI0_TMDS_CLK_P	A19	B19	HDMI0_TMDS_DATA0_P	HDMI	1.8 V	O
O	1.8 V	HDMI	HDMI0_TMDS_CLK_N	A20	B20	HDMI0_TMDS_DATA0_N	HDMI	1.8 V	O
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
I	5 V	HDMI	HDMI0_HPD	A22	B22	HDMI0_SCL	HDMI	1.8 / 3.3 V	O
IO	3.3 V	GPIO	GP7_02	A23	B23	HDMI0_SDA	HDMI	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A24	B24	DGND	Ground	0 V	–
O	1.8 V	LVDS	LVDS0_CH2_P	A25	B25	LVDS0_CH0_P	LVDS	1.8 V	O
O	1.8 V	LVDS	LVDS0_CH2_N	A26	B26	LVDS0_CH0_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A27	B27	DGND	Ground	0 V	–
O	1.8 V	LVDS	LVDS0_CH3_P	A28	B28	LVDS0_CH1_P	LVDS	1.8 V	O
O	1.8 V	LVDS	LVDS0_CH3_N	A29	B29	LVDS0_CH1_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A30	B30	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_DATA0_P	A32	B32	LVDS0_CLK_P	LVDS	1.8 V	O
I	1.8 V	CSI	CSI0_DATA0_N	A33	B33	LVDS0_CLK_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A34	B34	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_DATA2_P	A35	B35	CSI0_DATA1_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI0_DATA2_N	A36	B36	CSI0_DATA1_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A37	B37	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_CLK_P	A38	B38	CSI0_DATA3_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI0_CLK_N	A39	B39	CSI0_DATA3_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A40	B40	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI1_CLK_P	A42	B42	CSI1_DATA0_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI1_CLK_N	A43	B43	CSI1_DATA0_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
I	1.8 V	DU	DU_DOT_CLK2_IN	A45	B45	CSI1_DATA1_P	CSI	1.8 V	I
–	0 V	Ground	DGND	A46	B46	CSI1_DATA1_N	CSI	1.8 V	I
I	1.8 V	DU	DU_DOT_CLK1_IN	A47	B47	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A48	B48	SDA4	I2C	1.8 V	IO
I	1.8 V	DU	DU_DOT_CLK0_IN	A49	B49	SCL4	I2C	1.8 V	O
–	0 V	Ground	DGND	A50	B50	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
O	3.3 V	LBSC	CLKOUT	A52	B52	RD_WR#	LBSC	3.3 V	O
–	0 V	Ground	DGND	A53	B53	BS#	LBSC	3.3 V	O
IO	3.3 V	IIC_DVFS	IIC_DVFS_SDA	A54	B54	WE0#	LBSC	3.3 V	O
O	3.3 V	IIC_DVFS	IIC_DVFS_SCL	A55	B55	WE1#	LBSC	3.3 V	O

3.1.3 TQMaRZG2x pinout (continued)

Table 5: Pinout connector X1 (continued)

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A56	B56	RD#	LBSC	3.3 V	O
O	3.3 V	GPIO	AVS1	A57	B57	CS1#	LBSC	3.3 V	O
O	3.3 V	GPIO	AVS2	A58	B58	CS0#	LBSC	3.3 V	O
IO	3.3 V	GPIO	GP7_03	A59	B59	EX_WAIT0_A	LBSC	3.3 V	I
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
O	3.3 V	LBSC	A0	A61	B61	D0	LBSC	3.3 V	IO
O	3.3 V	LBSC	A1	A62	B62	D1	LBSC	3.3 V	IO
O	3.3 V	LBSC	A2	A63	B63	D2	LBSC	3.3 V	IO
O	3.3 V	LBSC	A3	A64	B64	D3	LBSC	3.3 V	IO
O	3.3 V	LBSC	A4	A65	B65	D4	LBSC	3.3 V	IO
O	3.3 V	LBSC	A5	A66	B66	D5	LBSC	3.3 V	IO
O	3.3 V	LBSC	A6	A67	B67	D6	LBSC	3.3 V	IO
O	3.3 V	LBSC	A7	A68	B68	D7	LBSC	3.3 V	IO
O	3.3 V	LBSC	A8	A69	B69	D8	LBSC	3.3 V	IO
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
O	3.3 V	LBSC	A9	A71	B71	D9	LBSC	3.3 V	IO
O	3.3 V	LBSC	A10	A72	B72	D10	LBSC	3.3 V	IO
O	3.3 V	LBSC	A11	A73	B73	D11	LBSC	3.3 V	IO
O	3.3 V	LBSC	A12	A74	B74	D12	LBSC	3.3 V	IO
O	3.3 V	LBSC	A13	A75	B75	D13	LBSC	3.3 V	IO
O	3.3 V	LBSC	A14	A76	B76	D14	LBSC	3.3 V	IO
O	3.3 V	LBSC	A15	A77	B77	D15	LBSC	3.3 V	IO
O	3.3 V	LBSC	A16	A78	B78	DGND	Ground	0 V	–
O	3.3 V	LBSC	A17	A79	B79	IRQ0	INTC	3.3 V	I
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
O	3.3 V	LBSC	A18	A81	B81	IRQ1	INTC	3.3 V	I
O	3.3 V	LBSC	A19	A82	B82	IRQ2	INTC	3.3 V	I
–	0 V	Ground	DGND	A83	B83	IRQ3	INTC	3.3 V	I
I	3.3 V	INTC	IRQ5	A84	B84	IRQ4	INTC	3.3 V	I
O	3.3 V	PWM	PWM	A85	B85	DGND	Ground	0 V	–
O	3.3 V	PWM	PWM1_A	A86	B86	AVB_TXCREFCLK	EtherAVB	3.3 V	I
O	3.3 V	PWM	PWM2_A	A87	B87	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A88	B88	AVB_TX_CTL	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RXC	A89	B89	AVB_TXC	EtherAVB	2.5 V	O
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
I	2.5 V	EtherAVB	AVB_RX_CTL	A91	B91	AVB_TD0	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD0	A92	B92	AVB_TD1	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD1	A93	B93	AVB_TD2	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD2	A94	B94	AVB_TD3	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD3	A95	B95	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A96	B96	AVB_MDIO	EtherAVB	3.3 V	IO
O	3.3 V	EtherAVB	AVB_MAGIC	A97	B97	AVB_MDC	EtherAVB	3.3 V	O
I	3.3 V	EtherAVB	AVB_PHY_INT	A98	B98	DGND	Ground	0 V	–
I	3.3 V	EtherAVB	AVB_LINK	A99	B99	RPC_INT#	RPC	1.8 V	I
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
O	3.3 V	EtherAVB	AVB_AVTP_MATCH_A	A101	B101	RPC_WP#	RPC	1.8 V	O
I	3.3 V	EtherAVB	AVB_AVTP_CAPTURE_A	A102	B102	RPC_RESET#	RPC	1.8 V	O
–	0 V	Ground	DGND	A103	B103	DGND	Ground	0 V	–
O	1.8 V	QSPI	QSPI1_CLK_CON	A104	B104	QSPI0_CLK_CON	QSPI	1.8 V	O
IO	1.8 V	QSPI	QSPI1_IO0_CON	A105	B105	QSPI0_IO0_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO1_CON	A106	B106	QSPI0_IO1_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO2_CON	A107	B107	QSPI0_IO2_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO3_CON	A108	B108	QSPI0_IO3_CON	QSPI	1.8 V	IO
O	1.8 V	QSPI	QSPI1_SS#_CON	A109	B109	QSPI0_SS#_CON	QSPI	1.8 V	O
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.1.3 TQMaRZG2x pinout (continued)

Table 6: Pinout connector X2

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
I	0.8 V	PCIE	PCIE1_CLK_P	A2	B2	PCIE0_CLK_P	PCIE	0.8 V	I
I	0.8 V	PCIE	PCIE1_CLK_M	A3	B3	PCIE0_CLK_M	PCIE	0.8 V	I
–	0 V	Ground	DGND	A4	B4	DGND	Ground	0 V	–
O	0.8 V	PCIE	PCIE1_TX_P	A5	B5	PCIE0_TX_P	PCIE	0.8 V	O
O	0.8 V	PCIE	PCIE1_TX_M	A6	B6	PCIE0_TX_M	PCIE	0.8 V	O
–	0 V	Ground	DGND	A7	B7	DGND	Ground	0 V	–
I	0.8 V	PCIE	PCIE1_RX_P	A8	B8	PCIE0_RX_P	PCIE	0.8 V	I
I	0.8 V	PCIE	PCIE1_RX_M	A9	B9	PCIE0_RX_M	PCIE	0.8 V	I
–	0 V	Ground	DGND	A10	B10	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
O	0.8 V	USB 3.0	USB3S0_TX_P	A12	B12	USB3HS0_DP	USB 3.0	3.3 V	IO
O	0.8 V	USB 3.0	USB3S0_TX_M	A13	B13	USB3HS0_DM	USB 3.0	3.3 V	IO
–	0 V	Ground	DGND	A14	B14	DGND	Ground	0 V	–
I	0.8 V	USB 3.0	USB3S0_RX_P	A15	B15	USB3S0_CLK_P	USB 3.0	0.8 V	I
I	0.8 V	USB 3.0	USB3S0_RX_M	A16	B16	USB3S0_CLK_M	USB 3.0	0.8 V	I
–	0 V	Ground	DGND	A17	B17	DGND	Ground	0 V	–
IO	3.3 V	USB 2.0	DP1	A18	B18	DP0	USB 2.0	3.3 V	IO
IO	3.3 V	USB 2.0	DM1	A19	B19	DM0	USB 2.0	3.3 V	IO
–	0 V	Ground	DGND	A20	B20	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
I	3.3 V	USB 2.0	ID1	A22	B22	VBUS0	USB 2.0	5 V	I
O	3.3 V	USB 2.0	USB1_PWEN	A23	B23	ID0	USB 2.0	3.3 V	I
I	3.3 V	USB 2.0	USB1_OVC	A24	B24	USB0_PWREN	USB 2.0	3.3 V	O
I	5 V	USB 3.0	USB3HS0_VBUS	A25	B25	USB0_OVC	USB 2.0	3.3 V	I
I	3.3 V	USB 3.0	USB3HS0_ID	A26	B26	DGND	Ground	0 V	–
O	3.3 V	USB 3.0	USB30_PWEN	A27	B27	SD3_DAT3_CON	SD	1.8 / 3.3 V	IO
I	3.3 V	USB 3.0	USB30_OVC	A28	B28	SD3_DAT2_CON	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A29	B29	SD3_DAT1_CON	SD	1.8 / 3.3 V	IO
O	1.8 / 3.3 V	SD	SD3_CLK_CON	A30	B30	SD3_DAT0_CON	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
IO	1.8 / 3.3 V	SD	SD3_DAT7_CON	A32	B32	SD3_DS_CON	SD	1.8 / 3.3 V	I
IO	1.8 / 3.3 V	SD	SD3_DAT6_CON	A33	B33	SD3_CMD_CON	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD3_DAT5_CON	A34	B34	RTC_INT_OUT#	RTC	3.3 V	O
IO	1.8 / 3.3 V	SD	SD3_DAT4_CON	A35	B35	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A36	B36	TRST#	DBG	1.8 V	I
I	3.3 V	RTC	V_BAT	A37	B37	TDI	DBG	1.8 V	I
–	0 V	Ground	DGND	A38	B38	TMS	DBG	1.8 V	I
I	3.3 V	SYSC	SWD_CLK	A39	B39	ASEBRK	DBG	1.8 V	IO
IO	3.3 V	SYSC	SWD_DIO	A40	B40	TDO	DBG	1.8 V	O
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
O	3.3 V	RESET	TQM_RST_OUT#	A42	B42	TCK	DBG	1.8 V	I
I	3.3 V	RESET	TQM_RST_IN#	A43	B43	JTAG_SRST#	SYSC	3.3 V	I
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
O	3.3 V	SYSC	PGOOD	A45	B45	USB_EXTAL_CON	USB	1.8 V	I
O	3.3 V	SYSC	BOOT_CFG#	A46	B46	DGND	Ground	0 V	–
–	–	RESERVED	RFU0	A47	B47	SYSC_UART0_TX	SYSC	3.3 V	O
–	–	RESERVED	RFU1	A48	B48	SYSC_UART0_RX	SYSC	3.3 V	I
–	–	RESERVED	RFU2	A49	B49	DGND	Ground	0 V	–
I	1.8 V	INTC	NMI	A50	B50	EXTALR_CON	CPG	1.8 V	I
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
IO	3.3 V	GPIO	GP6_30	A52	B52	FSCLKST#	CPG	1.8 V	O
IO	3.3 V	GPIO	GP6_31	A53	B53	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A54	B54	AUDIO_CLKB_B	ADG	3.3 V	I
IO	3.3 V	SSI	SSI_SDATA9_A	A55	B55	DGND	Ground	0 V	–

3.1.3 TQMaRZG2x pinout (continued)

Table 6: Pinout connector X2 (continued)

Dir.	Level	Group	Signal	Pin	Pin	Signal	Group	Level	Dir.
IO	3.3 V	SSI	SSI_SDATA8	A56	B56	AUDIO_CLKA_A	ADG	3.3 V	I
IO	3.3 V	SSI	SSI_SDATA7	A57	B57	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA6	A58	B58	SSI_SCK5	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA5	A59	B59	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA4	A61	B61	SSI_SCK6	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA3	A62	B62	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA2_A	A63	B63	SSI_SCK78	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA1_A	A64	B64	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA0	A65	B65	SSI_SCK4	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_WS78	A66	B66	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS5	A67	B67	SSI_SCK349	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_WS6	A68	B68	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS4	A69	B69	SSI_SCK01239	SSI	3.3 V	IO
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS349	A71	B71	VDDQVA_SD0	SD	1.8 / 3.3 V	I
IO	3.3 V	SSI	SSI_WS01239	A72	B72	VDDQVA_SD1	SD	1.8 / 3.3 V	I
O	3.3 V	TEMP	TEMPSENSOR#	A73	B73	VDDQVA_SD2	SD	1.8 / 3.3 V	I
I	3.3 V	EEPROM	EEPROM_WP	A74	B74	VDDQVA_SD3	SD	1.8 / 3.3 V	I
O	3.3 V	SCIF	TX0	A75	B75	DGND	Ground	0 V	–
I	3.3 V	SCIF	RX0	A76	B76	SCK2	SCIF	3.3 V	O
IO	3.3 V	SCIF	CTS0#	A77	B77	DGND	Ground	0 V	–
IO	3.3 V	SCIF	RTS0#	A78	B78	TX2_A	SCIF	3.3 V	O
O	3.3 V	SCIF	SCK0	A79	B79	RX2_A	SCIF	3.3 V	I
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
O	3.3 V	SCIF	TX1_A	A81	B81	MLB_CLK	MLB	3.3 V	I
I	3.3 V	SCIF	RX1_A	A82	B82	MLB_DAT	MLB	3.3 V	IO
IO	3.3 V	SCIF	CTS1#	A83	B83	MLB_SIG	MLB	3.3 V	IO
IO	3.3 V	SCIF	RTS1#	A84	B84	HRTS0#	HSCIF	3.3 V	IO
IO	3.3 V	MSIOF	MSIOF0_SYNC	A85	B85	HCTS0#	HSCIF	3.3 V	IO
O	3.3 V	MSIOF	MSIOF0_TXD	A86	B86	HRX0	HSCIF	3.3 V	I
I	3.3 V	MSIOF	MSIOF0_RXD	A87	B87	HTX0	HSCIF	3.3 V	O
O	3.3 V	MSIOF	MSIOF0_SS1	A88	B88	DGND	Ground	0 V	–
O	3.3 V	MSIOF	MSIOF0_SS2	A89	B89	HSCK0	HSCIF	3.3 V	I
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
O	3.3 V	MSIOF	MSIOF0_SCK	A91	B91	SD1_DAT0	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A92	B92	SD1_DAT1	SD	1.8 / 3.3 V	IO
I	3.3 V	SD	SD0_WP	A93	B93	SD1_DAT2	SD	1.8 / 3.3 V	IO
I	3.3 V	SD	SD0_CD	A94	B94	SD1_DAT3	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD0_CMD	A95	B95	SD1_CD	SD	3.3 V	I
IO	1.8 / 3.3 V	SD	SD0_DAT0	A96	B96	SD1_WP	SD	3.3 V	I
IO	1.8 / 3.3 V	SD	SD0_DAT1	A97	B97	SD1_CMD	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD0_DAT2	A98	B98	DGND	Ground	0 V	–
IO	1.8 / 3.3 V	SD	SD0_DAT3	A99	B99	SD1_CLK	SD	1.8 / 3.3 V	O
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
O	1.8 / 3.3 V	SD	SD0_CLK	A101	B101	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A102	B102	SD2_DAT0	SD	1.8 / 3.3 V	IO
I	3.3 V	SECURE	SE_ENABLE	A103	B103	SD2_DAT1	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_7816_IO1	A104	B104	SD2_DAT2	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_7816_IO2	A105	B105	SD2_DAT3	SD	1.8 / 3.3 V	IO
I	3.3 V	SECURE	SE_7816_RST#	A106	B106	SD2_CMD	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_14443_LA	A107	B107	SD2_DS	SD	1.8 / 3.3 V	I
IO	3.3 V	SECURE	SE_14443_LB	A108	B108	DGND	Ground	0 V	–
O	3.3 V	SECURE	SE_7816_CLK	A109	B109	SD2_CLK	SD	1.8 / 3.3 V	O
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.1.4 Boot source and boot mode configuration

The MBaRZG2x supports the following TQMaRZG2x boot sources.

- eMMC (on TQMaRZG2x)
- QSPI NOR flash (on TQMaRZG2x)
- SCIF download mode via UART (X9)
- USB download mode via USB-OTG (X10)

A detailed description of the boot sources can be found in the TQMaRZG2x User's Manual.
The following figure shows the structure of the boot configuration:

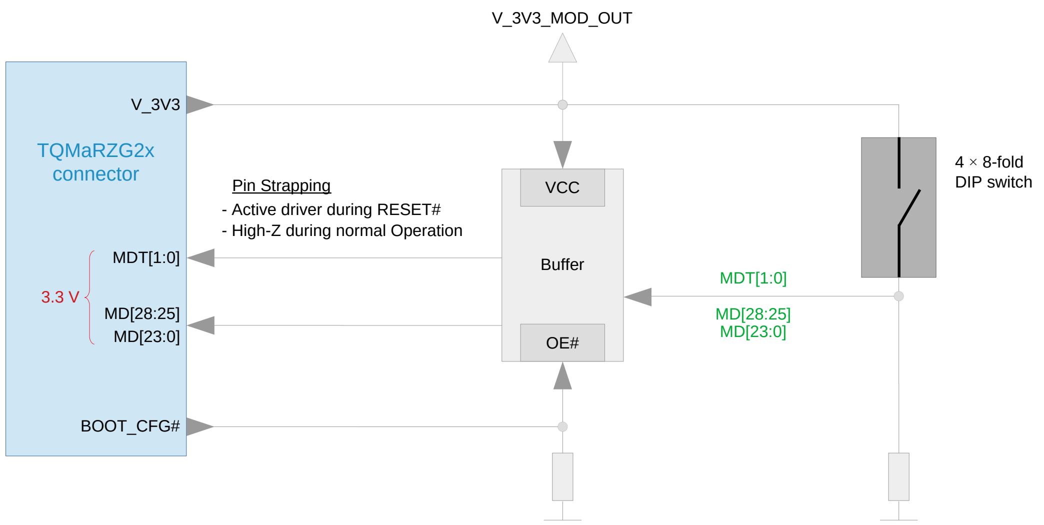


Figure 5: Block diagram boot mode and boot source setting

3.1.4 Boot source and boot mode configuration (continued)

The following table shows the permitted boot mode settings.
A "1" corresponds to a logic high level (3.3 V), a "0" corresponds to a logic low level (0 V):

Table 7: Boot mode configuration, DIP switch S2 to S5

DIP switch		Signal	TQMaRZG2x	eMMC	QSPI NOR	USB download	SCIF download
S5	1	MD_NC1	X31-3 [1]	–	–	–	–
	2	MD_NC2	X31-5 [1]	–	–	–	–
	3	MDT1	X1-B56	–	–	–	–
	4	MDT0	X1-B53	–	–	–	–
	5	MD28	X1-A61	1	1	1	1
	6	MD27	X1-A62	0	0	0	0
	7	MD26	X1-A64	0	0	0	0
	8	MD25	X1-A65	0	0	0	0
S4	1	MD23	X1-A67	0	0	0	0
	2	MD22	X1-A68	0	0	0	0
	3	MD21	X1-A74	–	–	–	–
	4	MD20	X1-A72	–	–	–	–
	5	MD19	X1-A75	0	0	0	0
	6	MD18	X1-A76	0	0	0	0
	7	MD17	X1-A77	0	0	0	0
	8	MD16	X1-A78	1	1	1	1
S3	1	MD15	X1-A79	1	1	1	1
	2	MD14	X1-A81	1	1	1	1
	3	MD13	X1-A82	0	0	0	0
	4	MD12	X1-B69	– [2]	– [2]	– [2]	– [2]
	5	MD11	X1-B65	–	–	–	–
	6	MD10	X1-B75	–	–	–	–
	7	MD9	X1-B74	1	1	1	1
	8	MD8	X1-B73	–	–	–	–
S2	1	MD7	X1-B72	0	0	0	0
	2	MD6	X1-B71	0	0	0	0
	3	MD5	X1-B68	1	1	1	1
	4	MD4	X1-B67	1	0	1	1
	5	MD3	X1-B66	1	1	1	1
	6	MD2	X1-B64	0	0	1	1
	7	MD1	X1-B63	1	0	0	1
	8	MD0	X1-B62	0	0	0	0

1: X31 on MBaRZG2x.
2: RZ/G2M = 0 (fixed); RZ/G2H or RZ/G2N = don’t care.

3.1.5 Reset structure

The MBaRZG2x provides several options to completely or partially reset the TQMaRZG2x.
With the PGOOD signal coming from the TQMaRZG2x and the design of the MBaRZG2x the correct power sequencing is ensured.

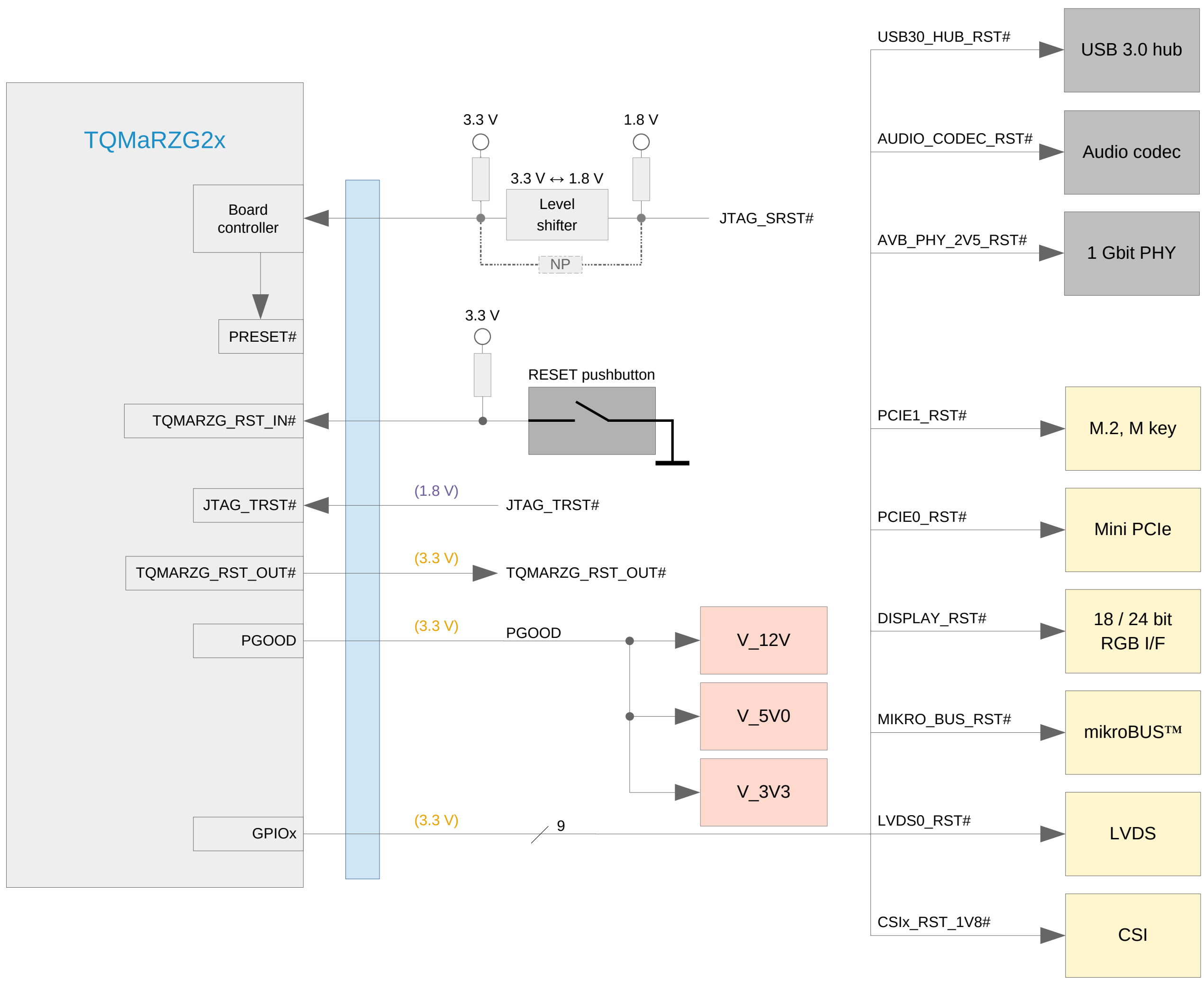


Figure 6: Block diagram Reset structure

3.1.5 Reset structure (continued)

The following TQMaRZG2x signals are used on the MBaRZG2x:

Table 8: Reset and Power Sequencing signals

Signal	Dir.	Level	Description
TQMARZG_RST_IN#	I	3.3 V	– Activates RESET of the RZ/G2x (low-active) – No pull-up on mainboard necessary – Pull low to activate (pushbuttons)
TQMARZG_RST_OUT#	O	3.3 V	– Serves the mainboard as status signal (CPU still in reset) – State is signalled by a red LED
JTAG_TRST#	I	1.8 V	– Is directly connected to the TRST# of the RZ/G2x – Pull-up after 1.8 V – Pull low to activate
JTAG_SRST#	I	3.3 V	– Activates PRESET of the RZ/G2x (low-active) via board controller – Voltage shifter required – Pull-up on mainboard necessary – Pull low to enable
PGOOD	O	3.3 V	– Activates Enable of the power supplies – Pull-down on mainboard necessary – To enable with high level from module
GPIOx	O	1.8 V 2.5 V 3.3 V	– Activates RESET of some components on MBaRZG2x and other interfaces – Pull low to activate

Attention: MBaRZG2x destruction or malfunction, Power-Up sequence	
⚠	To avoid cross-supplies and errors in the power-up sequence of the MBaRZG2x, no I/O pins may be externally supplied or driven until the power-up sequence of the I/O voltages on the MBaRZG2x is completed. At the same time, the carrier board component supply voltages must be stable. A high level of PGOOD indicates the successful completion of the power-up sequence.

3.1.6 Clocks

To use the interfaces of the MBaRZG2x, the CPU needs different clocks. These are generated by a clock device on the MBaRZG2x. The clock device is configured in the BSP via I2C4. Each output can be configured separately via I2C4.
The following figure shows the clock supply structure.

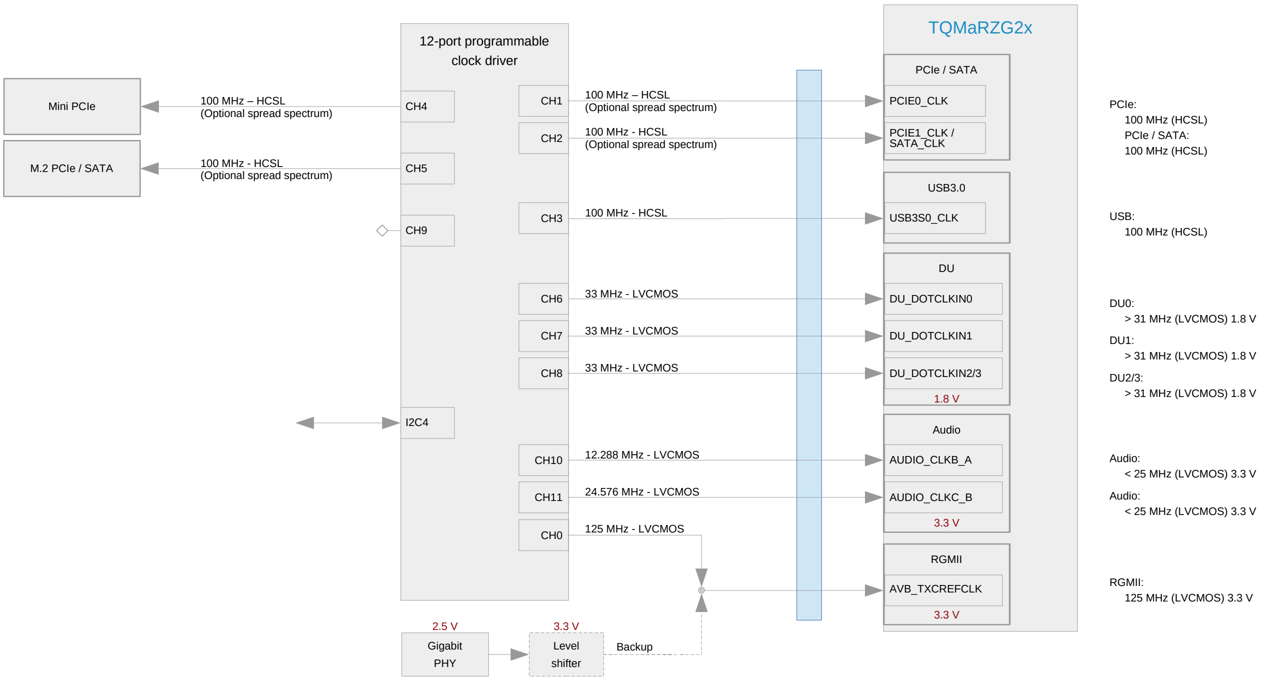


Figure 7: Clocks for TQMaRZG2x and MBaRZG2x

3.1.7 I²C devices

The RZ/G2x provides various I²C buses. I2C4, I2C6 and IIC_DVFS are routed to different headers, connectors and devices on the MBaRZG2x, but only I2C4 is used on the MBaRZG2x. The following block diagram shows the I²C bus structure.

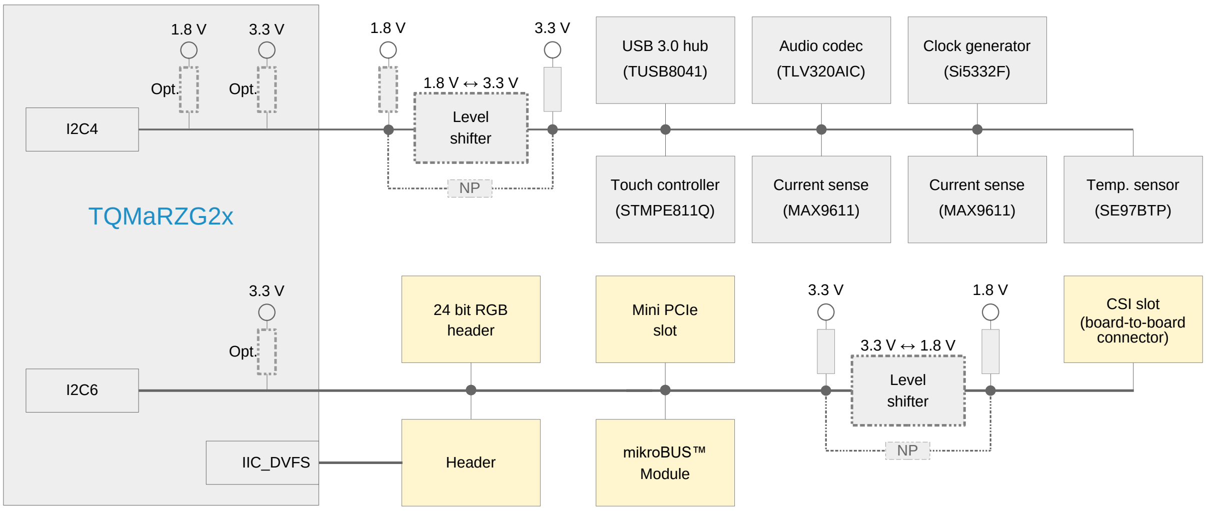


Figure 8: Block diagram I2C bus

The I²C device addresses used on the TQMaRZG2x were taken into account when I²C addresses were assigned to the devices on the MBaRZG2x. The following table shows the I²C address mapping on TQMaRZG2x and MBaRZG2x.

Table 9: I²C devices, address mapping on TQMaRZG2x and MBaRZG2x

Location	I²C bus	Device	Function	7-bit address	Remark
MBaRZG2x	I2C4	SI5332F	Clock generator	`0x6A / 110 1010b`	D1
		TUSB8041	USB 3.0 hub	`0x44 / 100 0100b`	D13
		STMPE811Q	Touch controller	`0x41 / 100 0001b`	D21
		SE97BTP	Temp. sensor	`0x1F / 001 1111b`	D22, temperature registers
		SE97BTP	EEPROM	`0x57 / 101 0111b`	D22, R/W in Normal Mode
		SE97BTP	EEPROM	`0x37 / 011 0111b`	D22, R/W in Protected Mode
		TLV320AIC	Audio codec	`0x18 / 001 1000b`	N13
		MAX9611	Current sense	`0x7D / 111 1101b`	N19, current sense V_5V0_MOD
		MAX9611	Current sense	`0x70 / 111 0000b`	N20, current sense V_24
	I2C6	Header	24 bit RGB	–	X12, device dependent
		mPCIe	Mini PCIe	–	X28, device dependent
		mikroBUS™	mikroBUS™	–	D12, device dependent
		Connector	CSI	–	X21, device dependent
		Header	Expansion	–	X35, device dependent
	IIC_DVFS	Header	Expansion	–	X35, device dependent
TQMaRZG2x		MKL04Z16	System controller	`0x11 / 001 0001b`	Should not be altered
		PCF85063	RTC	`0x51 / 101 0001b`	–
		SE97BTP	Temp. sensor	`0x1F / 001 1111b`	Temperature registers
		SE97BTP	EEPROM	`0x57 / 101 0111b`	R/W in Normal Mode
		SE97BTP	EEPROM	`0x37 / 011 0111b`	R/W in Protected Mode
		24LC256T	EEPROM	`0x50 / 101 0000b`	–
		SE050	TSE	`0x48 / 100 1000b`	–

3.2 Power supply

3.2.1 Supply structure

The MBaRZG2x has to be supplied with 16 V to 30 V (nominal 24 V) at X5 or X6, which are switched in parallel.
The following terminals are used on the MBaRZG2x:

- DC socket 2.5 mm/5.5 mm: Cui Stack / PJ-102BH
- 2-pin screw terminal: Lumberg / KRM2

The signal PGOOD is used to control the respective rails and to comply with the power sequencing.
On the MBaRZG2x the supply is divided into two parts:

1. Standby Power Supply (V_5V0_MOD, V_3V3_SYSC).
   - Permanently activated
   - Module supply / Reset button / LED

2. Switched Power Supply (V_12V, V_5V0, V_3V3)
   - Supply of the periphery
   - Switched by PGOOD
   - Switched off in standby mode

The following figure shows all voltages present on the MBaRZG2x, which are structured into three main paths consisting of a 12 V, 5 V, and a 3.3 V supply rail.

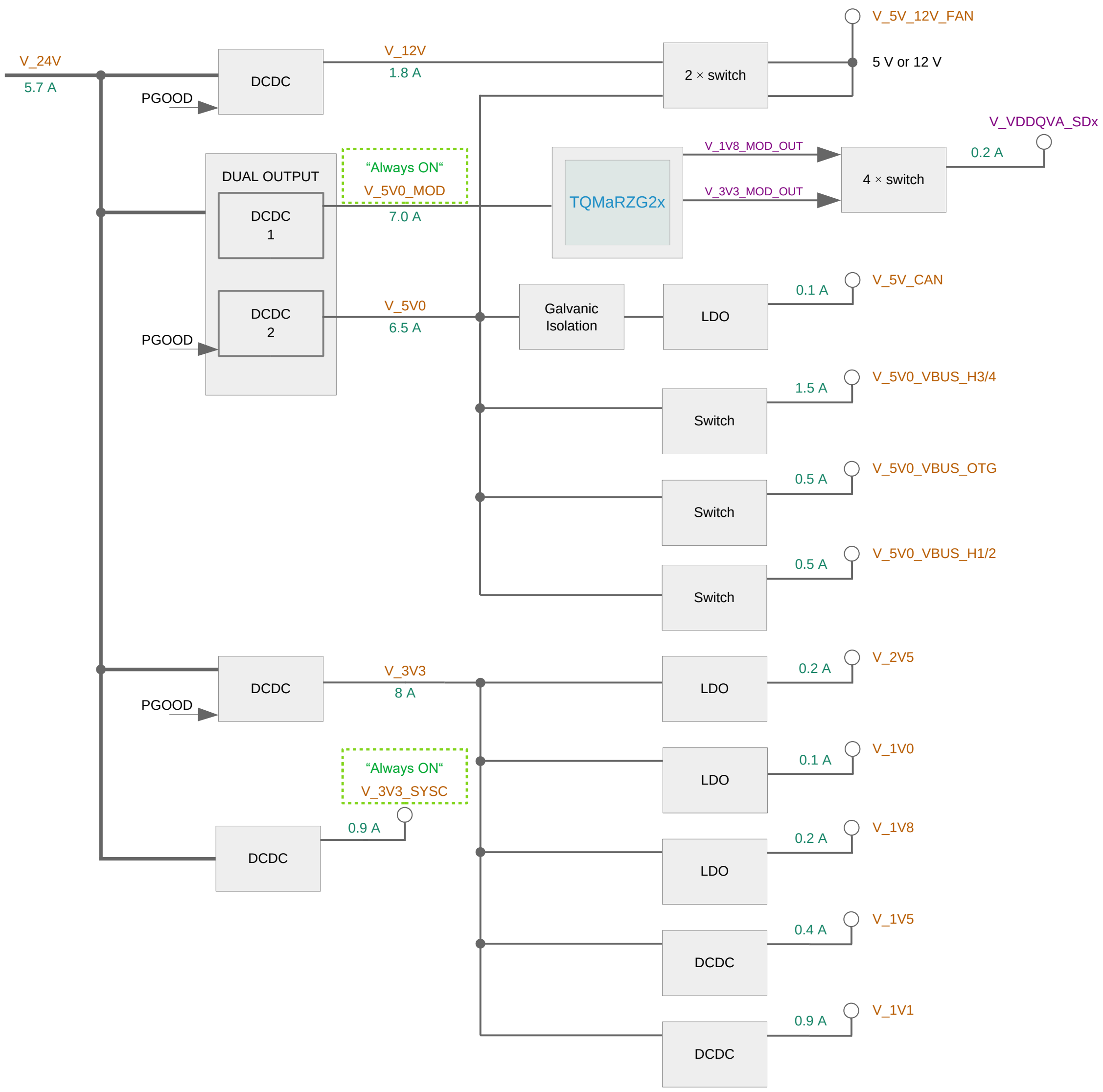


Figure 9: Block diagram power supply

3.2.2 Protective circuitry

The protection circuit (see Figure 10) features the following characteristics:

- Overcurrent protection by fuse 7 A, slow blow
- Overvoltage protection diode
- PI filter
- Reverse polarity protection by MOSFET

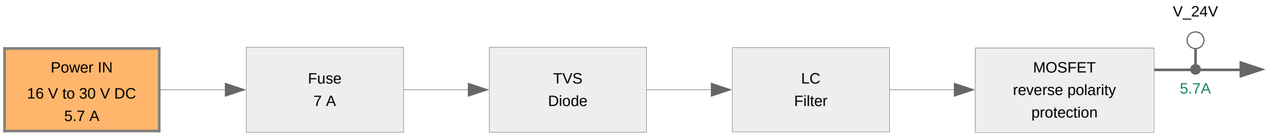


Figure 10: Block diagram protective circuit

The MBaRZG2x including the TQMaRZG2x may consume significantly more power when all supply rails are loaded with maximum current, e.g. by connecting external loads to the pin headers, connectors and interfaces on the MBaRZG2x.
The power supply used must be designed accordingly.

Attention: MBaRZG2x overcurrent protection	
⚠	All voltages provided at the MBaRZG2x pin headers are not short-circuit proof and are not protected by separate fuses. Technically it is possible to overload the main fuse. The resulting total current consumption of the MBaRZG2x must be observed and complied with.

The following current limits apply to the different supply voltages:

Table 10: Supply voltages, current limits

Voltage	Maximum current	Absolute limit
V_12V	2 A	4.7 A
V_5V0	6.5 A	–
V_5V0_MOD	7 A	9.4 A
V_5V0_VBUS_H1+H2	0.9 A	1.4 A
V_5V0_VBUS_H3+H4	0.9 A	1.1 A
V_5V0_VBUS_OTG	0.5 A	0.5 A
V_5V_CAN	0.1 A	0.1 A
V_3V3	8 A	14 A
V_3V3_SYSC	0.9 A	1 A
V_2V5	0.5 A	–
V_1V8	0.5 A	–
V_1V5	1 A	2.8 A
V_1V1	1.5 A	2.8 A
V_1V0	0.5 A	–

3.2.3 Battery

A battery type CR2032 on the MBaRZG2x in socket X25 supplies the RTC on the TQMaRZG2x via pin V_BAT, X2-A37.
Alternatively, V_BAT can also be supplied via X24 on the MBaRZG2x. The battery voltage range is 2.1 V to 3.7 V, nominal 3 V.
By default, X24 is not populated.

3.3 Data interfaces

3.3.1 Mini PCIe socket, SIM card socket

The MBaRZG2x provides a Mini PCIe slot with one PCIE lane (×1) for full-size cards (50.95 mm × 30 mm).
Any standard compliant Mini PCIe card can be used. A SIM card holder is also provided.
The clocks for CPU and the Mini PCIe card are generated by a discrete clock generator.

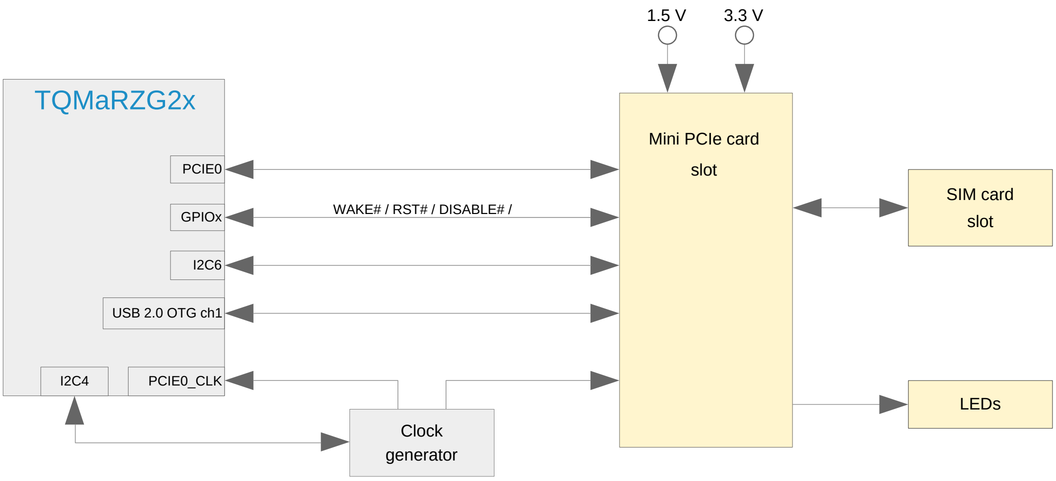


Figure 11: Block diagram Mini PCIe, SIM card

The voltages provided for the Mini PCIe card must not exceed the currents specified in the following table.

Table 11: Maximum permitted currents Mini PCIe X28

Voltage	Nominal value	I_{max}
V_3V3_PCIE	3.3 V	1.1 A
V_1V5_PCIE	1.5 V	0.375 A

Table 12: Pinout SIM card connector X37

Pin	Signal
C1	V_SIM_PWR
C2	SIM_RST
C3	SIM_CLK
C4	(NC)
C5	DGND
C6	SIM_VPP
C7	SIM_DATA
C8	(NC)
DC	SIM_CARD_DETECT
DS	DGND

3.3.1 Mini PCIe socket, SIM card socket (continued)

Table 13: Pinout Mini PCIe X28

Remark	Signal	Pin	Pin	Signal	Remark
–	PCIE0_WAKE#	1	2	V_3V3_MPCIE	–
–	(NC)	3	4	DGND	–
–	(NC)	5	6	V_1V5_MPCIE	–
–	(NC)	7	8	V_SIM_PWR	–
–	DGND	9	10	SIM_DATA	–
Signal from Clock Generator	PCIE0_CLK_M	11	12	SIM_CLK	–
Signal from Clock Generator	PCIE0_CLK_P	13	14	SIM_RST	–
–	DGND	15	16	SIM_VPP	–
Key notch					
–	(NC)	17	18	DGND	–
–	(NC)	19	20	PCIE0_DISABLE#	10 kΩ PU/PD, default: 10 kΩ PD
–	DGND	21	22	PCIE0_RST#	10 kΩ PU/PD, default: 10 kΩ PD
0 Ω in series	PCIE0_RX_M	23	24	V_3V3_MPCIE	–
0 Ω in series	PCIE0_RX_P	25	26	DGND	–
–	DGND	27	28	V_1V5_MPCIE	–
–	DGND	29	30	I2C6_SCL	–
100 nF in series	PCIE0_TX_M	31	32	I2C6_SDA	I^2C addresses; see Table 9
100 nF in series	PCIE0_TX_P	33	34	DGND	–
–	DGND	35	36	DM1	–
–	DGND	37	38	DP1	–
–	V_3V3_MPCIE	39	40	DGND	–
–	V_3V3_MPCIE	41	42	WWAN-LED	–
–	DGND	43	44	WLAN-LED	–
–	(NC)	45	46	WPAN-LED	–
–	(NC)	47	48	V_1V5_MPCIE	–
–	(NC)	49	50	DGND	–
–	(NC)	51	52	V_3V3_MPCIE	–

3.3.2 M.2, M key (SSD SATA)

The RZ/G2x provides two PCIe 2.0 compliant controllers with integrated PHYs. With the RZ/G2H and RZ/G2N derivatives, one of the two PCIe controllers can be used as a SATA interface. PCIE1 is provided on the MBaRZG2x as M.2 with M key (X22). The MBaRZG2x supports M.2 sizes 2242 and 2280. The standard mounting is for type 2280. DIP switch S10-1 on the MBaRZG2x toggles between PCIe and SATA. The clocks for CPU and the PCIe interface are generated by a discrete clock generator.

Table 14: Pinout M.2, M key X22

Signal	Pin	Pin	Signal
M2_CONFIG_3	1	2	3V3
GND	3	4	3V3
(NC)	5	6	(NC)
(NC)	7	8	(NC)
GND	9	10	DAS / DSS#
(NC)	11	12	3V3
(NC)	13	14	3V3
GND	15	16	3V3
(NC)	17	18	3V3
(NC)	19	20	(NC)
M2_CONFIG_0	21	22	(NC)
(NC)	23	24	(NC)
(NC)	25	26	(NC)
GND	27	28	(NC)
(NC)	29	30	(NC)
(NC)	31	32	(NC)
GND	33	34	(NC)
(NC)	35	36	(NC)
(NC)	37	38	DEVSLP
GND	39	40	(NC)
PCIE1_SATA_RX_M [3]	41	42	(NC)
PCIE1_SATA_RX_P [3]	43	44	(NC)
GND	45	46	(NC)
PCIE1_SATA_TX_M	47	48	(NC)
PCIE1_SATA_TX_P	49	50	PCIE1_RST#
GND	51	52	PCIE1_CLK_REQ#
PCIE1_CLK_M	53	54	PCIE1_WAKE#
PCIE1_CLK_P	55	56	(NC)
GND	57	58	(NC)
	M key	M key	
	M key	M key	
	M key	M key	
	M key	M key	
(NC)	67	68	SUSCLK
M2_CONFIG_1	69	70	3V3
GND	71	72	3V3
GND	73	74	3V3
M2_CONFIG_2	75		

3: RX pair is crossed due to the M.2 specification.

3.3.3 microSD card

The RZ/G2x provides four SDHC interfaces. On the MBaRZG2x SDHI0 is connected with 4 bit to the microSD card socket.
The microSD card can be used as boot media.

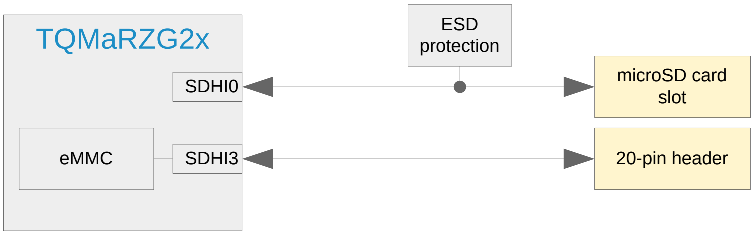


Figure 12: Block diagram microSD card

Table 15: Pinout microSD card X29

Pin	Signal	Remark
1	SD0_DATA2	10 kΩ PU to 3.3 V + ESD protection
2	SD0_DATA3	10 kΩ PU to 3.3 V + ESD protection
3	SD0_CMD	10 kΩ PU to 3.3 V + ESD protection
4	VCC3V3	–
5	SD0_CLK	ESD protection
6	DGND	–
7	SD0_DATA0	10 kΩ PU to 3.3 V + ESD protection
8	SD0_DATA1	10 kΩ PU to 3.3 V + ESD protection
SW1	SD0_CD#	10 kΩ PU to 3.3 V + ESD protection
SW2	DGND	–

Note: microSD card supply voltage	
	microSD cards always start with 3.3 V I/O voltage after power-up. The software automatically switches to 1.8 V I/O voltage if required by the mode. When rebooting or resetting the MBaRZG2x, the microSD card remains at the last I/O voltage used because it does not have a separate reset signal. The SDHC controller, on the other hand, returns to 3.3 V I/O voltage.

3.3.4 Gbit Ethernet

The RZ/G2x provides an RGMII compliant Ethernet AVB interface (audio video bridging). On the MBaRZG2x, the Ethernet Gigabit interface is provided via an RGMII PHY on an RJ-45 socket. The IO voltage of the RGMII signals is 2.5 V. The auxiliary signals (reset, interrupt...) operate with 3.3 V. The reference clock for the CPU is generated by a discrete clock generator.

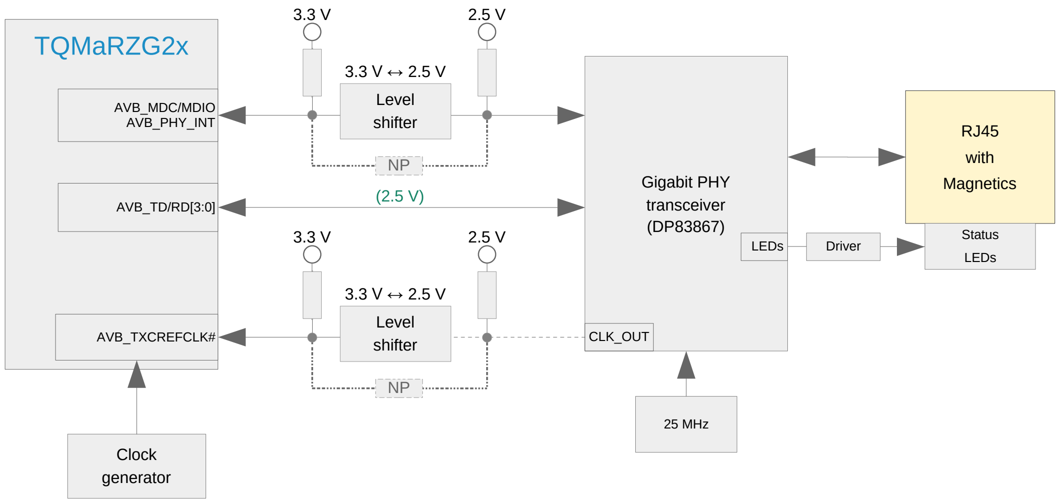


Figure 13: Block diagram Gbit Ethernet

3.3.5 USB 2.0 OTG

The RZ/G2x provides two USB 2.0 controllers with integrated PHY, which are also OTG capable.
USB0 is routed to a USB Micro AB connector on the MBaRZG2x. The USB port is ESD protected and secured against overload.
USB0 can be used for USB download mode; see chapter 3.1.4.

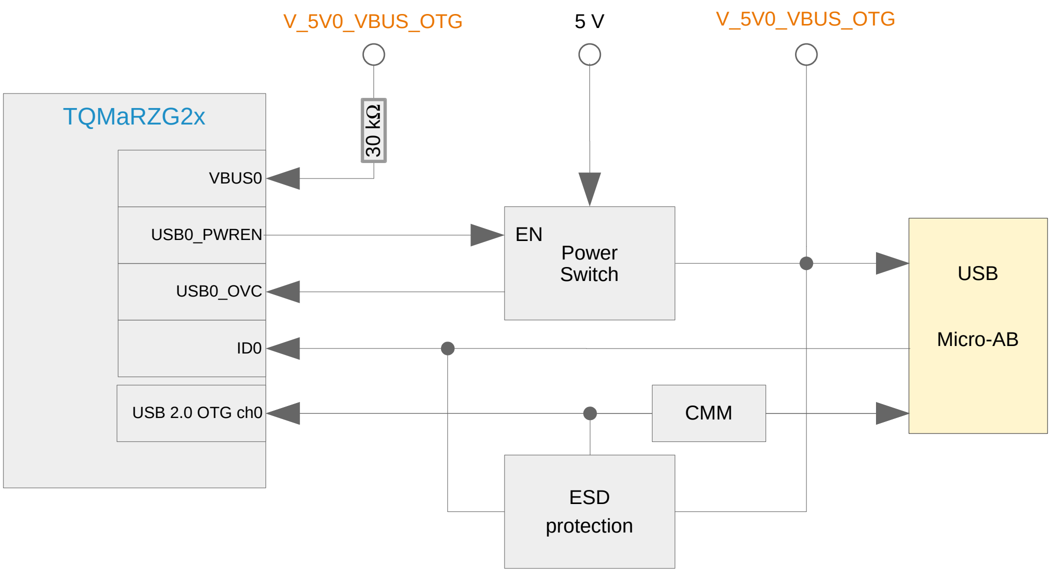


Figure 14: Block diagram USB 2.0 OTG

3.3.6 USB 3.0 hub

The TI USB 3.0 hub TUSB8041 on the MBaRZG2x, which is connected to the USB 3.0 port of the TQMaRZG2x, provides four USB host ports. Optionally the TUSB8041 can be programmed via I2C4, address `0x44 / 100 0100b`; see also Table 9. However, this option is disabled by default. Information on enabling this function can be found in the MBaRZG2x schematics.

On the MBaRZG2x two ports (USB host1&2) are routed as USB 3.0 interfaces to a stacked USB Type A connector (X11).

USB host1 is routed to the upper USB Type A connector, USB host2 is routed to the lower USB Type A connector.

USB host3 is routed as USB 2.0 to the RGB connector X12, USB host4 is routed as USB 2.0 to the LVDS control connector X20.

The following speed types are supported: SuperSpeed (5 Gbps), High Speed (480 Mbps), Full Speed, Low Speed (host only).

The USB 3.0 port of the TQMaRZG2x provides a theoretical data rate of 5 Gbit/s. This is divided among the connected ports.

Depending on the software and hardware used, the effective read and write rates of the ports may vary.

Power distribution switches provide 5 V for the USB connectors. The current is monitored and automatically switched off in case of overload and/or overheating.

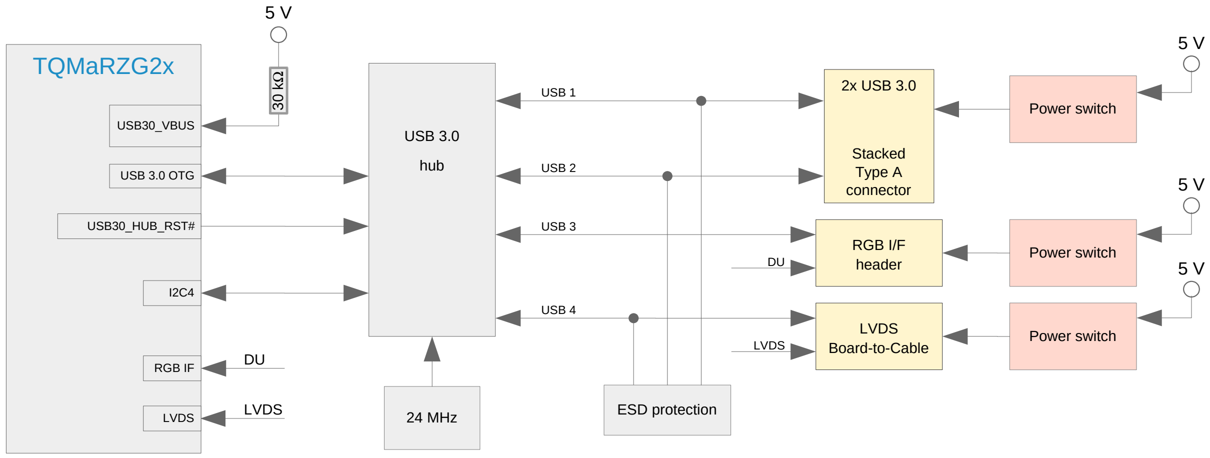


Figure 15: Block diagram USB 3.0 hub

3.3.7 UART to USB

The RZ/G2x provides several UARTs. On the MBaRZG2x two of the UARTs are routed via a TTL-USB bridge to a USB Micro AB connector. The bridge is supplied via VBUS (USB powered) as soon as a connection with the remote terminal (e.g. PC) is established. This enables communication with the TQMaRZG2x via USB.

Alternatively the SCIF0 can be switched to header X33 on the MBaRZG2x.

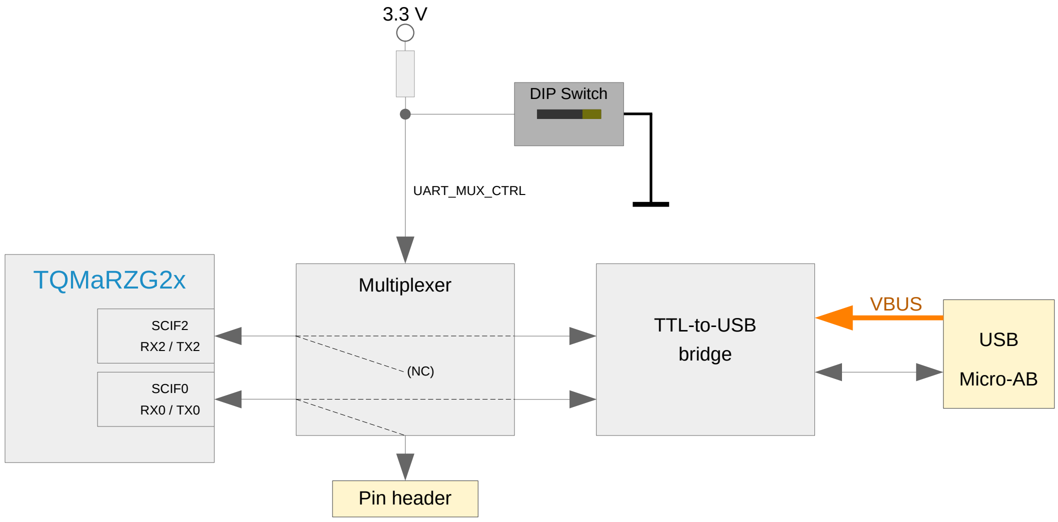


Figure 16: Block diagram Debug USB

The following table shows the function of DIP switch S10-4.

Table 16: DIP switch S10-4

DIP switch	ON	OFF
[4] 7~8	SCIF0 (UART0) on USB X9	SCIF0 (UART0) on header X33
	SCIF2 (UART2) on USB X9	(NC)

3.3.8 Audio

The RZ/G2x provides up to 10 SSI (Serial Sound Interface). On the MBaRZG2x one SSI is routed to an audio codec.
The following interfaces are available on the MBaRZG2x:

- 1 × Mic
- 1 × Line-in (Stereo)
- 1 × Line-out (Stereo)

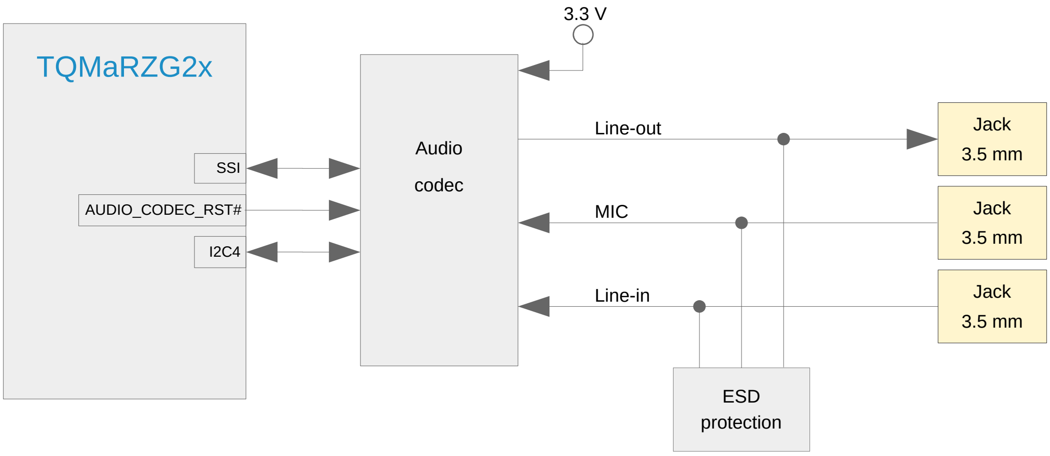


Figure 17: Block diagram Audio interface

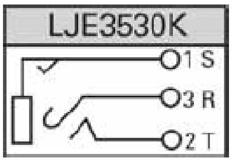


Figure 18: Signals on 3.5 mm audio jacks

The following table shows the pinout of the audio connectors on the MBaRZG2x:

Table 17: Pinout audio connectors X15 X16, X17

Channel	Pin	Signal	Dir.	Level	Remark
MIC (X15)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	MIC_IN_L	A_I	0.9 V	Mic left (Mono)
	3	MIC_IN_R	A_I	0.9 V	Mic right (not used ⇨ pull-down to AGND_AUD)
Line-In (X16)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	LINE_IN_L	A_I	1.65 V	Line-In left
	3	LINE_IN_R	A_I	1.65 V	Line-In right
Line-Out (X17)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	LINE_OUT_L	A_O	1.65 V	Line-Out left
	3	LINE_OUT_R	A_O	1.65 V	Line-Out right

3.3.9 CAN

Two ISO-11898 compliant CAN FD interfaces are provided on two 3-pin shrouded headers on the MBaRZG2x.
The interfaces are galvanically isolated, but not among each other. The High-Speed Mode supports data rates of up to 5 Mbit/s.

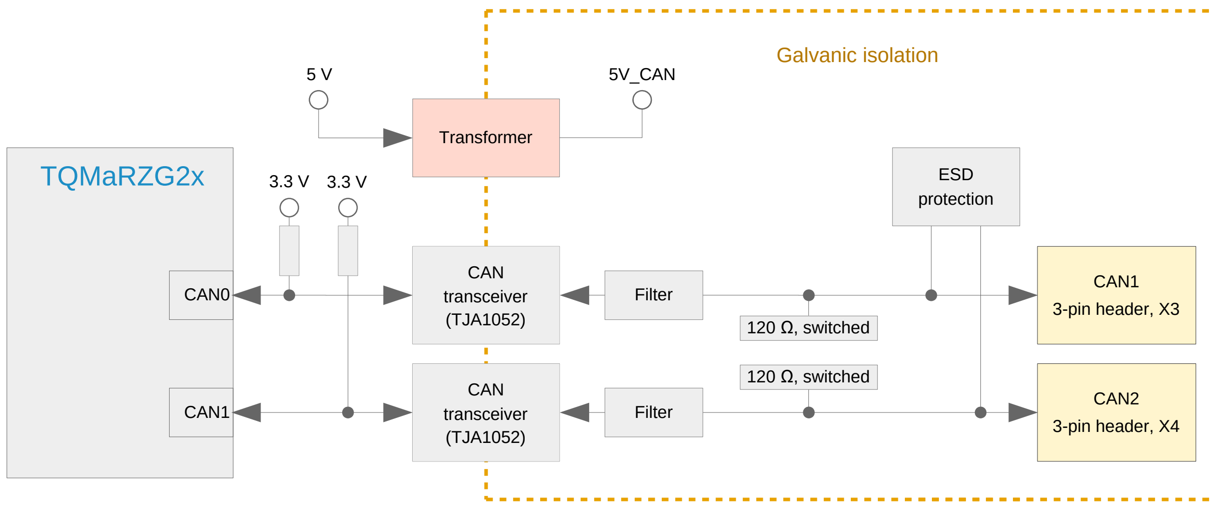


Figure 19: Block diagram CAN

The following table shows the pinout of the CAN connectors.

Table 18: Pinout CAN X3, X4

CAN bus	Connector	Pin	Signal	Direction	Remark
CAN1	X3	1	CAN1_H	I/O	Galvanically separated within MBaRZG2x
		2	CAN1_L	I/O	
		3	GND_CAN	–	
CAN2	X4	1	CAN2_H	I/O	
		2	CAN2_L	I/O	
		3	GND_CAN	–	

The CAN signals can be terminated with 120 Ω using the DIP switches S1-1 & S1-2

Table 19: CAN termination, DIP switch S1

DIP switch	Interface	ON	OFF
[1] 1~2	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated
[2] 3~4	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated

3.3.10 HDMI

The RZ/G2x provides an HDMI interface. On the MBaRZG2x, the HDMI interface is routed on an HDMI Type A connector.
ESD requirements are met by an HDMI companion chip.

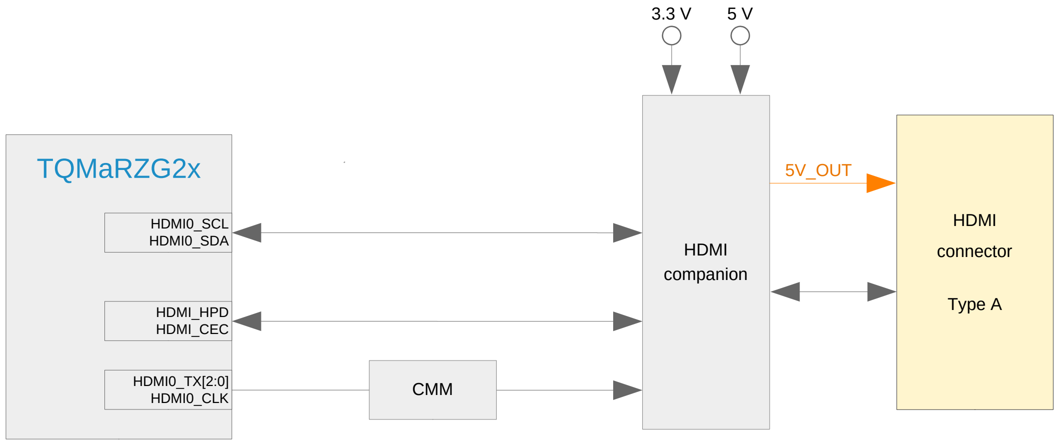


Figure 20: Block diagram HDMI

HDMI0_SCL and HDMI0_SDA operate at 1.8 V and are 3.3 V tolerant. MBaRZG2x boards < Rev. 100 were equipped with a level shifter.

3.3.11 LVDS

The RZ/G2x provides an LVDS interface. On the MBaRZG2x the LVDS interface is routed on an FPC connector.
The LVDS control signals are routed to a second FPC connector.

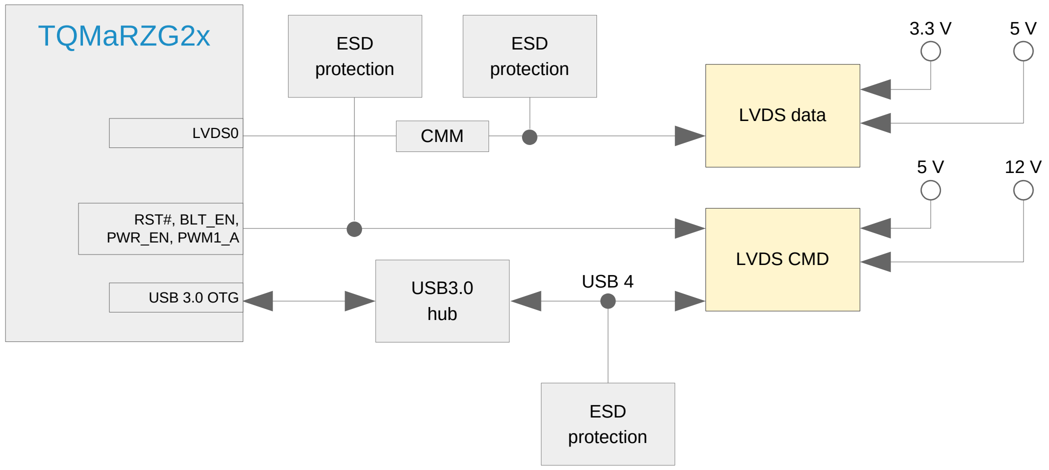


Figure 21: Block diagram LVDS

3.3.11 LVDS (continued)

Table 20: Pinout LVDS data signal connector X19

Pin	Signal	Remark
1	LVDS0_CH0_TX_M	Common Mode Choke in series + ESD protection
2	LVDS0_CH0_TX_P	Common Mode Choke in series + ESD protection
3	LVDS0_CH1_TX_M	Common Mode Choke in series + ESD protection
4	LVDS0_CH1_TX_P	Common Mode Choke in series + ESD protection
5	LVDS0_CH2_TX_M	Common Mode Choke in series + ESD protection
6	LVDS0_CH2_TX_P	Common Mode Choke in series + ESD protection
7	DGND	–
8	LVDS0_CLK_M	Common Mode Choke in series + ESD protection
9	LVDS0_CLK_P	Common Mode Choke in series + ESD protection
10	LVDS0_CH3_TX_M	Common Mode Choke in series + ESD protection
11	LVDS0_CH3_TX_P	Common Mode Choke in series + ESD protection
12	(NC)	–
13	(NC)	–
14	DGND	–
15	(NC)	–
16	(NC)	–
17	DGND	–
18	(NC)	–
19	(NC)	–
20	(NC)	–
21	(NC)	–
22	(NC)	–
23	(NC)	–
24	DGND	–
25 … 27	V_5V0_LVDS0	5 V, max. 1 A
28 … 30	V_3V3_LVDS0	3.3 V, max. 1 A
M1, M2	DGND	–

Table 21: Pinout LVDS control signal connector X20

Pin	Signal	Remark
1 … 3	V_12V_LVDS0	12 V, max. 1 A
4 … 6	DGND	–
7 … 8	V_5V0_LVDS0	5 V, max. 1 A
9 … 10	DGND	–
11	VBUS0_H4	ESD protection
12	DGND	–
13	USB0_H4_DM	Common Mode Choke in series + ESD protection
14	USB0_H4_DP	Common Mode Choke in series + ESD protection
15	DGND	–
16	LVDS0_RST#	ESD protection
17	LVDS0_BLT_EN	ESD protection
18	LVDS0_PWR_EN	ESD protection
19	LVDS0_PWM1_A	ESD protection
20	DGND	–
M1, M2	DGND	–

3.3.12 RGB

The Display Unit (DU) of the RZ/G2x provides a digital RGB interface through the VSP (Video Signal Processor).
On the MBaRZG2x this interface is made available as 18/24-bit RGB interface. DIP switch S11 toggles between 18 and 24 bit.
In addition to the RGB interface, further CPU signals, e.g. for a touch controller or display control, are also routed to this header.

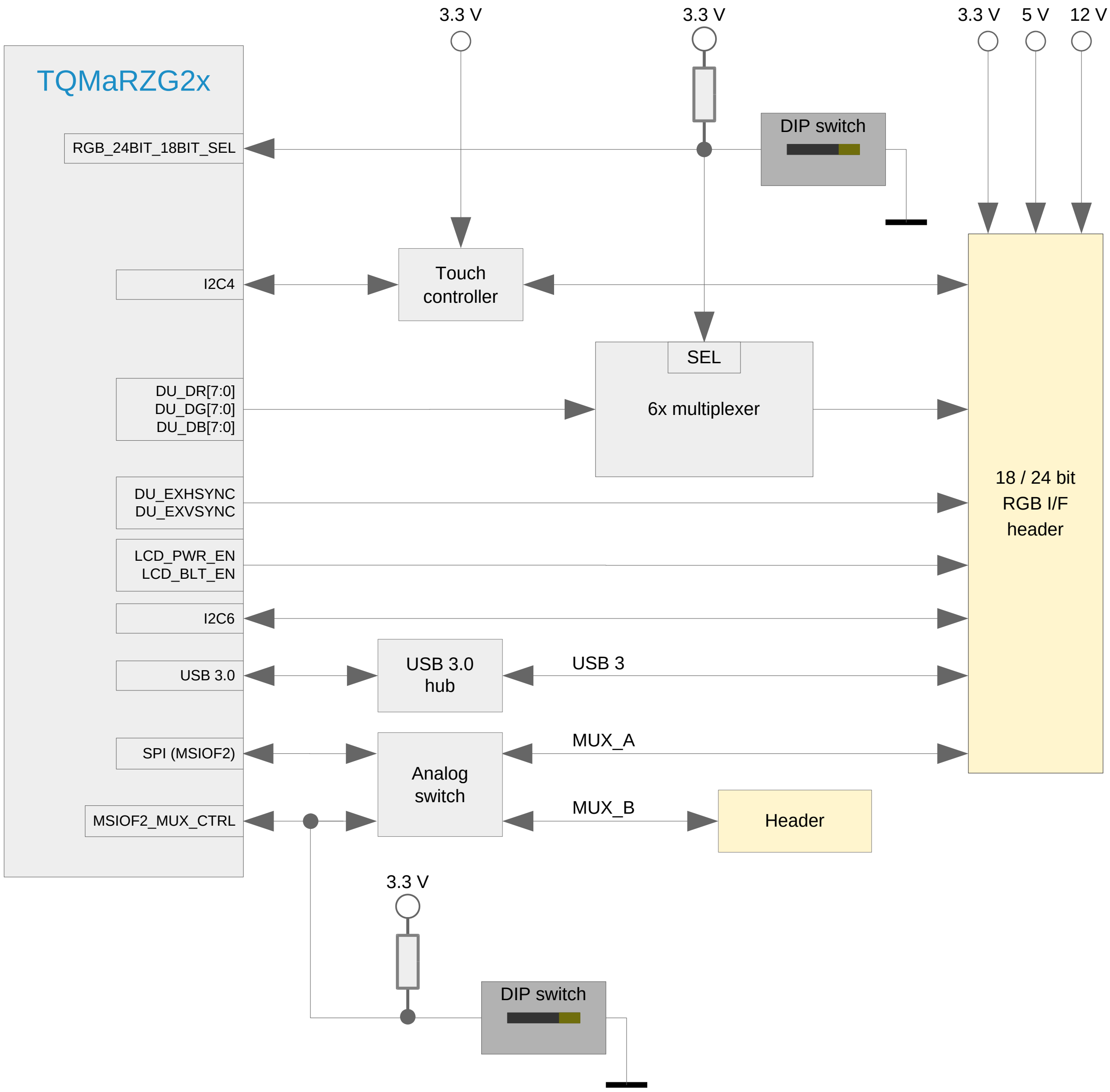


Figure 22: Block diagram RGB

3.3.12 RGB (continued)

Table 22: Pinout header X12

Signal	24 bit	18 bit	Pin	Pin	18 bit	24 bit	Signal
V_12V_DISP	–	–	1	2	–	–	V_3V3_DISP
V_5V0_DISP	–	–	3	4	–	–	V_3V3_DISP
DGND	–	–	5	6	–	–	DGND
DU_DOTCLKOUT1	–	–	7	8	–	–	DU_EXODDF
DU_EXHSYNC	–	–	9	10	B1	B1	DU_DB1_MUX
DU_EXVSYNC	–	–	11	12	B3	B3	DU_DB3_MUX
DU_DB0_MUX	B0	B0	13	14	B5	B5	DU_DB5_MUX
DU_DB2_MUX	B2	B2	15	16	G1	B7	DU_DB7_MUX
DU_DB4_MUX	B4	B4	17	18	G3	G1	DU_DG1_MUX
DU_DB6_MUX	B6	G0	19	20	G5	G3	DU_DG3_MUX
DU_DG0_MUX	G0	G2	21	22	R1	G5	DU_DG5_MUX
DU_DG2_MUX	G2	G4	23	24	R3	G7	DU_DG7_MUX
DU_DG4_MUX	G4	R0	25	26	R5	R1	DU_DR1_MUX
DU_DG6_MUX	G6	R2	27	28	–	R3	DU_DR3_MUX
DU_DR0_MUX	R0	R4	29	30	–	R5	DU_DR5_MUX
DU_DR2_MUX	R2	–	31	32	–	R7	DU_DR7_MUX
DU_DR4_MUX	R4	–	33	34	–	–	V_5V0_VBUS_H3
DU_DR6_MUX	R6	–	35	36	–	–	USB_H3_DM
DGND	–	–	37	38	–	–	USB_H3_DP
I2C6_SCL	–	–	39	40	–	–	DGND
I2C6_SDA	–	–	41	42	–	–	(NC)
MSIOF2_TXD_MUX_A	–	–	43	44	–	–	MSIOF2_RXD_MUX_A
MSIOF2_SS1_MUX_A	–	–	45	46	–	–	MSIOF2_SCK_MUX_A
(NC)	–	–	47	48	–	–	DGND
LCD_PWR_EN	–	–	49	50	–	–	LCD_BLT_EN
DISPLAY_RESET#	–	–	51	52	–	–	LCD_CONTRAST_PWM2_A
DGND	–	–	53	54	–	–	DGND
TOUCH_Y+	–	–	55	56	–	–	TOUCH_X+
TOUCH_Y–	–	–	57	58	–	–	TOUCH_X–
DGND	–	–	59	60	–	–	DGND

3.3.13 CSI

The RZ/G2x provides two CSI's (Camera Sensor Interfaces). CSI0 has four lanes, CSI1 has two lanes. On the MBaRZG2x the signals are routed to a TE Connectivity connector part no. 517798**6**-2. A suitable mating connector has part no. 517798**5**-2.

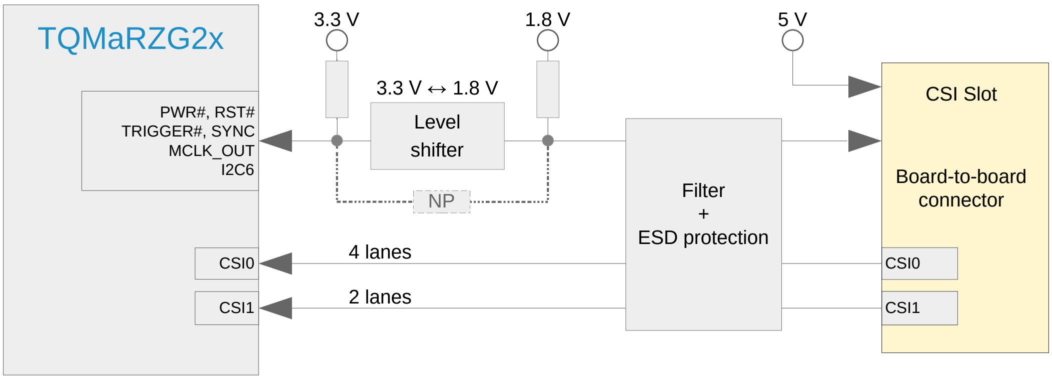


Figure 23: Block diagram CSI

The following table shows the pinout of the two CSI interfaces.
The signal direction is seen from the point of view of a connected device.

Table 23: Pinout CSI connector X21

Dir.	Signal	Pin	Pin	Signal	Dir.
–	DGND	1	2	DGND	–
I	CAM0_PWR#	3	4	CAM1_PWR#	I
I	CAM0_RST#	5	6	CAM1_RST#	I
I/O	CAM0_TRIGGER	7	8	CAM1_TRIGGER	I/O
I/O	CAM0_SYNC	9	10	CAM1_SYNC	I/O
–	(NC)	11	12	(NC)	–
–	DGND	13	14	DGND	–
O	MIPI_CSI0_DATA3_N	15	16	(NC)	–
O	MIPI_CSI0_DATA3_P	17	18	(NC)	–
–	DGND	19	20	DGND	–
O	MIPI_CSI0_DATA2_N	21	22	(NC)	–
O	MIPI_CSI0_DATA2_P	23	24	(NC)	–
–	DGND	25	26	DGND	–
O	MIPI_CSI0_DATA1_N	27	28	MIPI_CSI1_DATA1_N	O
O	MIPI_CSI0_DATA1_P	29	30	MIPI_CSI1_DATA1_P	O
–	DGND	31	32	DGND	–
O	MIPI_CSI0_DATA0_N	33	34	MIPI_CSI1_DATA0_N	O
O	MIPI_CSI0_DATA0_P	35	36	MIPI_CSI1_DATA0_P	O
–	DGND	37	38	DGND	–
O	MIPI_CSI0_CLK0_N	39	40	MIPI_CSI1_CLK1_N	O
O	MIPI_CSI0_CLK0_P	41	42	MIPI_CSI1_CLK1_P	O
–	DGND	43	44	DGND	–
I/O	I2C6_SDA_1V8	45	46	I2C6_SDA_1V8	I/O
I	I2C6_SCL_1V8	47	48	I2C6_SCL_1V8	I
–	DGND	49	50	DGND	–
I	CSI0_MCLK_OUT_1V8	51	52	CSI1_MCLK_OUT_1V8	I
–	DGND	53	54	DGND	–
–	(NC)	55	56	V_5V0	P
–	(NC)	57	58	V_5V0	P
–	(NC)	59	60	V_5V0	P

3.3.14 Fan

A polarized 3-pin 100 mil header with friction lock, TE Connectivity part no. 640456-3 is assembled on the MBaRZG2x.
The fan supply voltage can be selected with DIP switch S10-3 on the MBaRZG2x; see also 3.4.7:

- SEL_V_FAN is low: 12 V fan supply voltage
- SEL_V_FAN is high: 5 V fan supply voltage

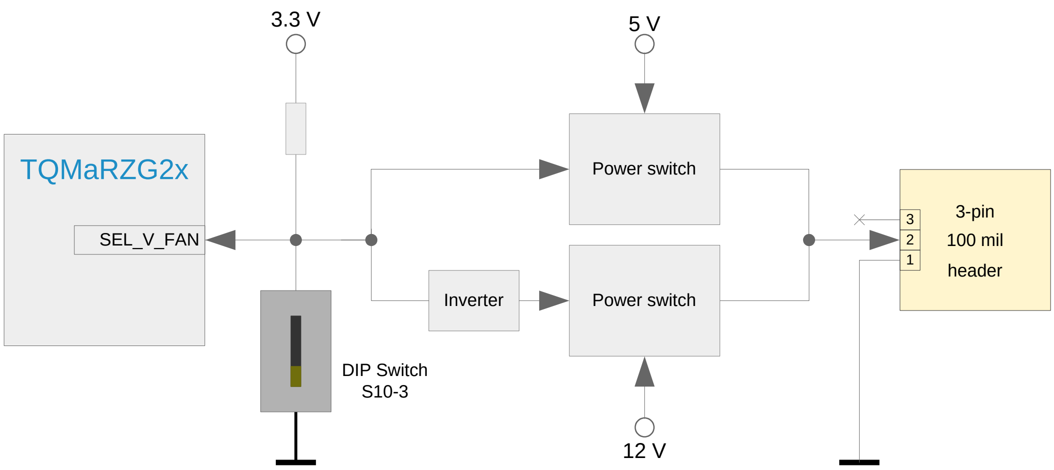


Figure 24: Block diagram fan connection

3.3.15 mikroBUS™

The MBaRZG2x provides a mikroBUS™ for system extensions. The I2C6 bus is routed to the mikroBUS™.
mikroBUS™ modules require 3.3 V and 5 V, which are provided by the MBaRZG2x. PTC fuses limit the current load at 750 mA.
SPI and UART interfaces are connected via a switch in order to use them on headers or on the mikroBUS™.
The current consumption is limited to 500 mA per supply rail.

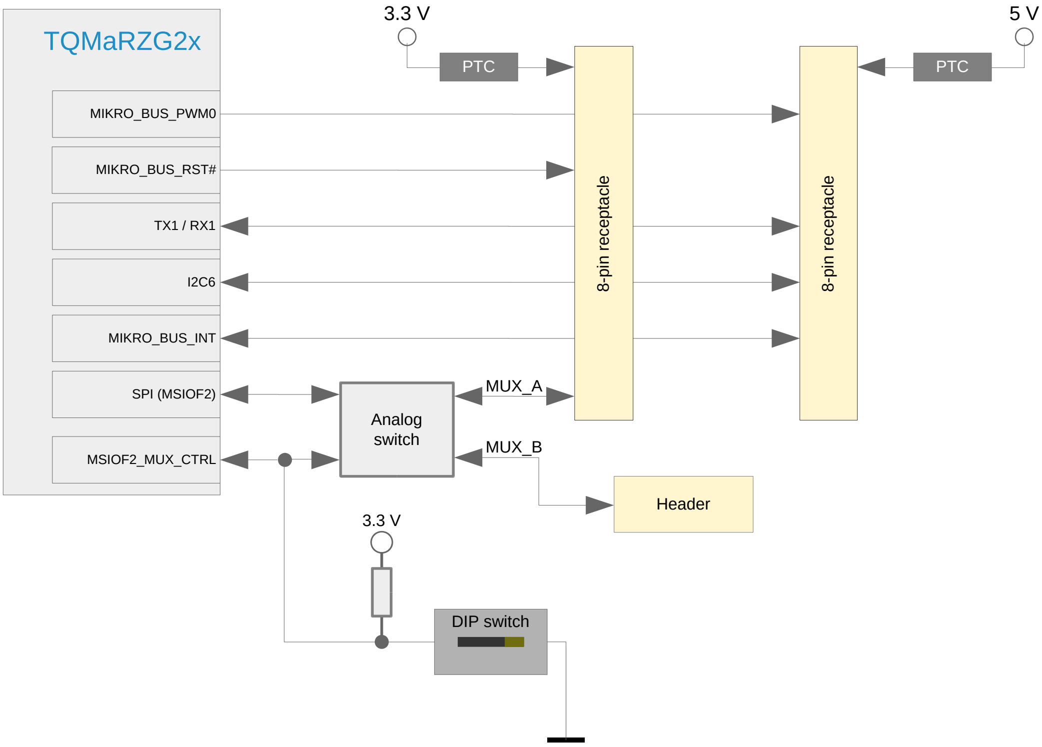


Figure 25: Block diagram mikroBUS™

The following table shows the signals of mikroBUS™ receptacles D12-X1 and D12-X2.

Table 24: Pinout mikroBUS™ receptacles D12-X1, D12-X2

D12-X1				D12-X2			
Remark	Signal	Name	Pin	Pin	Name	Signal	Remark
10 kΩ PD Option: 10 kΩ PU to 3.3 V	MIKRO_BUS_AN	AN	1	1	PWM	MIKRO_BUS_PWM0	–
10 kΩ PU to 3.3 V Option: 10 kΩ PD	MIKRO_BUS_RST#	RST	2	2	INT	MIKRO_BUS_INT	–
–	MSIOF2_SS1_MUX_B	CS	3	3	RX	TX1	SCIF1
–	MSIOF2_SCK_MUX_B	SCK	4	4	TX	RX1	SCIF1
–	MSIOF2_RXD_MUX_B	MISO	5	5	SCL	I2C6_SCL	–
–	MSIOF2_TXD_MUX_B	MOSI	6	6	SDA	I2C6_SDA	–
750 mA PTC fuse	V_3V3_MIKRO_BUS	VCC_3V3	7	7	VCC_5V	V_5V0_MIKRO_BUS	750 mA PTC fuse
–	DGND	GND	8	8	GND	DGND	–

3.3.16 Headers

The MBaRZG2x provides six 20-pin 100 mil header, which provide all unused signals and those which should be easy to access.
Two or more of the supply voltages 1.8 V, 3.3 V, 5 V, and 12 V are available at these headers.
The maximum current load of each voltage rail is 500 mA in sum at all connectors.

Table 25: Pinout header X8

Group	Signal	Pin		Signal	Group
Power	V_5V0	1	2	V_3V3	Power
Reset	TQMARZG_RST_OUT#	3	4	SYSC_UART0_RX	DEBUG
Reset	TQMARZG_RST_IN#	5	6	SYSC_UART0_TX	DEBUG
Reset	PGOOD	7	8	USB_EXTAL_CON	Clock
Clock	FSCLKST#	9	10	EXTALR_CON	Clock
HSCIF	HCTS0#	11	12	SE_ENABLE	SEC
HSCIF	HRX0	13	14	EEPROM_WP	EEPROM
HSCIF	HTX0	15	16	RTC_INT_OUT#	RTC
HSCIF	HRTS0#	17	18	EVENT_TEMPSENSOR#	EEPROM
Ground	DGND	19	20	DGND	Ground

Table 26: Pinout header X31

Group	Signal	Pin		Signal	Group
Power	V_5V0	1	2	V_3V3	Power
MISC	BUFF_D7_PIN3	3	4	AVS1	GPIO
MISC	BUFF_D7_PIN5	5	6	AVS2	GPIO
QSPI	QSPI1_CLK	7	8	QSPI0_CLK	QSPI
QSPI	QSPI1_IO0	9	10	QSPI0_IO0	QSPI
QSPI	QSPI1_IO1	11	12	QSPI0_IO1	QSPI
QSPI	QSPI1_IO2	13	14	QSPI0_IO2	QSPI
QSPI	QSPI1_IO3	15	16	QSPI0_IO3	QSPI
QSPI	QSPI1_SS#	17	18	QSPI0_SS#	QSPI
Ground	DGND	19	20	DGND	Ground

Table 27: Pinout header X32

Group	Signal	Pin		Signal	Group
Power	V_1V8	1	2	V_3V3	Power
Power	V_1V8	3	4	SD1_CLK	SDHI
SDHI	SD2_CLK	5	6	SD1_CMD	SDHI
SDHI	SD2_DS	7	8	SD1_WP	SDHI
SDHI	SD2_CMD	9	10	SD1_CD	SDHI
SDHI	SD2_DAT3	11	12	SD1_DAT3	SDHI
SDHI	SD2_DAT2	13	14	SD1_DAT2	SDHI
SDHI	SD2_DAT1	15	16	SD1_DAT1	SDHI
SDHI	SD2_DAT0	17	18	SD1_DAT0	SDHI
Ground	DGND	19	20	DGND	Ground

3.3.16 Headers (continued)

Table 28: Pinout header X33

Group	Signal	Pin		Signal	Group
Power	V_5V0	1	2	V_3V3	Power
Ground	DGND	3	4	V_3V3	Power
SCIF	TX0_MUX	5	6	DGND	Ground
SCIF	RX0_MUX	7	8	DGND	Ground
SEC	SE_14443_LA	9	10	ASEBRK	DEBUG
SEC	SE_14443_LB	11	12	MSIOF0_SCK	MSIOF
SEC	SE_7816_CLK	13	14	MSIOF0_SYNC	MSIOF
SEC	SE_7816_RST#	15	16	MSIOF0_TXD	MSIOF
SEC	SE_7816_IO1	17	18	MSIOF0_RXD	MSIOF
SEC	SE_7816_IO2	19	20	MSIOF0_SS2	MSIOF

Table 29: Pinout header X35

Group	Signal	Pin		Signal	Group
Power	V_5V0	1	2	V_3V3	Power
Power	V_12V	3	4	V_3V3	Power
Ground	DGND	5	6	DGND	Ground
DNC	RFU0	7	8	IIC_DVFS_SDA	I2C
DNC	RFU1	9	10	IIC_DVFS_SCL	I2C
DNC	RFU2	11	12	I2C6_SCL	I2C
MLB	MLB_SIG	13	14	I2C6_SDA	I2C
MLB	MLB_DAT	15	16	RPC_INT#	RPC
MLB	MLB_CLK	17	18	RPC_WP#	RPC
IRQ	NMI	19	20	RPC_RESET#	RPC

Table 30: Pinout header X36

Group	Signal	Pin		Signal	Group
Power	V_3V3	1	2	V_12V	Power
Power	V_3V3	3	4	V_12V	Power
Power	V_5V0	5	6	V_1V8	Power
Power	V_5V0	7	8	V_1V8	Power
Ground	DGND	9	10	SD3_DS	SDHI
SDHI	SD3_CLK	11	12	SD3_DAT4	SDHI
SDHI	SD3_DAT0	13	14	SD3_DAT5	SDHI
SDHI	SD3_DAT1	15	16	SD3_DAT6	SDHI
SDHI	SD3_DAT2	17	18	SD3_DAT7	SDHI
SDHI	SD3_DAT3	19	20	SD3_CMD	SDHI

3.4 Diagnostic and user interfaces

3.4.1 Temperature sensor

An SE97BTP temperature sensor is present on the MBaRZG2x. It is positioned under the TQMaRZG2x; see Figure 2, D22.

Table 31: Temperature sensor D22

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C	+75 °C to +95 °C
			Max. ±2 °C	+40 °C to +125 °C
			Max. ±3 °C	–40 °C to +125 °C

3.4.2 JTAG®

On the MBaRZG2x the RZ/G2x JTAG® port is routed to a 20-pin header (X7) with standard ARM® JTAG® pinout; see Figure 2.
The JTAG® port works with 1.8 V signal level. The JTAG® interface has no ESD protection.

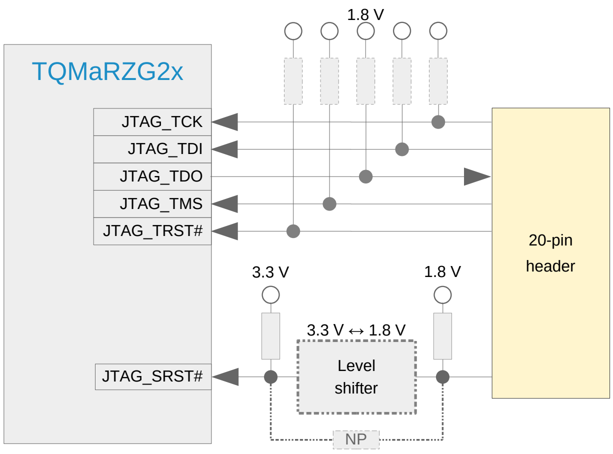


Figure 26: Block diagram JTAG®

Table 32: Pinout JTAG® header X7

Signal	Pin	Pin	Signal
VTREF	1	2	V_SUPPLY
TRST#	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
SRST#	15	16	GND
DBGRQ	17	18	GND
DBGACK	19	20	GND

3.4.3 SW Debug

An SWD (software debug) port for the TQMaRZG2x board controller is available on the MBaRZG2x.
The SWD port is routed to the 10-pin header X23 on the MBaRZG2x; see Figure 2.
This interface is not required for normal operation.

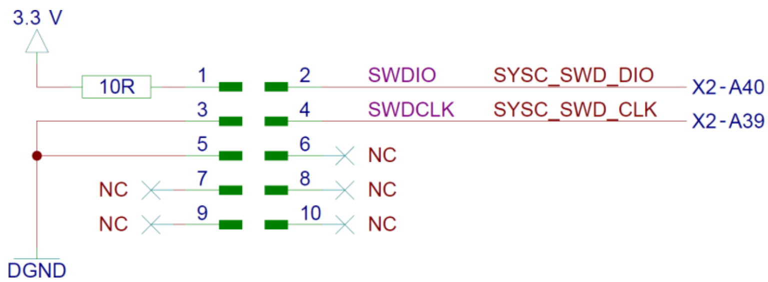


Figure 27: SWD port for TQMaRZG2x board controller

3.4.4 Status LEDs

The presence of all important supply voltages is indicated by green LEDs. They are lit when the corresponding voltage is active. The following supply voltages are indicated by green LEDs:

Table 33: Diagnostic and status LEDs

Interface	Reference	Colour	Signalling
Power	V8	Green	Status V_24V – lit when 24 V are active
	V9	Green	Status V_12V – lit when 12 V are active
	V10	Green	Status V_5V0 – lit when 5.0 V are active
	V13	Green	Status V_5V0_MOD – lit when TQMaRZG2x 5.0 V are active
	V7	Green	Status V_3V3 – lit when 3.3 V are active
	V77	Green	Status V_2V5 – lit when 2.5 V are active
	V11	Green	Status V_1V8 – lit when 1.8 V are active
	V12	Green	Status V_1V5 – lit when 1.5 V are active
	V14	Green	Status V_1V1 – lit when 1.1 V are active
	V15	Green	Status V_1V0 – lit when 1.0 V are active
Reset	V75	Red	Status Reset – lit when the TQMaRZG2x is in reset
	V78	Red	Status Reset – lit when the reset button S9 is pressed
	V18	Green	Status PGOOD – lit when the TQMaRZG2x power sequencing was successful
Debug-USB	V1	Green	Debug USB – lit when the bridge is USB powered
Mini PCIe	V4	Green	Mini PCIe WWAN activity
	V5	Green	Mini PCIe WLAN activity
	V6	Green	Mini PCIe WPAN activity
USB	V2	Green	Status V_5V0_VBUS_OTG – lit when 5.0 V is active
	V19	Green	Status V_5V0_VBUS_H1 – lit when 5.0 V are active
	V20	Green	Status V_5V0_VBUS_H2 – lit when 5.0 V are active
M.2	V3	Green	Device Activity M2
Ethernet	X26	Yellow	Activity LED integrated in X26
	X26	Green	Link LED integrated in X26
User LED	V17	Green	USER_LED1 – can be controlled by the CPU
	V16	Green	USER_LED2 – can be controlled by the CPU
	V46	Green	USER_LED3 – can be controlled by the CPU

3.4.5 Reset pushbutton

A reset pushbutton (S9) is provided on the MBaRZG2x. More details about full or partial reset can be found in chapter 3.1.5.

3.4.6 GP pushbuttons

Three general purpose pushbuttons (S6, S7, S8) are provided on the MBaRZG2x. The pushbuttons switch to Ground and have 4.7 kΩ pull-ups to 3.3 V. The pushbutton status can be read at the following GPIO ports:

Table 34: GP pushbuttons S6, S7, S8

GP pushbutton	Signal	TQMaRZG2x	RZ/G2x
S6	USER_BUTTON_1	X2-A55	GP6_21 / SSI_SDATA9_A
S7	USER_BUTTON_2	X2-A58	GP6_16 / SSI_SDATA6
S8	USER_BUTTON_3	X2-A66	GP6_18 / SSI_WS78

3.4.7 DIP switches

Four 8-fold DIP switches (S2 to S5) are provided on the MBaRZG2x. The single switches switch to 3.3 V and have 10 kΩ PDs.
The function of the DIP switches is explained in detail in chapter 3.1.4.
A 4-fold DIP switch (S10) is provided on the MBaRZG2x. The single switches switch to GND and have 4.7 kΩ pull-ups to 3.3 V.
The following table shows the functions of DIP switch S10.

Table 35: DIP switch S10

DIP switch	Signal	Position	Function		Remark
[1] 1~2	PCIE1_SATA_SEL	Open	PCIe		4.7 kΩ PU to 3.3 V
		Closed	SATA		
[2] 3~4	MSIOF2_MUX_CTRL	Open	MSIOF2_MUX_B		4.7 kΩ PU to 3.3 V
		Closed	MSIOF2_MUX_A		
[3] 5~6	SEL_V_FAN	Open	5 V fan supply		4.7 kΩ PU to 3.3 V
		Closed	12 V fan supply		
[4] 7~8	UART_MUX_CTRL	Open	SCIF0 (UART0)	UART0 on X33	4.7 kΩ PU to 3.3 V
			SCIF2 (UART2)	(NC)	
		Closed	SCIF0 (UART0)	UART0 on USB (X9)	
			SCIF2 (UART2)		

4. SOFTWARE

No software is required for the MBaRZG2x.
Suitable software is only required on the TQMaRZG2x and is not a part of this User's Manual.
More information can be found in the TQMaRZG2x Support Wiki.

5. MECHANICS

5.1 MBaRZG2x dimensions

The MBaRZG2x has overall dimensions (length × width) of 170 × 170 mm².
The highest component on the top side of the MBaRZG2x is approximately 15.5 mm (stacked USB Type A connector).
The highest components on the bottom side of the MBaRZG2x are:

- MIPI CSI connector (4.6 mm)
- M.2 connector (4.2 mm)
- mPCIe connector (4.0 mm)

The overall height of the MBaRZG2x is approximately 21.7 mm.
The MBaRZG2x has six 4.2 mm housing mounting holes, and four 2.7 mm heat sink mounting holes.
The MBaRZG2x weighs approximately 232 grams without TQMaRZG2x.

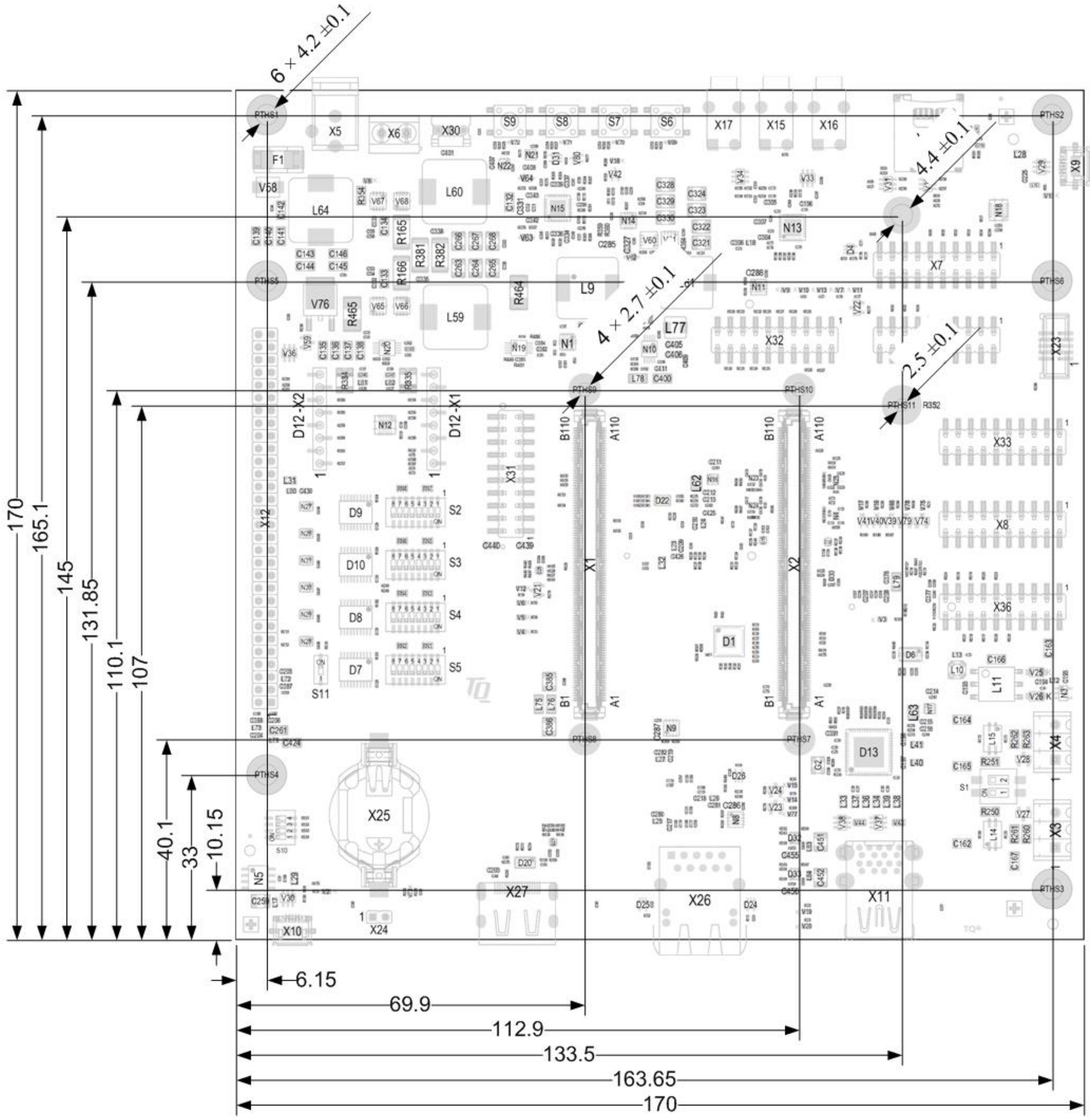


Figure 28: MBaRZG2x dimensions

5.2 MBaRZG2x labels

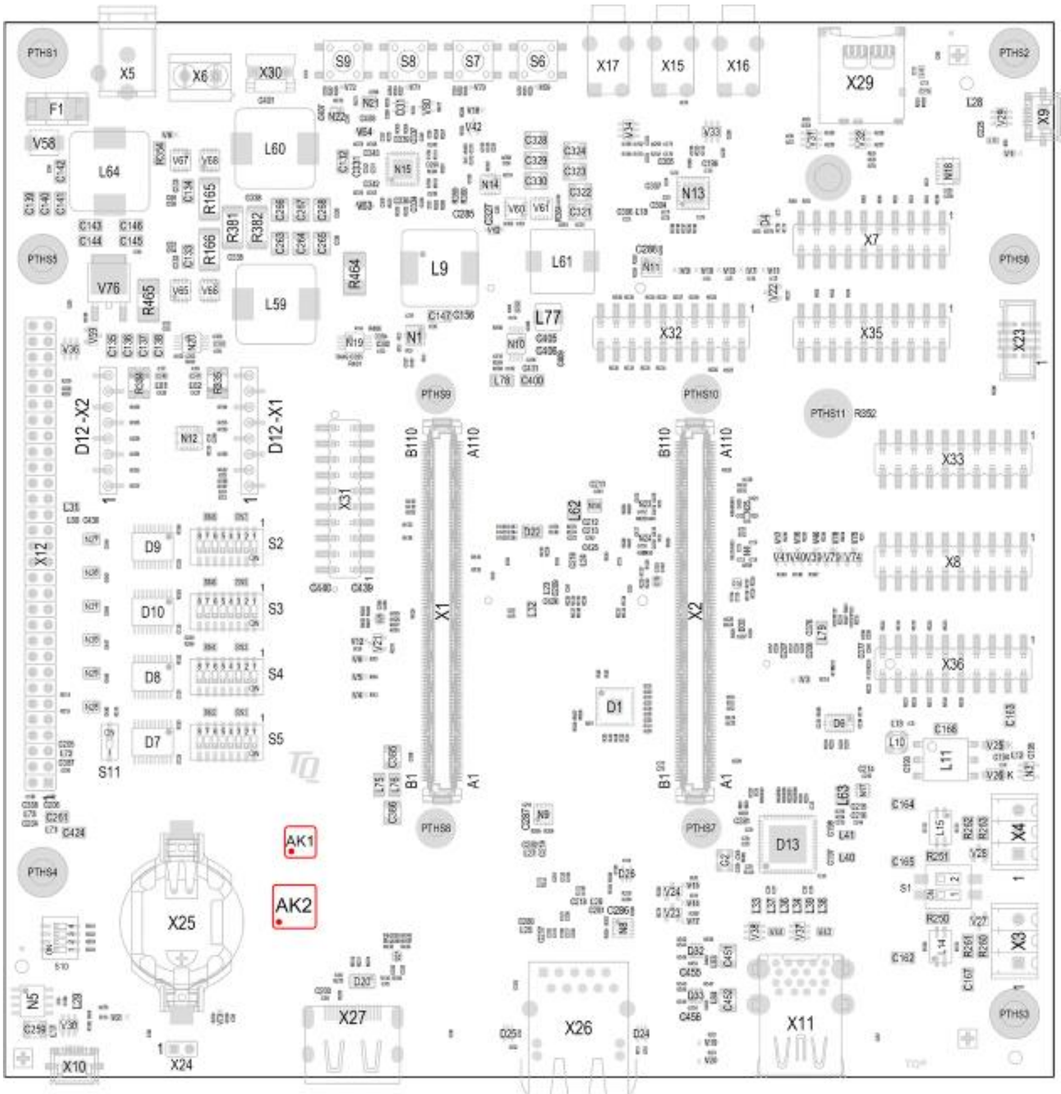


Figure 29: MBaRZG2x label position

The labels on the MBaRZG2x revision 0100 show the following information:

Table 36: Labels on MBaRZG2x

Label	Content
AK1	Serial number
AK2	MBaRZG2x version and revision, tests performed

5.3 Notes of treatment

The TQMaRZG2x is held in its mating connectors with a considerable retention force.
To avoid damage caused by mechanical stress, the TQMaRZG2x may only be extracted from the MBaRZG2x by using the extraction tool MOZIaRZG2x that can be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMaRZG2x for the extraction tool MOZIaRZG2x.

5.4 MBaRZG2x impedances

The MBaRZG2x serves as a design base for customer products, as well as a reference platform during development.
By default, all signals on the MBaRZG2x have a single-ended impedance of nominal 50 Ω ±10 %. Depending on the interface, other impedances are also used on the MBaRZG2x. The following table shows the affected interfaces:

Table 37: High-speed buses, impedances

Interface	Signal	Impedance on MBaRZG2x	Recommendation for carrier board
USB 2.0	Data	90 Ω differential	90 Ω ±10 % differential
USB 3.0	Data	90 Ω differential	90 Ω ±10 % differential
	Clock	100 Ω differential	100 Ω ±10 % differential
PCIe	Data	90 Ω differential	90 Ω ±10 % differential
	Clock	100 Ω differential	100 Ω ±10 % differential
SATA	Data	90 Ω differential	90 Ω ±10 % differential
CSI	Clock	100 Ω differential	100 Ω ±10 % differential
	Data	100 Ω differential	100 Ω ±10 % differential
HDMI	Clock	100 Ω differential	100 Ω ±10 % differential
	Data	100 Ω differential	100 Ω ±10 % differential
LVDS	Clock	100 Ω differential	100 Ω ±10 % differential
	Data	100 Ω differential	100 Ω ±10 % differential

5.5 Housing

The form factor and the mounting holes of the MBaRZG2x are designed for mounting in a standard Mini ITX housing.

5.6 Thermal management

When idle, the MBaRZG2x and TQMaRZG2x have an average power consumption of about 8 to 10 watts.
Further power dissipation occurs with higher CPU loads and on external devices (mPCIe, M.2, etc.).

Attention: TQMaRZG2x heat dissipation	
	The RZ/G2x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMaRZG2x must be taken into consideration when connecting the heat sink. The TQMaRZG2x is not the highest component. Inadequate cooling connections can lead to overheating of the TQMaRZG2x and thus malfunction, deterioration or destruction.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The MBaRZG2x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the MBaRZG2x.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety have not been carried out.

7. CLIMATIC AND OPERATIONAL CONDITIONS

The permissible temperature range of the MBaRZG2x strongly depends on the installation situation (heat emission through heat conduction and convection) and the usage. The heat generation of the TQMaRZG2x also contributes to this, so no fixed value can be given for the entire unit. In general, reliable operation is given if the following conditions are met:

Table 38: Climatic and operational conditions MBaRZG2x

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	Without Lithium battery
Storage temperature	–40 °C to +100 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMaRZG2x heat dissipation	
⚠	The RZ/G2x CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMaRZG2x must be taken into consideration when connecting the heat sink. The TQMaRZG2x is not the highest component. Inadequate cooling connections can lead to overheating of the TQMaRZG2x and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBaRZG2x. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBaRZG2x.
Service life-limiting components, such as electrolytic capacitors, were not used.
The MBaRZG2x is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBaRZG2x is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBaRZG2x was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000.
The MBaRZG2x must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBaRZG2x enable compliance with EuP requirements for the MBaRZG2x.

8.5 Packaging

The MBaRZG2x is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

Due to technical reasons a battery is necessary for the MBaRZG2x. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the MBaRZG2x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of the MBaRZG2x is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 39: Acronyms

Acronym	Meaning
ADG	Audio Clock Generator
ARM®	Advanced RISC Machine
AVB	Audio-Video Bridging
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN-FD	Controller Area Network Flexible Data rate
CPG	Clock Pulse Generator
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FPC	Flat Panel Cable
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
HDMI	High-Definition Multimedia Interface
HSCIF	High-speed Serial Communication Interface
I/O	Input/Output
I2C	Inter-Integrated Circuit
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LBSC	External Bus Controller for EX-Bus
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPDDR4	Low Power Double Data Rate 4
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Controller
MIPI	Mobile Industry Processor Interface
MLB	Media Link Bus
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean operating Time Between Failures
NC	Not Connected
NOR	Not-Or
NP	Not Populated
OTG	On-The-Go

9.1 Acronyms and definitions (continued)

Table 39: Acronyms (continued)

Acronym	Meaning
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PTC	Positive Temperature Coefficient
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
R/W	Read/Write
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SCIF	Serial Communication Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDHI	Secure Digital Host Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SSD	Solid-State Disk
SSI	Serial Sound Interface
SVHC	Substances of Very High Concern
TSE	Trust Secure Element
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
VSP	Video Signal Processor
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network
ZIF	Zero Insertion Force

9.2 References

Table 40: Further applicable documents

No.	Name	Rev., Date	Company
(1)	RZ/G2x User's Manual	Rev. 1.00, Mar. 2020	Renesas
(2)	TQMaRZG2x User's Manual	– current –	TQ-Systems
(3)	TQMaRZG2x Support Wiki	– current –	TQ-Systems

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