MBa8Mx
User's Manual

MBa8Mx UM 0102
11.07.2022

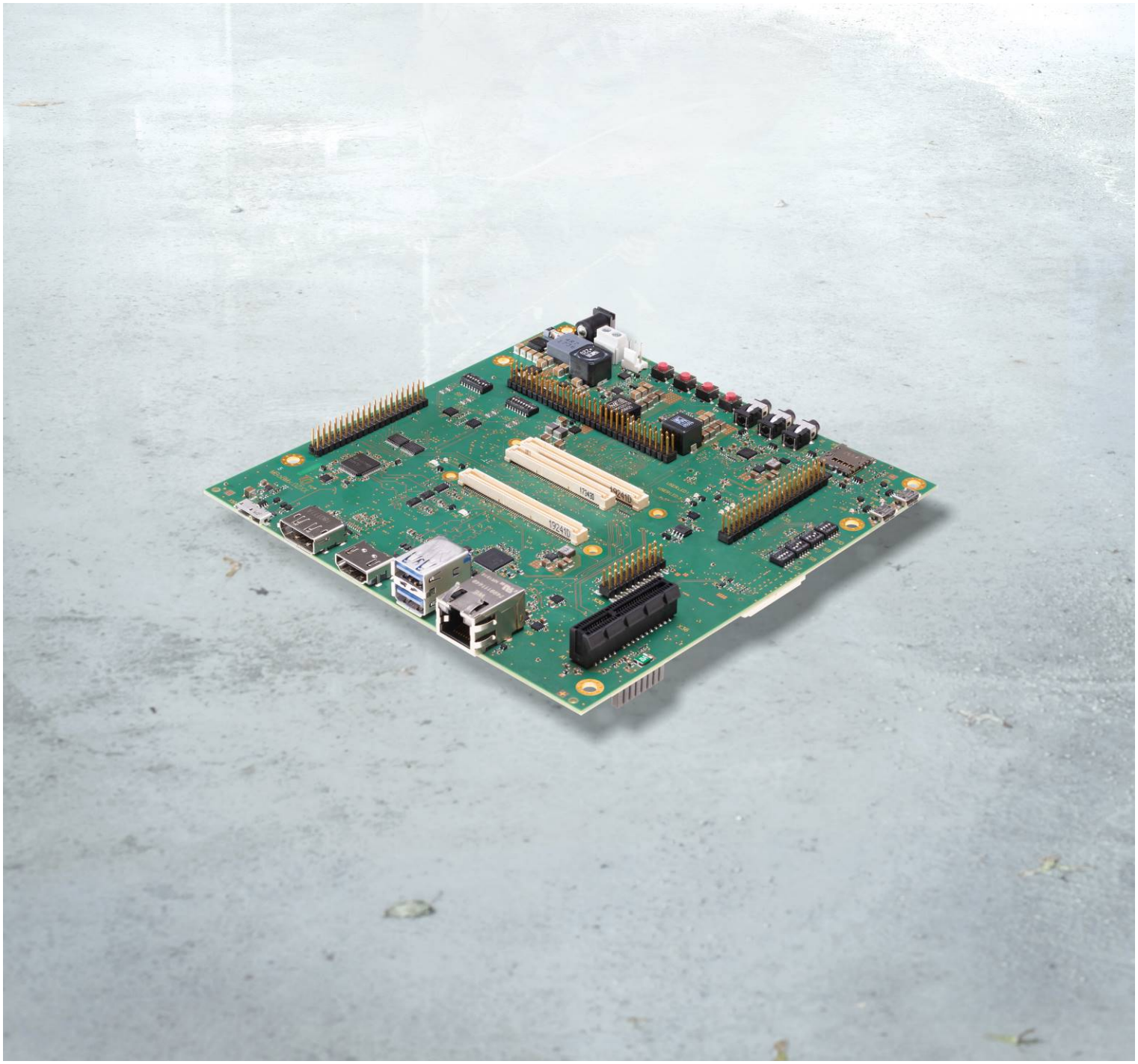

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	29.07.2020	Petz		First edition
0101	27.02.2021	Petz	All 2 Figure 1 Figure 2 Table 12, Table 15 Table 13, Figure 14 3.2.2 3.2.2.1, 3.2.2.2 Table 39 6.6	Non-functional changes, formatting, structure, phrases, expressions CPUs, “Note” and revision 03xx added Updated Added Clarified Added Restructured Added Footnote 9 added Differentiated between Rev. 02xx and Rev. 03xx
0102	11.07.2022	Petz Kreuzer	All 3.1.1.2 Table 12, Table 13 Table 20 Footnotes 4 to 7 3.2.8 Table 2 Table 35, Table 37	Non-functional changes, expressions, phrases Information regarding signal direction added S8 signal names according to MBa8Mx revision differentiated “on MBa8Mx revision 02xx” added Corrected Notes about the removal of eDP eDP entry corrected corrected

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa8Mx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8Mx schematics
- TQMa8Mx User's Manual
- i.MX 8M Data Sheets
- i.MX 8M Reference Manuals
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8Mx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa8Mx, as of revision 0200 and as of revision 0300.
Differences between both revisions, if relevant, are described in this User's Manual.

Note: Designations, available features and interfaces	
	In order to facilitate the readability of this User's Manual, the designations “MBa8Mx” and “i.MX 8M” are used throughout. If technical aspects require a differentiation between TQMa8Mx, TQMa8MxML and TQMa8MxNL, or i.MX 8M, i.MX 8M Mini and i.MX 8M Nano, the appropriate designation is used. This User's Manual describes all features and interfaces provided by the MBa8Mx or TQMa8Mx family. A certain MBa8Mx or TQMa8Mx derivative does not necessarily provide all features and interfaces described in this User's Manual.

The MBa8Mx is designed as a carrier board for the TQ-Minimodules TQMa8Mx, TQMa8MxML and TQMa8MxNL.
The TQMa8Mx can be directly plugged in the MBa8Mx.
For development purposes, the TQMa8MxML and the TQMa8MxNL are soldered on an LGA-to-plug-in adapter.
Core of the MBa8Mx is the TQMa8Mx with an NXP i.MX 8M, i.MX 8M Mini or i.MX 8M Nano CPU.
The TQMa8Mx connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, SD card, etc., all other available signals of the TQMa8Mx are routed on 100 mil standard pin headers on the MBa8Mx.
CPU features and interface can be evaluated, software development for a TQMa8Mx-based project can start immediately.
Currently fifteen i.MX 8M derivatives are supported:

I. TQMa8Mx (Plug-in module)
   1. i.MX 8M Dual (Dual Cortex®-A53)
   2. i.MX 8M QuadLite (Quad Cortex®-A53)
   3. i.MX 8M Quad (Quad Cortex®-A53)

II. TQMa8MxML (LGA module, via adapter)
   4. i.MX 8M Mini SoloLite (Single Cortex®-A53)
   5. i.MX 8M Mini Solo (Single Cortex®-A53)
   6. i.MX 8M Mini DualLite (Dual Cortex®-A53)
   7. i.MX 8M Mini Dual (Dual Cortex®-A53)
   8. i.MX 8M Mini QuadLite (Quad Cortex®-A53)
   9. i.MX 8M Mini Quad (Quad Cortex®-A53)

III. TQMa8MxNL (LGA module, via adapter)
   10. i.MX 8M Nano SoloLite (Single Cortex®-A53)
   11. i.MX 8M Nano Solo (Single Cortex®-A53)
   12. i.MX 8M Nano DualLite (Dual Cortex®-A53)
   13. i.MX 8M Nano Dual (Dual Cortex®-A53)
   14. i.MX 8M Nano QuadLite (Quad Cortex®-A53)
   15. i.MX 8M Nano Quad (Quad Cortex®-A53)

2.1 MBa8Mx block diagram

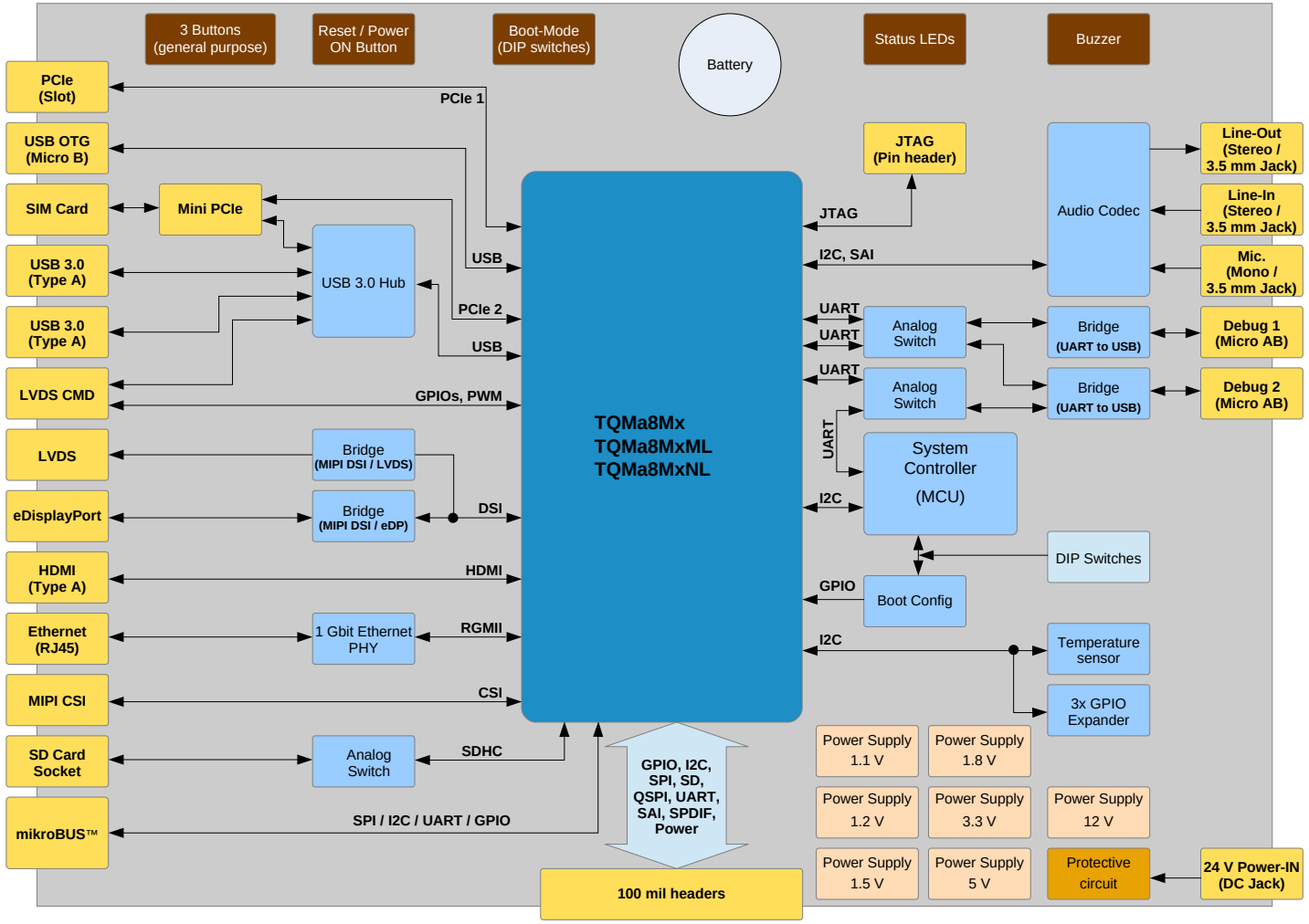


Figure 1: Block diagram MBa8Mx revision 02xx

2.1 MBa8Mx block diagram (continued)

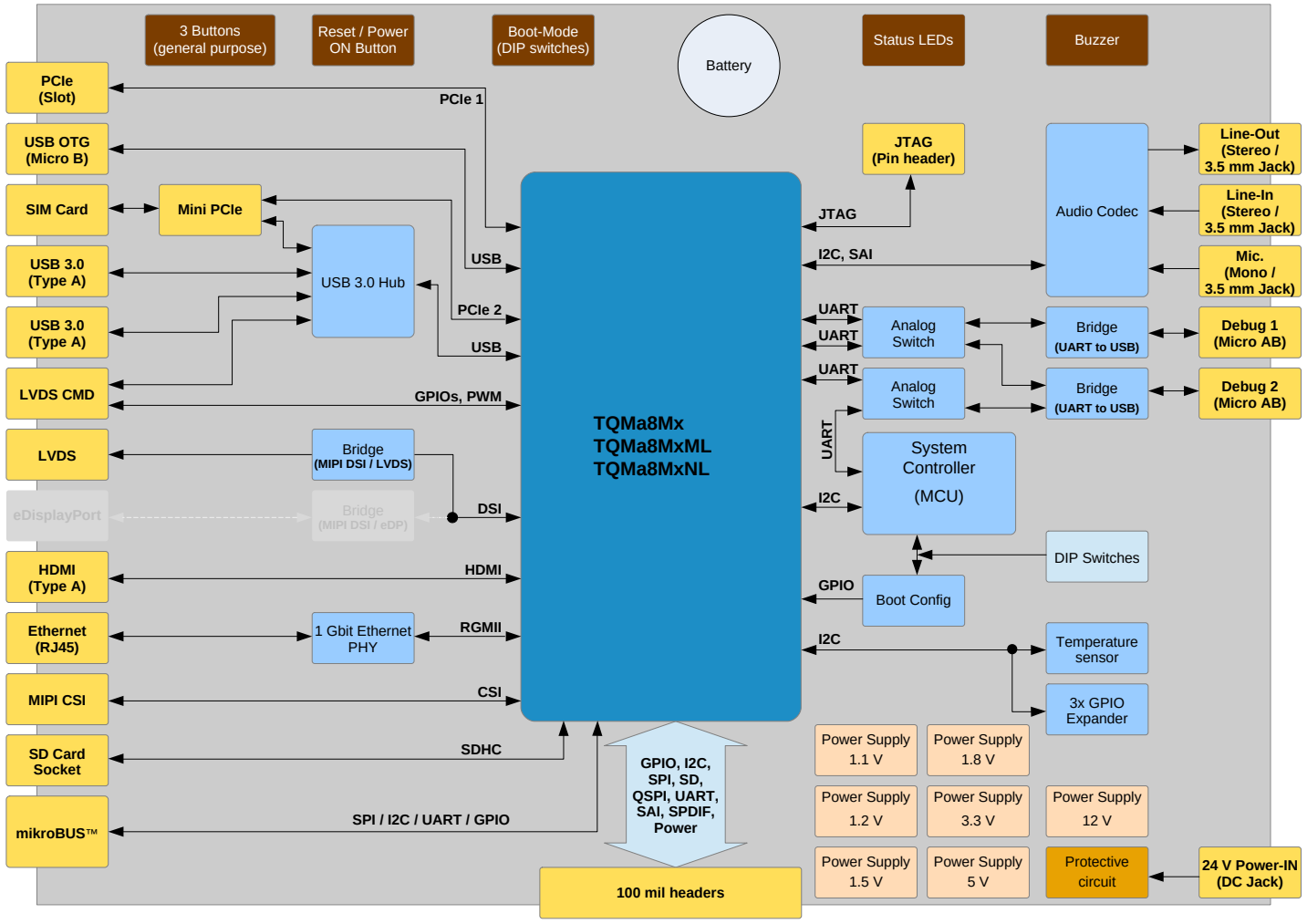


Figure 2: Block diagram MBa8Mx revision 03xx

2.2 MBa8Mx data interfaces

The following interfaces/functions and user interfaces are available on the MBa8Mx:

Table 2: Data interfaces

Interface	Connector	Type	MBa8Mx	MBa8MxML	MBa8MxNL
USB 3.0 SS Host	X6	USB, stacked Type A	✓	Only USB2.0	Only USB2.0
USB 3.0 SS OTG	X19	USB, Micro B	✓	✓	Switchable with hub – adapter board
Ethernet, 1000 Base-T	X9	RJ-45, integrated magnetics	✓	✓	✓
SD card	X8	Push-pull	✓	✓	✓
HDMI	X11	HDMI Type A	✓	(n/a)	(n/a)
eDisplayPort	X24	20-pin, 90°	(n/a)	(n/a)	(n/a)
LVDS	X37	30-pin, DF19G	✓	✓	✓
LVDS CMD	X23	20-pin, DF19G	✓	✓	✓
MIPI CSI	X31	60-pin, Board-to-Board	✓	✓	✓
Audio	X12 X13 X14	3.5 mm jack • MIC • Line-in • Line-out	✓	✓	✓
PCIe	X36	PCIe slot, 1 lane	✓	✓	✓
	X28	Mini PCIe slot	✓	Only USB	Only USB
	X29	SIM card holder	✓	✓	✓
Headers	X17 X34, X35	100 mil header 1 × 60-pin 2 × 40-pin	✓	Not all interfaces available	Not all interfaces available
Mikro Bus	X20, X21	2 × 8-pin header	✓	✓	✓
Power In	X4	DC jack (2.5 mm / 5.5 mm)	✓	✓	✓
	X5	2-pin screw terminal block	✓	✓	✓
Debug UART	X15, X16	USB, Micro AB	✓	✓	✓
Coin cell	X33	CR2032 holder	✓	✓	✓

The MBa8Mx provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	2 × Blue LED	Input voltage, Power_Good
	1 × Red LED	Power fail
	2 × Green LED	Debug LEDs for USB debug interface
	2 × Green LED	GP LEDs at port expander
	3 × Green LED	WWAN, WLAN, WPAN
	2 × Green LED	GP LEDs
	1 × Orange LED	GP LED
	2 × Green / Yellow LED	Ethernet-LEDs (Activity / Speed)
Temperature sensor	1 × SE97BTP	Digital I^2C temperature sensor
Power / Reset button	1 × Push button	CPU-ON/OFF
GP button	3 × Push button	General purpose push button at port expander
Boot-Mode configuration	2 × 8-fold DIP switch	Boot Device configuration
Other configurations	3 × 4-fold DIP switch	2 × Boot Mode configuration 1 × Mux control 1 × System control
Buzzer	1 × KMTG1203	–
JTAG	1 × 20-pin, 100 mil header	Available with all TQMa8Mx /ML /NL versions

3. ELECTRONICS

3.1 MBa8Mx functional groups

The following chapters describe the interfaces of the MBa8Mx in connection with a TQMa8Mx.
Functional differences of TQMa8MxML and TQMa8MxNL are referred to, when applicable. The functionality is shown in Table 2.

3.1.1 TQMa8Mx

The TQMa8Mx is the central system on the MBa8Mx. It provides LPDDR4 SDRAM, eMMC, NOR flash, RTC, an EEPROM, power supply and power management functionality. All TQMa8Mx internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa8Mx connectors or LGA pads. This enables to use the TQMa8Mx with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa8Mx User's Manual. On the MBa8Mx the standard interfaces like USB, Ethernet, etc., provided by the TQMa8Mx are routed to industry standard connectors. All other signals and buses provided by the TQMa8Mx are routed to 100 mil headers.
The boot behaviour of the TQMa8Mx can be controlled. The boot mode configuration is set by DIP switches on the MBa8Mx.
Furthermore the MBa8Mx provides all power supplies and configurations required for the operation of the TQMa8Mx.
The MBa8Mx supports TQMa8Mx modules with an i.MX 8M, i.MX 8M Mini, or i.MX 8M Nano CPU.

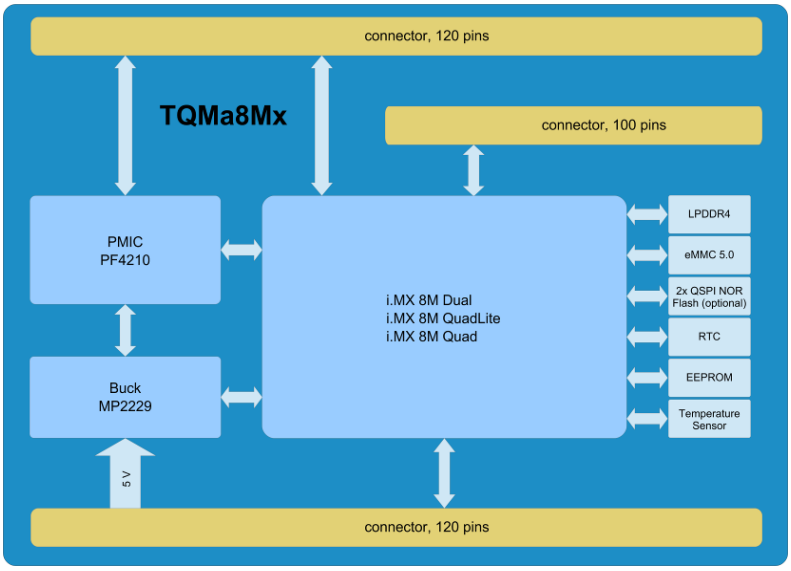


Figure 3: Block diagram TQMa8Mx

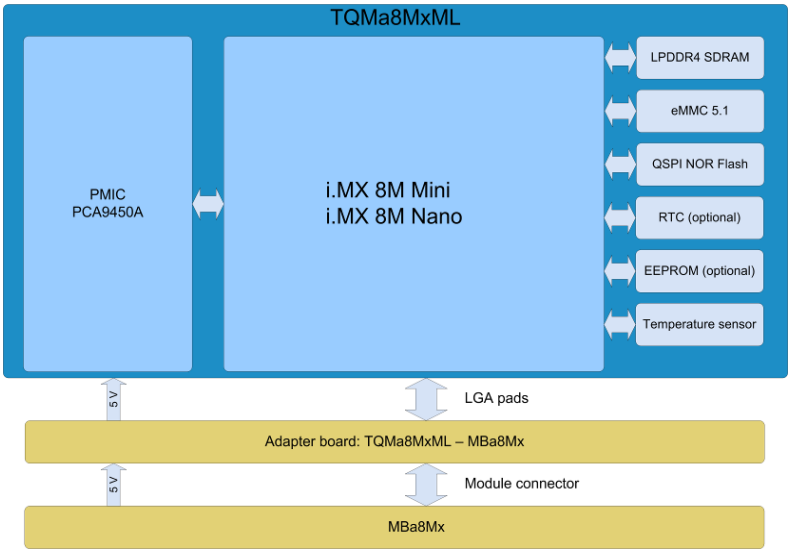


Figure 4: Block diagram TQMa8MxML or TQMa8MxNL

3.1.1.1 TQMa8Mx mating connectors

The TQMa8Mx is connected to the MBa8Mx with 340 pins on three connectors.
The following table shows details of the connectors assembled on the MBa8Mx:

Table 4: Connectors assembled on MBa8Mx

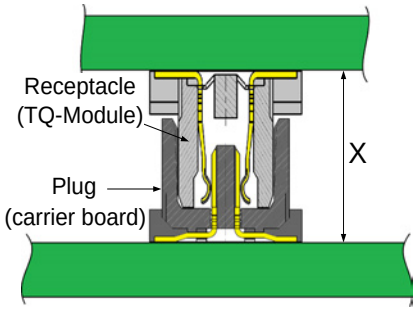
Manufacturer	Pin count / part number	Qty.	Remark
TE connectivity	120-pin / 5177986-5	2	0.2 µm gold plating
	100-pin / 5177986-4	1	0.2 µm gold plating

The TQMa8Mx is held in the mating connectors on the MBa8Mx by 340 pins with a retention force of approximately 34 N.
To avoid damaging the connectors of the MBa8Mx or the TQMa8Mx while removing the TQMa8Mx, the use of the extraction tool MOZIa8M is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8Mx for the extraction tool MOZIa8M.

The following table shows some suitable mating connectors for the carrier board:

Table 5: Carrier board mating connectors

Manufacturer	Pin count	Part number	Remark	Stack height (X)	
TE connectivity	100-pin: 120-pin:	5177986-4 5177986-5	On MBa8Mx	5 mm	
	100-pin: 120-pin:	1-5177986-4 1-5177986-5	–	6 mm	
	100-pin: 120-pin:	2-5177986-4 2-5177986-5	–	7 mm	
	100-pin: 120-pin:	3-5177986-4 3-5177986-5	–	8 mm	

The pins assignment listed in Table 6, Table 7 and Table 8 refer to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 6, Table 7 and Table 8 refer to the i.MX 8M documentation, see Table 49.

3.1.1.2 TQMa8Mx pinout

All available TQMa8Mx signals are routed on three connectors on the MBa8Mx. All available TQMa8MxML or TQMa8MxNL signals are routed to LGA pads and made available via an LGA-to-plug-in adapter, which can be plugged on the MBa8Mx.
The direction of the signals in the following tables are seen from the TQMa8Mx's perspective.

Note: Available interfaces	
	Depending on the TQMa8Mx derivative not all interfaces are available. More information about available interfaces can be found in the TQMa8Mx, or TQMa8MxML_NL User's Manuals and pinout tables.

3.1.1.2 TQMa8Mx pinout (continued)

Table 6: Pinout TQMa8Mx connector X1

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	5 V	Supply	VCC5V_IN	1	2	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	3	4	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	5	6	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	7	8	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	9	10	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	11	12	VCC5V_IN	Supply	5 V	P	–
–	P	0 V	Ground	DGND	13	14	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	15	16	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	17	18	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	19	20	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	21	22	I2C4_SDA	I2C	3.3 V	I/O	F9
E9	I/O	3.3 V	I2C	I2C3_SDA	23	24	I2C4_SCL	I2C	3.3 V	O	F8
G8	O	3.3 V	I2C	I2C3_SCL	25	26	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	27	28	UART2_TXD	UART	1.8 V / 3.3 V [1]	O	D6
A7	O	1.8 V / 3.3 V [1]	UART	UART1_TXD	29	30	UART2_RXD	UART	1.8 V / 3.3 V [1]	I	B6
C7	I	1.8 V / 3.3 V [1]	UART	UART1_RXD	31	32	UART4_TXD	UART	1.8 V / 3.3 V [1]	O	D7
B7	O	1.8 V / 3.3 V [1]	UART	UART3_TXD	33	34	UART4_RXD	UART	1.8 V / 3.3 V [1]	I	C6
A6	I	1.8 V / 3.3 V [1]	UART	UART3_RXD	35	36	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	37	38	CSI2_CLK_N	CSI	1.8 V	O	A19
–	P	0 V	Ground	DGND	39	40	CSI2_CLK_P	CSI	1.8 V	O	B19
A22	O	1.8 V	CSI	CSI1_CLK_N	41	42	DGND	Ground	0 V	P	–
B22	O	1.8 V	CSI	CSI1_CLK_P	43	44	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	45	46	CSI2_D3_N	CSI	1.8 V	I	C19
–	P	0 V	Ground	DGND	47	48	CSI2_D3_P	CSI	1.8 V	I	D19
C21	I	1.8 V	CSI	CSI1_D3_N	49	50	DGND	Ground	0 V	P	–
D21	I	1.8 V	CSI	CSI1_D3_P	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	CSI2_D2_N	CSI	1.8 V	I	A21
–	P	0 V	Ground	DGND	55	56	CSI2_D2_P	CSI	1.8 V	I	B21
B24	I	1.8 V	CSI	CSI1_D2_N	57	58	DGND	Ground	0 V	P	–
C23	I	1.8 V	CSI	CSI1_D2_P	59	60	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	61	62	CSI2_D1_N	CSI	1.8 V	I	A20
–	P	0 V	Ground	DGND	63	64	CSI2_D1_P	CSI	1.8 V	I	B20
C22	I	1.8 V	CSI	CSI1_D1_N	65	66	DGND	Ground	0 V	P	–
D22	I	1.8 V	CSI	CSI1_D1_P	67	68	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	69	70	CSI2_D0_N	CSI	1.8 V	I	C20
–	P	0 V	Ground	DGND	71	72	CSI2_D0_P	CSI	1.8 V	I	D20
A23	I	1.8 V	CSI	CSI1_D0_N	73	74	DGND	Ground	0 V	P	–
B23	I	1.8 V	CSI	CSI1_D0_P	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	QSPI_B_DQS	QSPI_B [2]	1.8 V	I	K19
M20	I	1.8 V	QSPI_A [2]	QSPI_A_DQS	79	80	QSPI_B_SS1#	QSPI_B	1.8 V	O	H20
G21	O	1.8 V	QSPI_A	QSPI_A_SS1#	81	82	QSPI_B_SS0#	QSPI_B [2]	1.8 V	O	F21
H19	O	1.8 V	QSPI_A [2]	QSPI_A_SS0#	83	84	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	85	86	QSPI_B_DATA3	QSPI_B [2]	1.8 V	I/O	M19
J21	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA3	87	88	QSPI_B_DATA2	QSPI_B [2]	1.8 V	I/O	L19
H22	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA2	89	90	QSPI_B_DATA1	QSPI_B [2]	1.8 V	I/O	J22
J20	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA1	91	92	QSPI_B_DATA0	QSPI_B [2]	1.8 V	I/O	L20
G20	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA0	93	94	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	95	96	QSPI_B_SCLK	QSPI_B [2]	1.8 V	O	H21
G19	O	1.8 V	QSPI_A [2]	QSPI_A_SCLK	97	98	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	99	100	ENET_MDC	ENET	1.8 V	O	N20
N19	I/O	1.8 V	ENET	ENET_MDIO	101	102	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	103	104	ENET_TXC	ENET	1.8 V	O	T19
T20	I	1.8 V	ENET	ENET_RXC	105	106	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	107	108	DGND	Ground	0 V	P	–
T21	I	1.8 V	ENET	ENET_RX_CTL	109	110	ENET_TX_CTL	ENET	1.8 V	O	P19
U19	I	1.8 V	ENET	ENET_RD0	111	112	ENET_TD0	ENET	1.8 V	O	R20
U21	I	1.8 V	ENET	ENET_RD1	113	114	ENET_TD1	ENET	1.8 V	O	R21
U20	I	1.8 V	ENET	ENET_RD2	115	116	ENET_TD2	ENET	1.8 V	O	R19
V19	I	1.8 V	ENET	ENET_RD3	117	118	ENET_TD3	ENET	1.8 V	O	P20
–	P	0 V	Ground	DGND	119	120	DGND	Ground	0 V	P	–

1: Voltage can be set via NVCC_UART, pin X2-10.
2: Depending on the MBa8Mx variant, one or both QSPI_A / QSPI_B interfaces are used by populated NOR flash.

3.1.1.2 TQMa8Mx pinout (continued)

Table 7: Pinout TQMa8Mx connector X2

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	3.3 V	Supply	VCC3V3	1	2	DGND	Ground	0 V	P	–
F5	P	1.8 V / 3.3 V	Supply	NVCC_ECSPI	3	4	V_LICELL	Supply	3 V	P	–
–	P	0 V	Ground	DGND	5	6	NVCC_1V8	Supply	1.8 V	P	–
F6	O	3.3 V	SPDIF	SPDIF_TX	7	8	NVCC_SD2	Supply	1.8 V / 3.3 V	P	N23
G6	I	3.3 V	SPDIF	SPDIF_RX	9	10	NVCC_UART	Supply	1.8 V / 3.3 V	P	D8
E6	I	3.3 V	SPDIF	SPDIF_EXT_CLK	11	12	DGND	Ground	0 V	P	–
W6	I	3.3 V	Config	BOOT_MODE0	13	14	SYS_RST#	Config	3.3 V	I	–
V6	I	3.3 V	Config	BOOT_MODE1	15	16	ONOFF	Config	3.3 V	I	W21
K20	I/O	1.8 V	GPIO	GPIO3_IO16	17	18	DGND	Ground	0 V	P	–
E8	I/O	3.3 V	I2C	I2C1_SDA	19	20	GPIO3_IO17	GPIO	1.8 V	I/O	K22
E7	O	3.3 V	I2C	I2C1_SCL	21	22	GPIO3_IO18	GPIO	1.8 V	I/O	K21
–	P	0 V	Ground	DGND	23	24	I2C2_SCL	I2C	3.3 V	O	G7
A3	O	3.3 V	SAI	SAI1_MCLK	25	26	I2C2_SDA	I2C	3.3 V	I/O	F7
C1	O	3.3 V	SAI	SAI1_TXD7	27	28	DGND	Ground	0 V	P	–
B3	O	3.3 V	SAI	SAI1_TXD6	29	30	ECSPI1_SCLK	ECSPI	1.8 V / 3.3 V	O	D5
C2	O	3.3 V	SAI	SAI1_TXD5	31	32	ECSPI1_MISO	ECSPI	1.8 V / 3.3 V	I	B4
–	P	0 V	Ground	DGND	33	34	ECSPI1_MOSI	ECSPI	1.8 V / 3.3 V	O	A4
D2	O	3.3 V	SAI	SAI1_TXD4	35	36	ECSPI1_SS0	ECSPI	1.8 V / 3.3 V	O	D4
D1	O	3.3 V	SAI	SAI1_TXD3	37	38	DGND	Ground	0 V	P	–
B2	O	3.3 V	SAI	SAI1_TXD2	39	40	ECSPI2_SCLK	ECSPI	1.8 V / 3.3 V	O	C5
E2	O	3.3 V	SAI	SAI1_TXD1	41	42	ECSPI2_MISO	ECSPI	1.8 V / 3.3 V	I	B5
–	P	0 V	Ground	DGND	43	44	ECSPI2_MOSI	ECSPI	1.8 V / 3.3 V	O	E5
F2	O	3.3 V	SAI	SAI1_TXD0	45	46	ECSPI2_SS0	ECSPI	1.8 V / 3.3 V	O	A5
H1	O	3.3 V	SAI	SAI1_TXFS	47	48	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	49	50	SAI3_MCLK	SAI	3.3 V	O	D3
E1	O	3.3 V	SAI	SAI1_TXC	51	52	SAI3_RXD	SAI	3.3 V	I	F3
G1	I	3.3 V	SAI	SAI1_RXD7	53	54	SAI3_RXFS	SAI	3.3 V	I	G4
G2	I	3.3 V	SAI	SAI1_RXD6	55	56	SAI3_RXC	SAI	3.3 V	I	F4
F1	I	3.3 V	SAI	SAI1_RXD5	57	58	SAI3_TXD	SAI	3.3 V	O	C3
–	P	0 V	Ground	DGND	59	60	SAI3_TXFS	SAI	3.3 V	O	G3
J1	I	3.3 V	SAI	SAI1_RXD4	61	62	SAI3_TXC	SAI	3.3 V	O	C4
J2	I	3.3 V	SAI	SAI1_RXD3	63	64	DGND	Ground	0 V	P	–
H2	I	3.3 V	SAI	SAI1_RXD2	65	66	SAI2_MCLK	SAI	3.3 V	O	H5
L2	I	3.3 V	SAI	SAI1_RXD1	67	68	SAI2_RXD0	SAI	3.3 V	I	H6
K2	I	3.3 V	SAI	SAI1_RXD0	69	70	SAI2_RXFS	SAI	3.3 V	I	J4
L1	I	3.3 V	SAI	SAI1_RXFS	71	72	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	73	74	SAI2_RXC	SAI	3.3 V	I	H3
K1	O	3.3 V	SAI	SAI1_RXC	75	76	SAI2_TXD0	SAI	3.3 V	O	G5
M5	I	3.3 V	SAI	SAI5_RXD0	77	78	SAI2_TXFS	SAI	3.3 V	O	H4
L4	I	3.3 V	SAI	SAI5_RXD1	79	80	SAI2_TXC	SAI	3.3 V	O	J5
M4	I	3.3 V	SAI	SAI5_RXD2	81	82	DGND	Ground	0 V	P	–
K5	I	3.3 V	SAI	SAI5_RXD3	83	84	SAI5_RXC	SAI	3.3 V	O	L5
–	I	0 V	Ground	DGND	85	86	SAI5_RXFS	SAI	3.3 V	I	N4
W2	I	1.8 V	HDMI	HDMI_HPD	87	88	SAI5_MCLK	SAI	3.3 V	O	K4
W3	I/O	1.8 V	HDMI	HDMI_CEC	89	90	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	91	92	HDMI_TX0_P	HDMI	1.8 V	O	T1
–	P	0 V	Ground	DGND	93	94	HDMI_TX0_N	HDMI	1.8 V	O	T2
U2	O	1.8 V	HDMI	HDMI_TX1_P	95	96	DGND	Ground	0 V	P	–
U1	O	1.8 V	HDMI	HDMI_TX1_N	97	98	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	99	100	HDMI_TX2_P	HDMI	1.8 V	O	N2
–	P	0 V	Ground	DGND	101	102	HDMI_TX2_N	HDMI	1.8 V	O	N1
M1	O	1.8 V	HDMI	HDMI_TX3_P	103	104	DGND	Ground	0 V	P	–
M2	O	1.8 V	HDMI	HDMI_TX3_N	105	106	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	107	108	HDMI_AUXP	HDMI	1.8 V	I	V1
–	P	0 V	Ground	DGND	109	110	HDMI_AUXN	HDMI	1.8 V	I	V2
R3	O	1.8 V	HDMI	HDMI_DDC_SCL	111	112	DGND	Ground	0 V	P	–
P3	I/O	1.8 V	HDMI	HDMI_DDC_SDA	113	114	JTAG_TDI	JTAG	3.3 V	I	W5
V5	I	3.3 V	JTAG	JTAG_TMS	115	116	JTAG_TDO	JTAG	3.3 V	O	U5
T5	I	3.3 V	JTAG	JTAG_TCK	117	118	JTAG_TRST#	JTAG	3.3 V	I	U6
–	P	0 V	Ground	DGND	119	120	JTAG_MOD	JTAG	3.3 V	I	U7

3.1.1.2 TQMa8Mx pinout (continued)

Table 8: Pinout TQMa8Mx connector X3

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
P7	I/O	3.3 V	GPIO	GPIO1_IO05	1	2	GPIO1_IO07	DNC [3]	3.3 V	I/O	N6
N5	I/O	3.3 V	DNC [3]	GPIO1_IO06	3	4	GPIO1_IO08	GPIO	3.3 V	I/O	N7
L7	O	3.3 V	USB	USB1_OTG_PWR	5	6	GPIO1_IO09	GPIO	3.3 V	I/O	M6
K6	I	3.3 V	USB	USB1_OTG_OC	7	8	USB2_OTG_PWR	USB	3.3 V	O	K7
M7	I	3.3 V	USB	USB1_OTG_ID	9	10	USB2_OTG_OC	USB	3.3 V	I	J6
–	P	0 V	Ground	DGND	11	12	USB2_OTG_ID	USB	3.3 V	I	L6
A12	I	3.3 V	USB	USB1_RX_P	13	14	DGND	Ground	0 V	P	–
B12	I	3.3 V	USB	USB1_RX_N	15	16	DGND	Ground	0 V	P	–
D14	I	3.3 V	USB	USB1_VBUS	17	18	USB2_VBUS	USB	3.3 V	I	D9
C14	I	3.3 V	USB	USB1_ID	19	20	USB2_ID	USB	3.3 V	I	C9
–	P	0 V	Ground	DGND	21	22	USB2_RX_P	USB	3.3 V	I	A8
–	P	0 V	Ground	DGND	23	24	USB2_RX_N	USB	3.3 V	I	B8
A13	O	3.3 V	USB	USB1_TX_P	25	26	DGND	Ground	0 V	P	–
B13	O	3.3 V	USB	USB1_TX_N	27	28	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	29	30	USB2_TX_P	USB	3.3 V	O	A9
–	P	0 V	Ground	DGND	31	32	USB2_TX_N	USB	3.3 V	O	B9
A14	I/O	3.3 V	USB	USB1_DP	33	34	DGND	Ground	0 V	P	–
B14	I/O	3.3 V	USB	USB1_DN	35	36	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	37	38	USB2_DP	USB	3.3 V	I/O	A10
–	P	0 V	Ground	DGND	39	40	USB2_DN	USB	3.3 V	I/O	B10
C16	O	1.8 V	DSI	DSI_CLK_N	41	42	DGND	Ground	0 V	P	–
D16	O	1.8 V	DSI	DSI_CLK_P	43	44	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	45	46	DSI_D3_N	DSI	1.8 V	O	A15
–	P	0 V	Ground	DGND	47	48	DSI_D3_P	DSI	1.8 V	O	B15
A16	O	1.8 V	DSI	DSI_D1_N	49	50	DGND	Ground	0 V	P	–
B16	O	1.8 V	DSI	DSI_D1_P	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	DSI_D2_N	DSI	1.8 V	O	A18
–	P	0 V	Ground	DGND	55	56	DSI_D2_P	DSI	1.8 V	O	B18
A17	O	1.8 V	DSI	DSI_D0_N	57	58	DGND	Ground	0 V	P	–
B17	O	1.8 V	DSI	DSI_D0_P	59	60	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	61	62	PCIE1_TX_N	PCIE	3.3 V	O	J24
–	P	0 V	Ground	DGND	63	64	PCIE1_TX_P	PCIE	3.3 V	O	J25
E24	O	3.3 V	PCIE	PCIE2_TX_N	65	66	DGND	Ground	0 V	P	–
E25	O	3.3 V	PCIE	PCIE2_TX_P	67	68	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	69	70	PCIE1_RX_N	PCIE	3.3 V	I	H24
–	P	0 V	Ground	DGND	71	72	PCIE1_RX_P	PCIE	3.3 V	I	H25
D24	I	3.3 V	PCIE	PCIE2_RX_N	73	74	DGND	Ground	0 V	P	–
D25	I	3.3 V	PCIE	PCIE2_RX_P	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	PCIE1_REF_CLK_N	PCIE	3.3 V	I	K24
–	P	0 V	Ground	DGND	79	80	PCIE1_REF_CLK_P	PCIE	3.3 V	I	K25
F24	I	3.3 V	PCIE	PCIE2_REF_CLK_N	81	82	DGND	Ground	0 V	P	–
F25	I	3.3 V	PCIE	PCIE2_REF_CLK_P	83	84	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	85	86	GPIO1_IO01 [4]	DNC	3.3 V	I/O	T7
P4	I/O	3.3 V	DNC	TEMP_INT# [5]	87	88	GPIO1_IO00 [6]	DNC	3.3 V	I/O	T6
R4	I/O	3.3 V	DNC	WDOG1# [7]	89	90	SD2_VSELECT	uSDHC2	3.3 V	O	P5
N22	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA0	91	92	SD2_WP	uSDHC2	1.8 V / 3.3 V	I	M21
N21	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA1	93	94	SD2_CD#	uSDHC2	1.8 V / 3.3 V	I	L21
P22	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA2	95	96	SD2_RST#	uSDHC2	1.8 V / 3.3 V	O	R22
P21	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA3	97	98	SD2_CMD	uSDHC2	1.8 V / 3.3 V	I/O	M22
–	P	0 V	Ground	DGND	99	100	SD2_CLK	uSDHC2	1.8 V / 3.3 V	O	L22

3: GPIOs can be made available as on request. Please contact TQ-Support.
4: GPIO1_IO01, can be used as CLK2_IN.
5: TEMP_INT# (GPIO1_IO03), can be used as CLK1_IN.
6: GPIO1_IO00, can be used as CLK2_OUT.
7: WDOG1# (GPIO1_IO02), can be used as CLK1_OUT.

3.1.1.3 Boot Mode configuration

The Boot Mode configuration is set with DIP switches. The configuration can be read in by the i.MX 8M and the system controller on the MBa8Mx (via a 16 bit port expander).

With the MBa8Mx all boot media intended for the respective TQMa8Mx or TQMa8MxML/NL can be used.

- eMMC
- Micro SD card (on MBa8Mx)
- QSPI NOR flash (on TQMa8MxNL)
- NAND (on TQMa8MxNL)
- Serial downloader via USB-OTG1

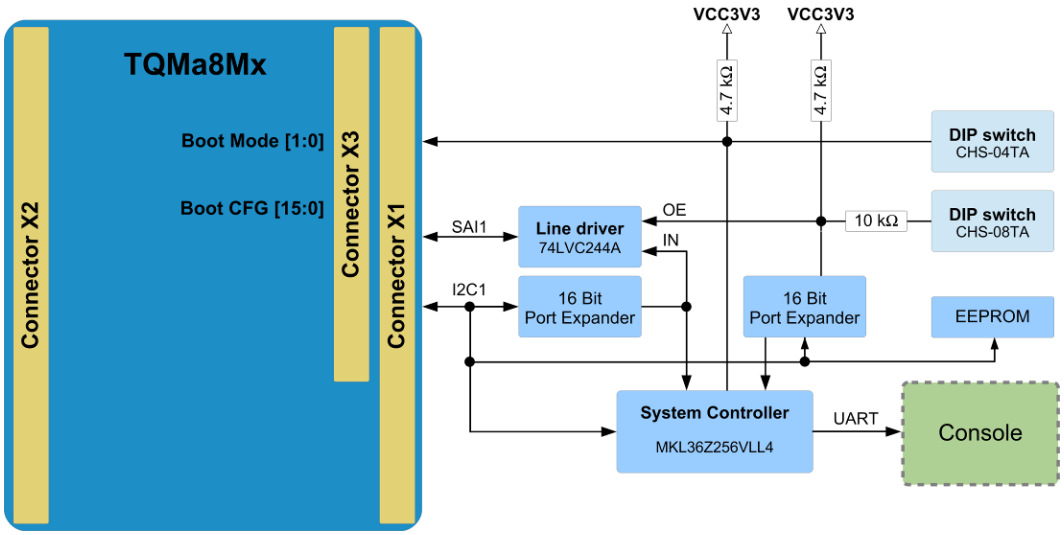


Figure 5: Block diagram Boot Mode

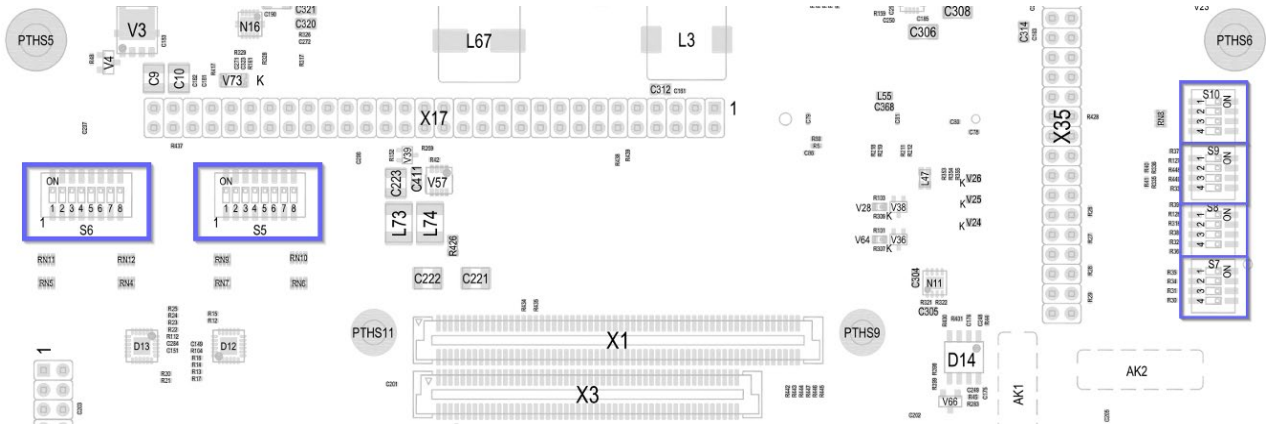


Figure 6: Position of DIP switches S5 ~ S10 on MBa8Mx

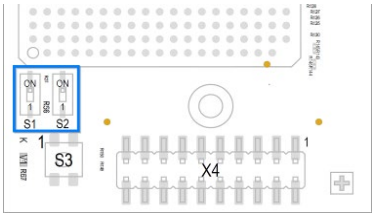


Figure 7: Position of DIP switches S1 and S2 on LGA adapter board

3.1.1.3 Boot Mode configuration (continued)

Information on the boot configurations of i.MX 8M, i.MX 8M Mini and i.MX 8M Nano can be found in the respective CPU documentation, see Table 49. For the TQMa8Mx and the TQMa8MxML, the boot source must be selected with signals BMODE[1:0], for the TQMa8MxNL with signals BMODE[3:0]. The following tables show all options.

Table 9: Boot Source options TQMa8Mx, TQMa8MxML

Boot Mode[1:0]	Boot Source
00	Boot from eFuses
01	Serial Downloader
10	Internal Boot
11	(Reserved)

Table 10: Boot Source options TQMa8MxNL

Boot Mode[3:0]	Boot Source
0000	Boot from eFuses
0001	Serial Downloader
0010	Boot from USDHC3
0011	Boot from USDHC2 (SD card)
010x	Boot from NAND (not supported)
0110	Boot from QSPI (3-Byte Read)
0111	Boot from QSPI (Hyperflash)
1000	Boot from eCSPI (not supported)
1001	(Reserved)

Table 11: DIP switches S1, S2, S9

DIP switch	Location	BOOT Mode[x]	Signal	Remark
S1	LGA adapter	3	TEST_MODE	S1 switches to 3.3 V
S2	LGA adapter	2	JTAG_TRST#	S2 switches to GND
S9-3 (5 ~ 6)	MBa8Mx	1	BOOT_MODE1	S9 switches to GND
S9-2 (3 ~ 4)	MBa8Mx	0	BOOT_MODE0	S9 switches to GND

Note: DIP switch position and voltage levels	
	DIP switches S5 to S10 on the MBa8Mx switch to GND and have pull-ups. DIP switch position “ON” means a low signal, DIP switch position “OFF” means a high signal. DIP switch S2 on the LGA adapter board switches to GND and has a pull-up. DIP switch S1 on the LGA adapter board switches to 3.3 V and has a pull-down.

Note: Boot Mode TQMa8MxNL	
	The TQMa8MxNL does not provide BOOT_CFG signals.

3.1.1.3 Boot Mode configuration (continued)

The following table shows the Boot Mode configuration for the TQMa8Mx.

Table 12: Boot Mode configuration, TQMa8Mx

DIP switch		Signal	eMMC		SD card		Serial Downloader	
			Switch	Level	Switch	Level	Switch	Level
S5	1	BOOT_CFG0	ON	Low	ON	Low	–	X
	2	BOOT_CFG1	ON	Low	ON	Low	–	X
	3	BOOT_CFG2	ON	Low	ON	Low	–	X
	4	BOOT_CFG3	ON	Low	ON	Low	–	X
	5	BOOT_CFG4	ON	Low	ON	Low	–	X
	6	BOOT_CFG5	ON	Low	ON	Low	–	X
	7	BOOT_CFG6	ON	Low	ON	Low	–	X
	8	BOOT_CFG7	ON	Low	ON	Low	–	X
S6	1	BOOT_CFG8	ON	Low	ON	Low	–	X
	2	BOOT_CFG9	ON	Low	ON	Low	–	X
	3	BOOT_CFG10	ON	Low	OFF	High	–	X
	4	BOOT_CFG11	ON	Low	ON	Low	–	X
	5	BOOT_CFG12	ON	Low	OFF	High	–	X
	6	BOOT_CFG13	OFF	High	ON	Low	–	X
	7	BOOT_CFG14	ON	Low	ON	Low	–	X
	8	BOOT_CFG15	ON	Low	ON	Low	–	X
S7	1	(NC)	–	X	–	X	–	X
	2	(NC)	–	X	–	X	–	X
	3	UART2_MUX_CTRL	–	X	–	X	–	X
	4	UART1_MUX_CTRL	–	X	–	X	–	X
S8	1	TQMa8M_SYS_RST#	OFF	High	OFF	High	–	X
	2	TQMa8M_ONOFF	OFF	High	OFF	High	–	X
	3	MBa8Mx 02xx: SD_MUX_CTRL MBa8Mx 03xx: I2C_ADDRESS_SW	–	X	ON	Low	–	X
	4	SPI_MUX_CTRL	–	X	–	X	–	X
S9	1	EN_VCC_FAN	–	X	–	X	–	X
	2	BOOT_MODE0	ON	Low	ON	Low	OFF	High
	3	BOOT_MODE1	OFF	High	OFF	High	ON	Low
	4	DSI_MUX_CTRL	–	X	–	X	–	X

3.1.1.3 Boot Mode configuration (continued)

The following table shows the Boot Mode configuration for the TQMa8MxML.

Table 13: Boot Mode configuration, TQMa8MxML

DIP switch		Signal	eMMC		SD card		Serial Downloader	
			Switch	Level	Switch	Level	Switch	Level
S5	1	BOOT_CFG0	ON	Low	ON	Low	–	X
	2	BOOT_CFG1	ON	Low	ON	Low	–	X
	3	BOOT_CFG2	ON	Low	ON	Low	–	X
	4	BOOT_CFG3	ON	Low	ON	Low	–	X
	5	BOOT_CFG4	ON	Low	ON	Low	–	X
	6	BOOT_CFG5	ON	Low	ON	Low	–	X
	7	BOOT_CFG6	ON	Low	ON	Low	–	X
	8	BOOT_CFG7	ON	Low	ON	Low	–	X
S6	1	BOOT_CFG8	ON	Low	ON	Low	–	X
	2	BOOT_CFG9	ON	Low	ON	Low	–	X
	3	BOOT_CFG10	ON	Low	OFF	High	–	X
	4	BOOT_CFG11	ON	Low	ON	Low	–	X
	5	BOOT_CFG12	ON	Low	OFF	High	–	X
	6	BOOT_CFG13	OFF	High	ON	Low	–	X
	7	BOOT_CFG14	ON	Low	ON	Low	–	X
	8	BOOT_CFG15	ON	Low	ON	Low	–	X
S7	1	(NC)	–	X	–	X	–	X
	2	(NC)	–	X	–	X	–	X
	3	UART2_MUX_CTRL	–	X	–	X	–	X
	4	UART1_MUX_CTRL	–	X	–	X	–	X
S8	1	TQMa8M_ONOFF	OFF	High	OFF	High	–	X
	2	TQMa8M_SYS_RST#	OFF	High	OFF	High	–	X
	3	MBa8Mx 02xx: SD_MUX_CTRL MBa8Mx 03xx: I2C_ADDRESS_SW	–	X	OFF	High	–	X
	4	SPI_MUX_CTRL	–	X	–	X	–	X
S9	1	EN_VCC_FAN	–	X	–	X	–	X
	2	BOOT_MODE0	ON	Low	ON	Low	OFF	High
	3	BOOT_MODE1	OFF	High	OFF	High	ON	Low
	4	DSI_MUX_CTRL	–	X	–	X	–	X

The following table shows the DIP switch settings required for the TQMa8Mx variants.

Table 14: TQMa8Mx variant selection, DIP switch S10

DIP switch		Signal	TQMa8Mx		TQMa8MxML		TQMa8MxNL	
			Switch	Level	Switch	Level	Switch	Level
S10	1	DIP_SW_SYSC_1	ON	Low	OFF	High	OFF	High
	2	DIP_SW_SYSC_2	ON	Low	OFF	High	OFF	High
	3	DIP_SW_SYSC_3	ON	Low	ON	Low	OFF	High
	4	DIP_SW_SYSC_4	ON	Low	ON	Low	OFF	High

3.1.2 System controller

The MBa8Mx provides a system controller that offers more possibilities over the debug console output, e.g.:

- Measuring supply voltages
- Reading the DIP switch positions
- Saving / reading configurations
- Keep reset control variable
- Customize power sequencing
- Display information on the console

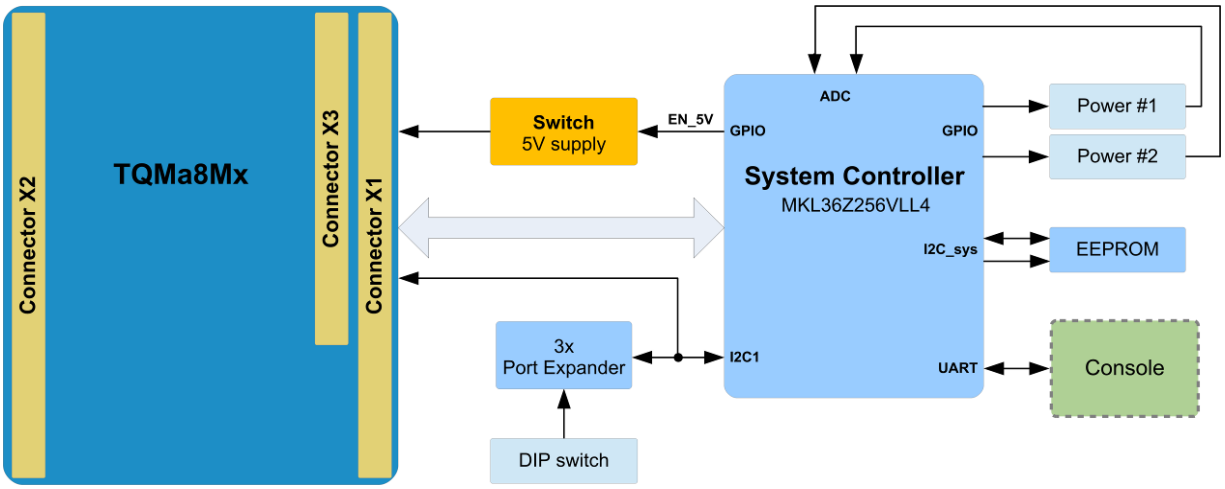


Figure 8: Block diagram System Controller on MBa8Mx

3.1.3 Temperature sensor

TQMa8Mx and MBa8Mx each have their own temperature sensor SE97BTP.
The sensors are controlled by I2C1 (TQMa8Mx) and I2C2 (MBa8Mx), see Table 16.
The I²C address of the sensor on the MBa8Mx can be changed by reassembling resistors.
When changing the address, care must be taken to avoid address conflicts with existing I²C devices.
The assembly options are documented in the MBa8Mx schematics.
The temperature sensor D11 is located on the top side of the MBa8Mx.

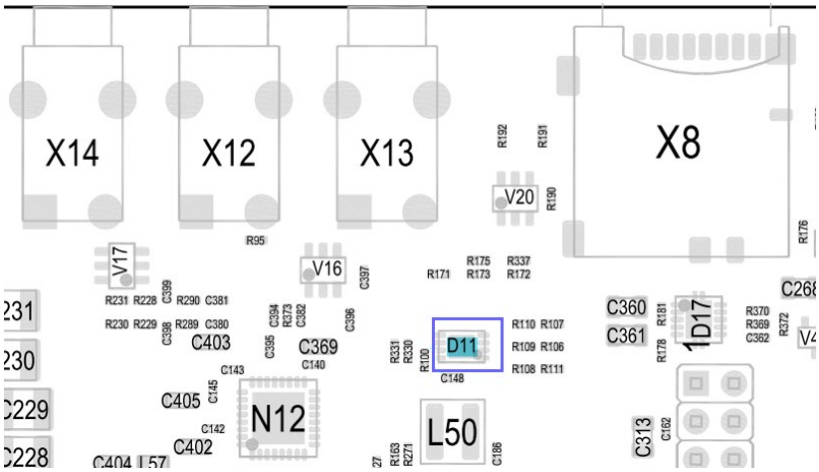


Figure 9: Position of temperature sensor SE97BTP on MBa8Mx

Table 15: Basic temperature sensor data SE97BTP

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C	+75 °C to +95 °C
			Max. ±2 °C	+40 °C to +125 °C
			Max. ±3 °C	–40 °C to +125 °C

3.1.4 I²C devices, address mapping

The TQMa8Mx provides up to four I²C buses, of which I2C1 is used on the TQMa8Mx.
The I²C device addresses on the TQMa8Mx must be taken into account if further I²C devices are connected on the carrier board.
I2C1, I2C2 and I2C3 are used on the MBa8Mx. I2C4 is not used on the MBa8Mx and is routed to header X35.
On the MBa8Mx a system controller and three port expanders are connected to I2C1.
An audio codec, a temperature sensor, the USB hub and the PCIe clock generator can be controlled by I2C2.
The following block diagram shows the I²C bus structure.

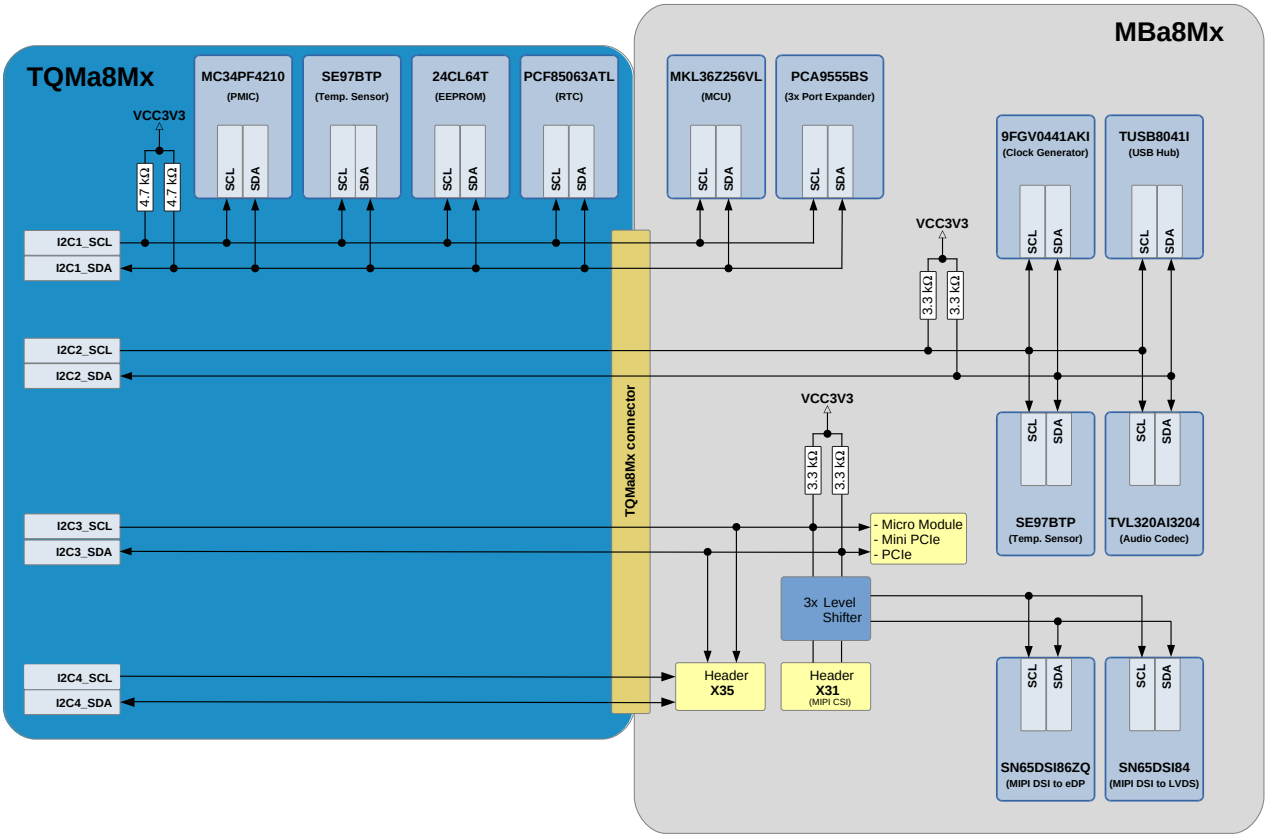


Figure 10: Block diagram I²C bus

3.1.4 I2C devices, address mapping (continued)

The following table shows the addresses used on the TQMa8Mx and the MBa8Mx.
Attention must be paid to which TQMa8Mx variant is used.
The addresses used are listed in the respective User's Manual of TQMa8Mx and TQMa8MxML_NL.

Table 16: I²C devices, address mapping on TQMa8Mx and MBa8Mx

Location	I²C bus	Device	Function	7-bit address	Remark
TQMa8Mx	I2C1	MC34PF4210	System Controller	0x08 / 000 1000b	Should not be altered
		PCF85063A	RTC	0x51 / 101 0001b	Optional
		M24LC64	EEPROM	0x57 / 101 0111b	–
		SE97BTP	Temperature sensor	0x1B / 001 1011b	–
			EEPROM	0x33 / 011 0011b	R/W access in Protected Mode
				0x53 / 101 0011b	R/W access in Normal Mode
MBa8Mx		MKL36Z256	System Controller	0x11 / 001 0001b	D5, should not be altered
		PCA9555BS	Port Expander	0x23 / 010 0011b	D31
		PCA9555BS	Port Expander	0x24 / 010 0100b	D13
		PCA9555BS	Port Expander	0x25 / 010 0101b	D12, only TQMa8Mx
				0x27 / 010 0111b	D12, only TQMa8MxML/NL
	I2C2	TLV320AIC3204	Audio Codec	0x18 / 001 1000b	N12
		SE97BTP	Temperature sensor	0x1F / 001 1111b	D11
			EEPROM	0x37 / 011 0111b	D11, R/W access in Protected Mode
				0x57 / 101 0111b	D11, R/W access in Normal Mode
		TUSB8041I	USB 3.0 Hub	0x44 / 100 0100b	D8
		9FGV0441A	Clock Generator	0x68 / 110 1000b	D10
	I2C3	SN65DSI86	MIPI DSI to eDP	0x2C / 010 1100b	D36
		SN65DSI84	MIPI DSI to LVDS	0x2D / 010 1101b	D37
		Socket	mPCIe	(Device dependent)	X28
		Slot	PCIe	(Device dependent)	X36
		Connectors	Mikro Bus	(Device dependent)	X20, X21
		Board-to-Board	0.8 mm connector	(Device dependent)	X31
		Connector	100 mil header	(Device dependent)	X35

3.1.5 GPIO port expander

Three port expanders PCA9555 with 16 ports each are provided on the MBa8Mx to control components like Reset signals for Mini PCIe, Ethernet, LCD, or audio codec. Boot configuration signals as well as enable and request signals are also connected to the port expanders. The port expanders are controlled by the I2C1 bus. The I²C address of the port expanders on the MBa8Mx can be adapted by rearranging resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices. The assembly options are documented in the MBa8Mx schematics.

After power-up, all ports are set as input and the connected component is thus deactivated.

The following table shows the signals controlled by the port expanders.

Table 17: Function of Port Expanders

Device	Port	Signal	Dir.	Default	Remark
Port Expander 1, D12	IO0_0	AUDIO_CODEC_RESET#	O	Low	Reset signal for audio codec TLV320AIC3204RHBT
	IO0_1	LCD_RESET#	O	Low	Reset signal on LVDS connector X23
	IO0_2	LCD_BLT_EN	O	Low	Backlight enable signal on LVDS connector X23
	IO0_3	LCD_PWR_EN	O	Low	Power Enable signal on LVDS connector X23
	IO0_4	eDP_IRQ	I	Low	Interrupt request signal for eDP
	IO0_5	HDMI_FAULT#	I	High	HDMI error feedback
	IO0_6	ETH1_IRQ	I	High	Interrupt for Ethernet
	IO0_7	ETH1_RESET#	O	Low	Reset signal for Ethernet
	IO1_0	MPCIE_WAKE#	O	Low	Wake signal PCIe
	IO1_1	SIM_CARD_DETECT	I	High	SIM card detection
	IO1_2	CAMx_PWR#	O	Low	Enable signal camera power supply
	IO1_3	INT_MIKRO_MODULE	I	High	Interrupt for Mikro Module
	IO1_4	MPCIE_DIS#	O	Low	Disable mPCIe
	IO1_5	MPCIE_RST#	O	Low	Mini PCIe Reset
	IO1_6	CAMx_RST#	O	Low	Camera Reset
	IO1_7	RESET_MIKRO_MODULE#	O	Low	Reset Mikro Module
Port Expander 2, D13	IO0_0	BOOT_CFG[0]	I	–	–
	IO0_1	BOOT_CFG[1]	I	–	–
	IO0_2	BOOT_CFG[2]	I	–	–
	IO0_3	BOOT_CFG[3]	I	–	–
	IO0_4	BOOT_CFG[4]	I	–	–
	IO0_5	BOOT_CFG[5]	I	–	–
	IO0_6	BOOT_CFG[6]	I	–	–
	IO0_7	BOOT_CFG[7]	I	–	–
	IO1_0	BOOT_CFG[8]	I	–	–
	IO1_1	BOOT_CFG[9]	I	–	–
	IO1_2	BOOT_CFG[10]	I	–	–
	IO1_3	BOOT_CFG[11]	I	–	–
	IO1_4	BOOT_CFG[12]	I	–	–
	IO1_5	BOOT_CFG[13]	I	–	–
	IO1_6	BOOT_CFG[14]	I	–	–
	IO1_7	BOOT_CFG[15]	I	–	–
Port Expander 3, D31	IO0_0	UART1_MUX_CTRL	I	–	–
	IO0_1	UART2_MUX_CTRL	I	–	–
	IO0_2	SD_MUX_CTRL	I	–	MBa8Mx revision 02xx: Toggle USDHC2 between X8 (SD card) and X17 (header)
		I2C_ADDRESS_SW	I	–	MBa8Mx revision 03xx: Toggle between TQMa8Mx and TQMa8MxML/NL due to address conflict.
	IO0_3	DSI_MUX_CTRL	I	–	–
	IO0_4	SPI_MUX_CTRL	I	–	–
	IO0_5	AVCC1V8_LVDS_EN	O	High	Enable signal for LVDS power supply
	IO0_6	LVDS_BRIDGE_EN	O	Low	Enable signal for LVDS bridge
	IO0_7	LVDS_BRIDGE_IRQ	I	Low	Interrupt for LVDS bridge
	IO1_0	SD_MUX_EN#	O	Low	Enable signal multiplexer for SD card
	IO1_1	EN_HDMI_TERM	O	Low	Enable signal HDMI
	IO1_2	DSI_MUX_OE#	O	Low	Enable signal multiplexer for DSI
	IO1_3	EN_eDP_BRIDGE_3V3	O	Low	Enable signal eDP bridge
	IO1_4	BOOT_CFG_OE#	O	Low	Enable signal Boot
	IO1_5	RST_USB_HUB#	O	Low	Reset signal USB hub
	IO1_6	PCIE_RST#	O	Low	Reset signal PCIe
	IO1_7	PCIE_WAKE#	O	Low	Wake signal PCIe

3.1.6 Power management and Reset

The system controller on the MBa8Mx is the control center of the Reset structure.
This ensures that the reset is enabled at the right time during power up. A Reset push button is available.
The voltages VCC3V3 and NVCC_1V8 become active when the power sequencing ends.

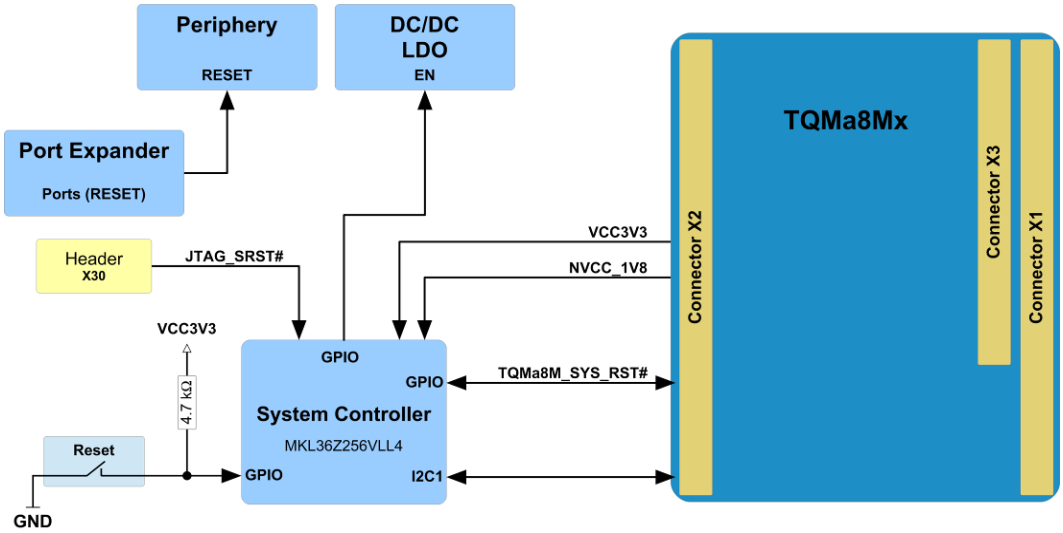


Figure 11: Block diagram MBa8Mx Reset structure

Attention: Malfunction caused by cross supply during Power-up	
	To avoid cross-supply and resulting errors in the power up/down sequence of the TQMa8Mx, the reset configuration to switch the buck regulators on or off must be taken into account. The voltages VCC3V3 and NVCC_1V8 become active when the power sequencing ends. A suitable circuitry can be taken from the MBa8Mx schematics.

For the TQMa8MxML and the TQMa8MxNL an additional reset button is available on the LGA adapter board (between MBa8Mx and TQMa8MxML). The reset button has no connection to the MBa8Mx and is directly connected to the PMIC of the TQMa8MxML. It allows to use the PMIC_RST# of the TQMa8MxML, which can be configured as warm or cold reset.
LED V1 on the LGA adapter board lights up when the TQMa8MxML triggers a reset.

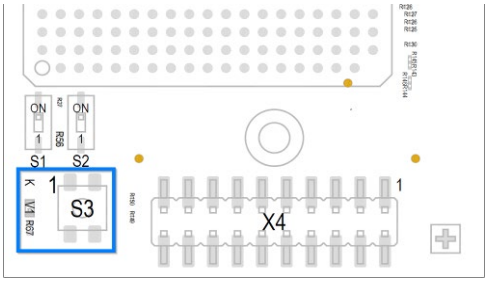


Figure 12: Position of PMIC_RST# button on LGA adapter board

3.1.7 Power supply

The power supply structure shows that VCC5V is always activated. 3.3 V for the system controller are derived from VCC5V.
The system controller in turn controls further voltages.
3.3 V, 5 V and 12 V are available at the three headers X17, X34 and X35 on the MBa8Mx, see chapter 3.2.12.
The following block diagram shows all voltages available on the mainboard, divided into three main paths, consisting of two LTC3851E and one TPS45335A.

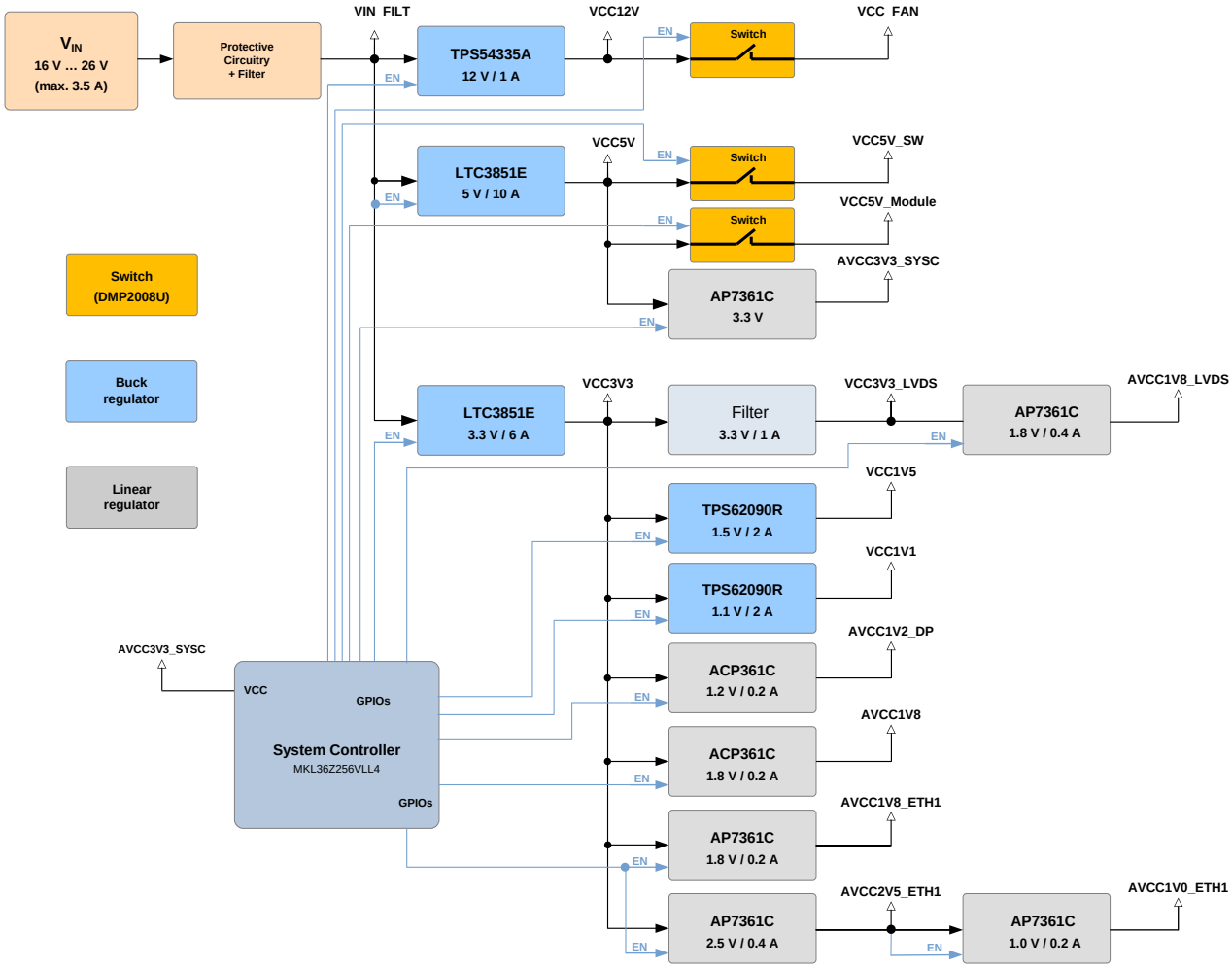


Figure 13: Block diagram power supply MBa8Mx revision 02xx.

Attention: Malfunction caused by cross supply	
	To avoid cross-supply and resulting errors in the power up/down sequence of the TQMa8Mx, the reset configuration to switch the buck regulators on or off must be taken into account. A suitable circuitry can be taken from the MBa8Mx schematics.

3.1.7 Power supply (continued)

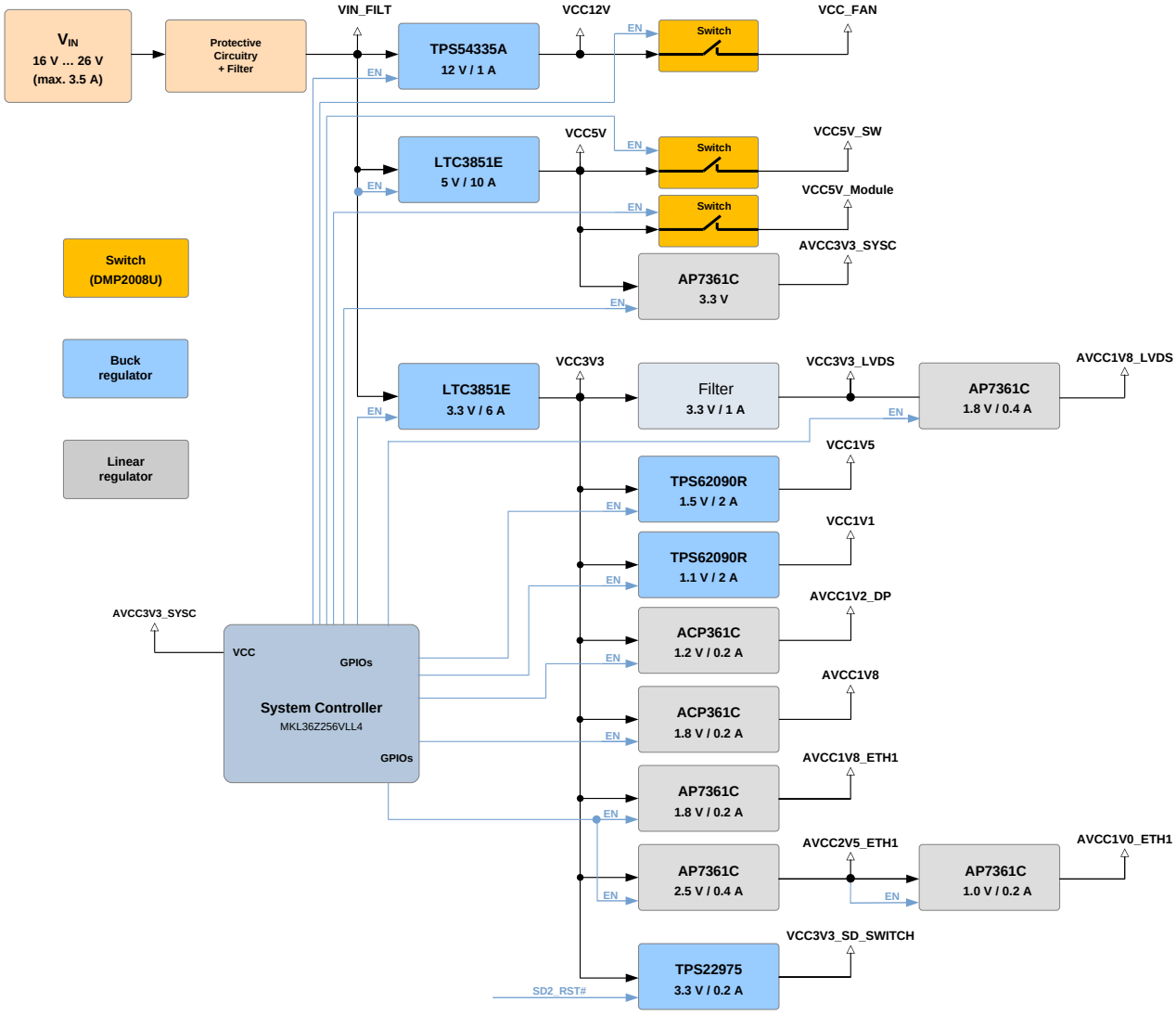


Figure 14: Block diagram power supply MBa8Mx revision 03xx.

Attention: Malfunction caused by cross supply	
	To avoid cross-supply and resulting errors in the power up/down sequence of the TQMa8Mx, the reset configuration to switch the buck regulators on or off must be taken into account. A suitable circuitry can be taken from the MBa8Mx schematics.

3.1.7.1 Protective circuitry

The protective circuit (see Figure 15) features the following characteristics:

- Overcurrent protection by fuse 10 A, Slow Blow
- Overvoltage protection
- PI filter
- Reverse polarity protection
- Capacitors for voltage smoothing

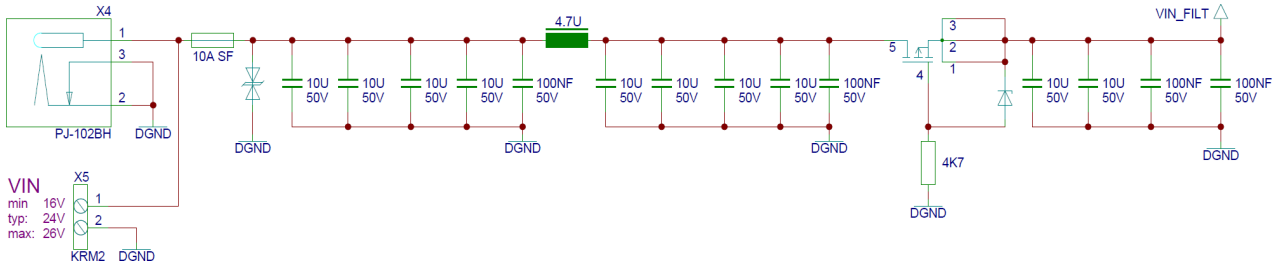


Figure 15: MBa8Mx protective circuit

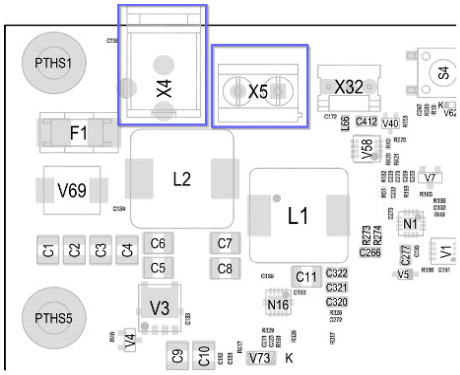


Figure 16: Position of X4 and X5 on MBa8Mx

The MBa8Mx including TQMa8Mx may consume significant current peaks when all supply voltages are loaded with maximum current, e.g., by external loads on the headers and slots. The sole operation of the MBa8Mx including the TQMa8Mx consumes approx. 8.5 watts when the i.MX 8M operates at 100 % load.

3.1.8 RTC backup

In case of power failure or power down a lithium battery type CR2032 on the MBa8Mx supplies the RTC on the TQMa8Mx via pin LICELL (X2-4), which can be supplied with 2.1 V to 3.7 V, typical 3.0 V. The TQMa8Mx features an i.MX 8M-internal RTC or a discrete RTC PCF85063A. The RTC is supplied at pin LICELL (X2-4) in either way.

3.2 Communication interfaces

3.2.1 Ethernet 1000 Base-T (RGMII)

The Ethernet MAC of the TQMa8Mx is connected to a TI PHY DP83867 on the MBa8Mx. The RGMII interface includes PHY reset and interrupt signals. The PHY DP83867 provides boot straps to start with configurable default values. All boot straps can be customized on the MBa8Mx by assembly options. Further information can be found in the MBa8Mx schematics.
The achievable data throughput is influenced by the system load and the software platform used.

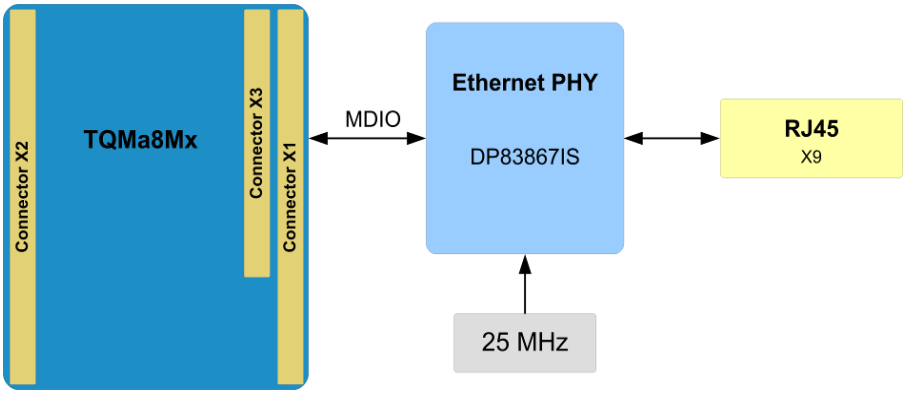


Figure 17: Block diagram Ethernet 1000 Base-T

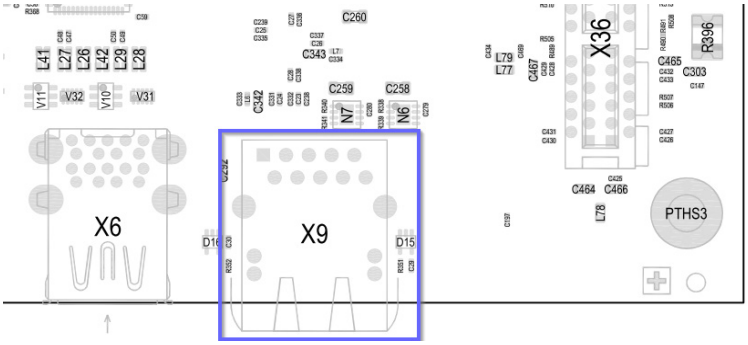


Figure 18: Position of RJ-45 Ethernet connector X9

Table 18: Pinout RJ-45 Ethernet connector, X9

Pin	Signal
1	ENET1_A+
2	ENET1_A–
3	ENET1_B+
6	ENET1_B–
4	ENET1_C+
5	ENET1_C–
7	ENET1_D+
8	ENET1_D–

3.2.2 SD card interface

The SD card interface of MBa8Mx revision 02xx differs from the interface on MBa8Mx revision 03xx, but position and pinout of SD card connector X8 are identical on both MBa8Mx revisions.

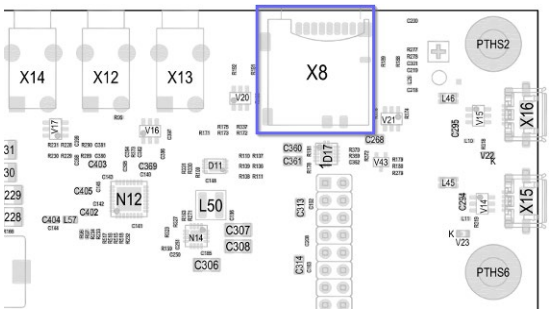


Figure 19: Position of Micro SD card holder, X8

Table 19: Pinout Micro SD card holder, X8

Pin	Signal	Remark
1	SD2_DATA2	10 Ω in series, ESD protection, 10 kΩ PU to VCC3V3 [8]
2	SD2_DATA3	10 Ω in series, + ESD protection, 10 kΩ PU to VCC3V3 [8] not populated
3	SD2_CMD	10 Ω in series, ESD protection, 10 kΩ PU to VCC3V3 [8]
4	VCC3V3	–
5	SD2_CLK	ESD protection
6	DGND	–
7	SD2_DATA0	10 Ω in series, ESD protection, 10 kΩ PU to VCC3V3 [8]
8	SD2_DATA1	10 Ω in series, ESD protection, 10 kΩ PU to VCC3V3 [8]
SW1	SD2_CD#	ESD protection, 10 kΩ PU to VCC3V3 [8]
SW2	DGND	–
M1 ~ M4	SHIELD	Connected to DGND

The following two chapters describe the connections on the respective MBa8Mx revision.

8: PU to VCC3V3 on MBa8Mx revision 02xx, PU to VCC3V3_SD_SWITCH on MBa8Mx revision 03xx.

3.2.2.1 SD card interface, MBa8Mx revision 02xx

The USDHC2 interface of the TQMa8Mx is connected with a four bit interface to a Micro SD card holder. Alternatively, the USDHC2 interface can be routed to header X17 on the MBa8Mx with DIP switch S8-3 (5~6). The SD card can be used as boot source, see chapter 3.1.1.3. All data signals are ESD protected.

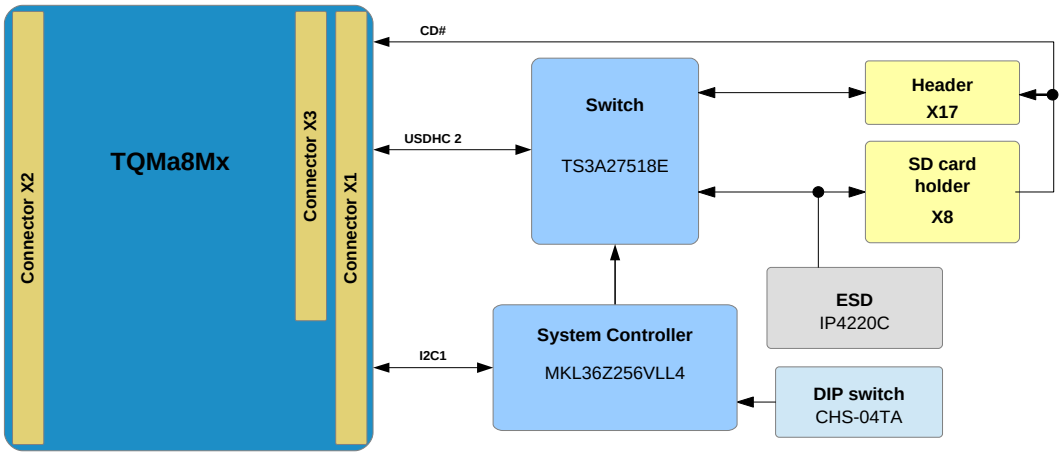


Figure 20: Block diagram SD card interface, MBa8Mx revision 02xx

Table 20: USDHC2 routing, DIP switch S8 on MBa8Mx revision 02xx

DIP switch	Signal	ON (logic "0")	OFF (logic "1")
S8-3 (5~6)	SD_MUX_CTRL	SD card holder X8	X17

3.2.2.2 SD card interface, MBa8Mx revision 03xx

A Micro SD card holder with a four bit interface is connected to the USDHC2 interface of the TQMa8Mx. From SD card can be booted, see chapter 3.1.1.3. All data lines are ESD protected.

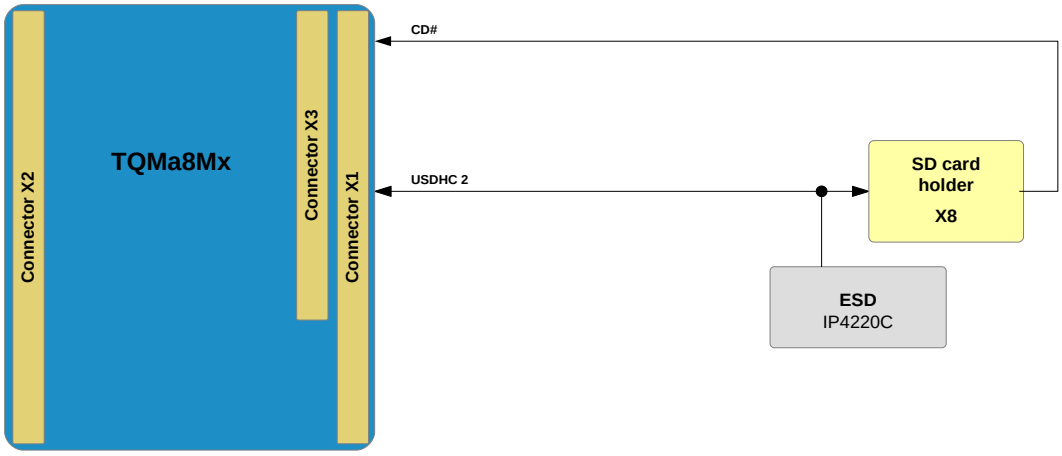


Figure 21: Block diagram SD card interface, MBa8Mx revision 03xx

3.2.3 USB

The TQMa8Mx provides two USB3.0 / 2.0 controller with integrated PHYs. Both controller are OTG interfaces and routed to the TQMa8Mx connectors. The USB1 interface is configured as OTG and routed to USB Micro B connector X19 on the MBa8Mx.

A USB 3.0 hub TUSB8041I is connected to the USB2 interface on the MBa8Mx, which provides four USB 3.0 / 2.0 host interfaces.

The USB connectors are supplied with 5 V via power switches. The current is monitored and can be switched off in case of an overload and/or overheating.

USB 3.0 Host 1 & 2 of the TUSB8041I are connected to a Dual USB 3.0 Type A socket (X6) on the MBa8Mx.

USB Host 3 is routed to the LVDS-CMD connector X23, USB Host 4 is routed to the Mini PCIe connector X28 on the MBa8Mx.

The USB2 port of the TQMa8Mx provides a theoretical data rate of 5 Gbit/s. This is divided among the connected ports. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

The USB hub is programmed via bootstrapping or I²C. Further information can be found in the TUSB8041I data sheet and the MBa8Mx schematics.

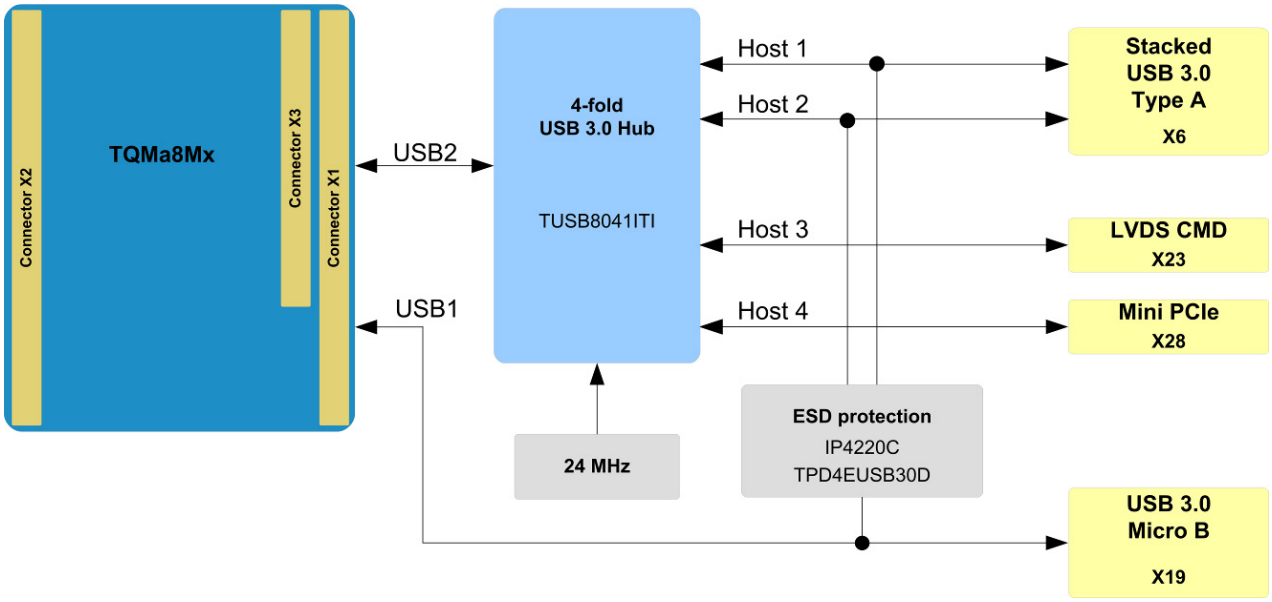


Figure 22: Block diagram USB

Table 21: Pinout USB Host3, 20-pin DF19G, X23

Pin	Pin name	Signal	Remark
11	VBUS	VBUS_H3	100 µF + EMI filter
12	DGND	DGND	–
13	D–	USB_H3_DN	Common Mode Choke in series + ESD protection
14	D+	USB_H3_DP	Common Mode Choke in series + ESD protection
15	DGND	DGND	–

Table 22: Pinout USB Host4, Mini PCIe connector, X28

Pin	Pin name	Signal	Remark
36	D–	USB_H4_DN	Common Mode Choke in series
38	D+	USB_H4_DP	Common Mode Choke in series

Table 23: USB Host power supply

Parameter	Min.	Typical	Max.	Remark
Voltage	4.75 V	5 V	5.25 V	Ensured at max. 900 mA (per VBUS)
Current	–	500 mA	900 mA	–

3.2.3.1 USB 3.0 Host 1&2

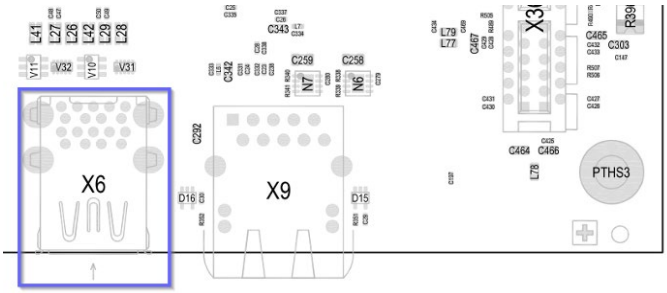


Figure 23: Position of USB 3.0 Host 1&2, X6

The following table shows the pinout of stacked USB connector X6.

Table 24: Pinout USB 3.0 Host1&2, stacked Type A, X6

Pin	Pin name	Signal	Remark	Position
1	VBUS_H2	VBUS_2	100 µF + EMI filter	Bottom
2	USB_H2_D–	D–_2	Common Mode Choke in series	
3	USB_H2_D+	D+_2	Common Mode Choke in series	
4	DGND	GND_2	–	
5	USB_H2_SSRX–	SSRX–_2	Common Mode Choke in series	
6	USB_H2_SSRX+	SSRX+_2	Common Mode Choke in series	
7	DGND	GND-DRAIN_2	–	
8	USB_H2_SSTX–	SSTX–_2	100 nF + Common Mode Choke in series	
9	USB_H2_SSTX+	SSTX+_2	100 nF + Common Mode Choke in series	
10	VBUS_H1	VBUS_1	100 µF + EMI filter	Top
11	USB_H1_D–	D–_1	Common Mode Choke in series	
12	USB_H1_D+	D+_1	Common Mode Choke in series	
13	DGND	GND_1	–	
14	USB_H1_SSRX–	SSRX–_1	Common Mode Choke in series	
15	USB_H1_SSRX+	SSRX+_1	Common Mode Choke in series	
16	DGND	GND-DRAIN_1	–	
17	USB_H1_SSTX–	SSTX–_1	100 nF + Common Mode Choke in series	
18	USB_H1_SSTX+	SSTX+_1	100 nF + Common Mode Choke in series	
M1 ~ M4	Shield	DGND	–	–

3.2.3.2 USB 3.0 OTG

The USB1 interface is configured as OTG and routed to USB Micro B connector X19 on the MBa8Mx.
The USB1 port of the TQMa8Mx provides a theoretical data rate of 5 Gbit/s.
Depending on the software and hardware used, the effective read and write rates of the ports may vary.

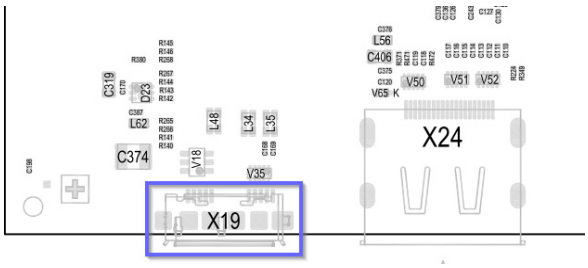


Figure 24: Position of USB OTG, X19

The following table shows the pinout of USB OTG connector X19.

Table 25: Pinout USB2 OTG (USB Micro B), X19

Pin	Pin name	Signal	Remark
1	VBUS	VBUS_OTG	100 µF + EMI filter
2	D–	USB1_D–	Common Mode Choke in series
3	D+	USB1_D+	Common Mode Choke in series
4	ID	USB1_ID	–
5	GND	DGND	–
6	SSTX–	USB1_SSTX–	Common Mode Choke in series
7	SSTX+	USB1_SSTX+	Common Mode Choke in series
8	GND_DRAIN	DGND	–
9	SSRX–	USB1_SSRX–	100 nF + Common Mode Choke in series
10	SSRX+	USB1_SSRX+	100 nF + Common Mode Choke in series
M1 ~ M6	Shield	DGND	–

3.2.4 PCIe

The i.MX 8M provides two PCIe 2.0 interfaces with one lane each.
PCIe 1 is routed to PCIe connector X36 on the MBa8Mx. Additionally, I2C3 is routed to X36.
The PCIe interface is supplied with the required clock by a clock generator 9FGB0441.
The maximum current for the provided voltages is specified in Table 26.

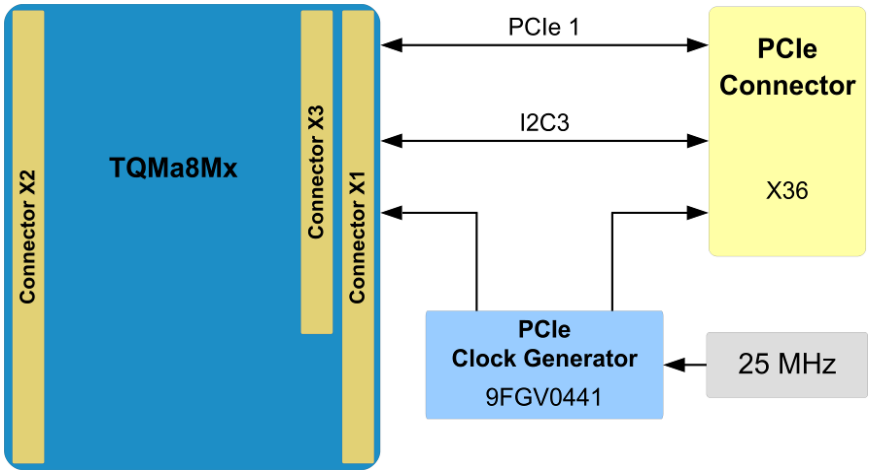


Figure 25: Block diagram PCIe

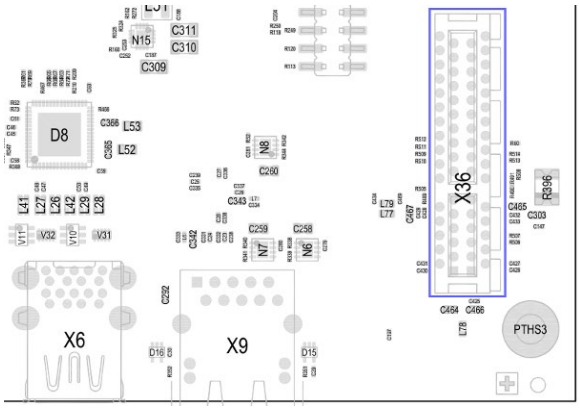


Figure 26: Position of PCIe, X36

The voltages provided for the PCIe card must not exceed the currents specified in the following table.

Table 26: Maximum permitted currents PCIe

Voltage rail	Nominal voltage	I_{max}
VCC12V_PCIE	12 V	0.5 A
VCC3V3_PCIE	3.3 V	3 A

3.2.4 PCIe (continued)

Table 27: Pinout PCIe, X36

Remark	Signal	Pin		Signal	Remark
Max. current see Table 26	VCC12V_PCIE	B1	A1	GND	–
Max. current see Table 26	VCC12V_PCIE	B2	A2	VCC12V_PCIE	Max. current see Table 26
Max. current see Table 26	VCC12V_PCIE	B3	A3	VCC12V_PCIE	Max. current see Table 26
–	DGND	B4	A4	DGND	–
–	I2C3_SCL	B5	A5	(NC)	–
I^2C address see Table 16	I2C3_SDA	B6	A6	(NC)	–
–	DGND	B7	A7	(NC)	–
Max. current see Table 26	VCC3V3_PCIE	B8	A8	(NC)	–
–	(NC)	B9	A9	VCC3V3_PCIE	Max. current see Table 26
Max. current see Table 26	VCC3V3_PCIE	B10	A10	VCC3V3_PCIE	Max. current see Table 26
–	PCIE_WAKE#	B11	A11	PCIE_RST#	–
Key notch					
(NC)	(NC)	B12	A12	DGND	–
–	DGND	B13	A13	PCIe_ETH_CLK_P	Signal from Clock Generator
–	PCIE1_TXN_P	B14	A14	PCIe_ETH_CLK_N	Signal from Clock Generator
–	PCIE1_TXN_N	B15	A15	DGND	–
–	DGND	B16	A16	PCIE1_RXN_P	–
10 kΩ PU to VCC3V3_PCIE	PCIE_PRSNT#	B17	A17	PCIE1_RXN_N	–
–	DGND	B18	A18	DGND	–
(NC)	(NC)	B19	A19	(NC)	(NC)
(NC)	(NC)	B20	A20	DGND	–
–	DGND	B21	A21	(NC)	(NC)
–	DGND	B22	A22	(NC)	(NC)
(NC)	(NC)	B23	A23	DGND	–
(NC)	(NC)	B24	A24	DGND	–
–	DGND	B25	A25	(NC)	(NC)
–	DGND	B26	A26	(NC)	(NC)
(NC)	(NC)	B27	A27	DGND	–
(NC)	(NC)	B28	A28	DGND	–
–	DGND	B29	A29	(NC)	(NC)
(NC)	(NC)	B30	A30	(NC)	(NC)
10 kΩ PU to VCC3V3_PCIE	PCIE_PRSNT#	B31	A31	DGND	–
–	DGND	B32	B32	(NC)	(NC)

3.2.5 Mini PCIe

The MBa8Mx provides a Mini PCIe slot for standard compliant full-size cards of 50.95 × 30 mm².
PCIe 2 is routed to PCIe connector X28 on the MBa8Mx. Additionally, I2C3 is routed to X28.
The Mini PCIe interface is supplied with the required clock by a clock generator 9FGB0441.
The maximum current for the provided voltages is specified in Table 28.

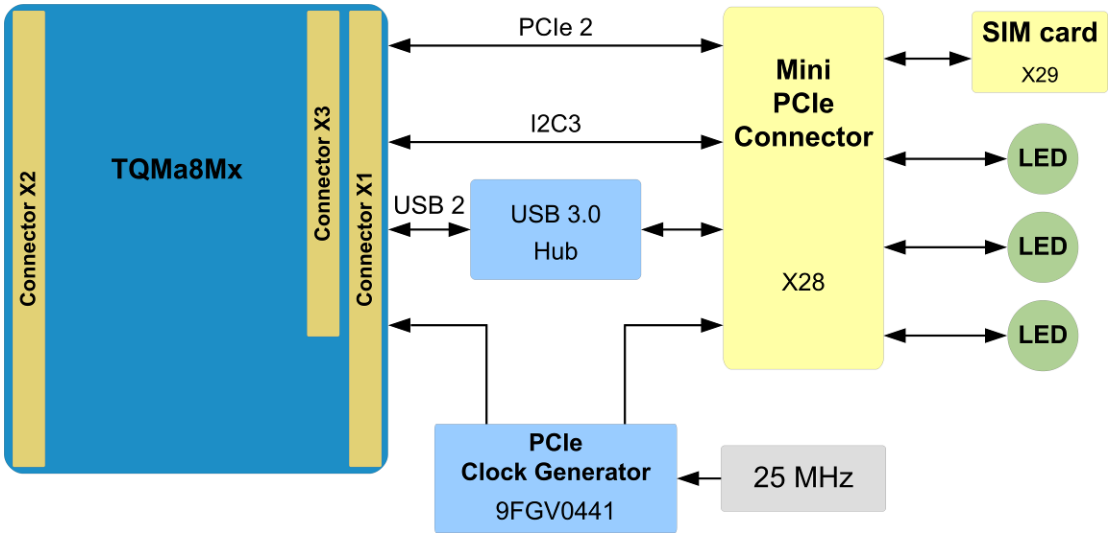


Figure 27: Block diagram Mini PCIe

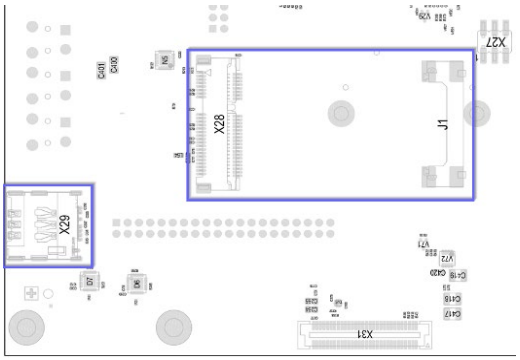


Figure 28: Position of Mini PCIe, X28, SIM card, X29

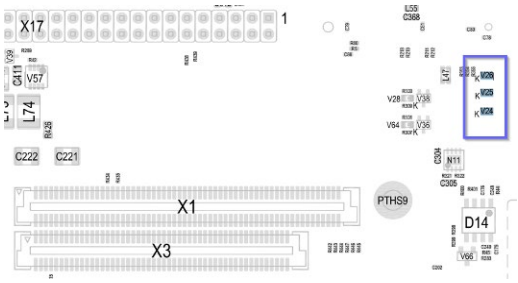


Figure 29: Position of Mini PCIe, status LEDs

The voltages provided for the Mini PCIe card must not exceed the currents specified in the following table.

Table 28: Maximum permitted currents Mini PCIe

Voltage rail	Nominal voltage	I_{max}
VCC3V3_MPCIE	3.3 V	1.1 A
VCC1V5_MPCIE	1.5 V	0.375 A

3.2.5 Mini PCIe (continued)

Table 29: Pinout Mini PCIe, X28

Remark	Signal	Pin		Signal	Remark
–	MPCIE_WAKE#	1	2	VCC3V3_MPCIE	Max. current see Table 28
–	(NC)	3	4	DGND	–
–	(NC)	5	6	VCC1V5_MPCIE	Max. current see Table 28
–	(NC)	7	8	VCC	SIM card signal, see Table 30
–	DGND	9	10	DATA	SIM card signal, see Table 30
Signal from Clock Generator	MPCIE_CLK_N	11	12	CLK	SIM card signal, see Table 30
Signal from Clock Generator	MPCIE_CLK_P	13	14	RST	SIM card signal, see Table 30
–	DGND	15	16	VPP	SIM card signal, see Table 30
Key notch					
–	(NC)	17	18	DGND	–
–	(NC)	19	20	MPCIE_DIS#	–
–	DGND	21	22	MPCIE_RST#	–
–	PCIE2_RXN_N	23	24	VCC3V3_MPCIE	Max. current see Table 28
–	PCIE2_RXN_P	25	26	DGND	–
–	DGND	27	28	VCC1V5_MPCIE	Max. current see Table 28
–	DGND	29	30	I2C3_SCL	–
100 nF in series	PCIE2_TXN_N	31	32	I2C3_SDA	I^2C address, see Table 16
100 nF in series	PCIE2_TXN_P	33	34	DGND	–
–	DGND	35	36	USB_H4_DN	Common mode choke in series
–	DGND	37	38	USB_H4_DP	Common mode choke in series
Max. current see Table 28	VCC3V3_MPCIE	39	40	DGND	–
Max. current see Table 28	VCC3V3_MPCIE	41	42	LED_WWAN#	Green LED
–	DGND	43	44	LED_WLAN#	Green LED
–	(NC)	45	46	LED_WPAN	Green LED
–	(NC)	47	48	VCC1V5_MPCIE	Max. current see Table 28
–	(NC)	49	50	DGND	–
–	(NC)	51	52	VCC3V3_MPCIE	Max. current see Table 28

A SIM card holder is also provided, which is wired as follows:

Table 30: Pinout SIM card holder, X29

Pin	Signal
C1	VCC
C2	RST
C3	CLK
C4	(n/a)
C5	DGND
C6	VPP
C7	DATA
DL	SIM_CARD_DETECT
DS	DGND

3.2.6 PCIe clock supply

A PCIe clock generator 9FGV0441 on the MBa8Mx provides a stable clock for the PCIe and Mini PCIe interfaces. Further information can be found in the MBa8Mx schematics.

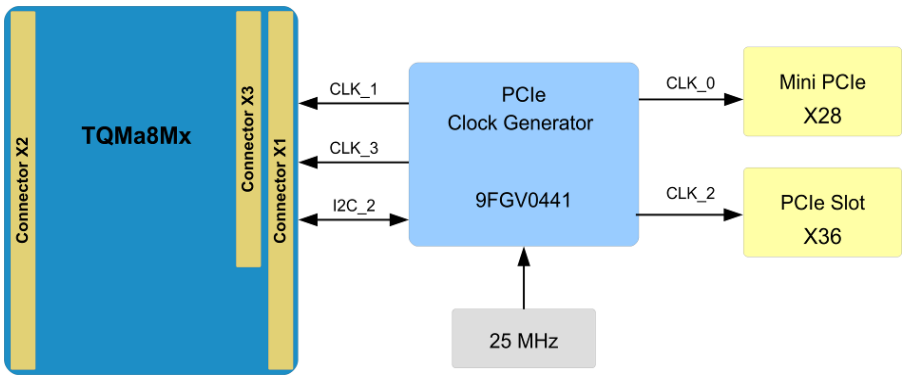


Figure 30: Block diagram PCIe clock supply

3.2.7 Debug interface

The TQMa8Mx provides four UARTs, which are used as follows:

- UART1 for CPU (i.MX 8M) debug
- UART2 for MCU (in i.MX 8M) debug
- UART3 as additional debug interface
- UART4 is routed to header X17

In addition, all four UARTs are routed to header X17. The destination of a certain UART can be set with DIP switch S7.

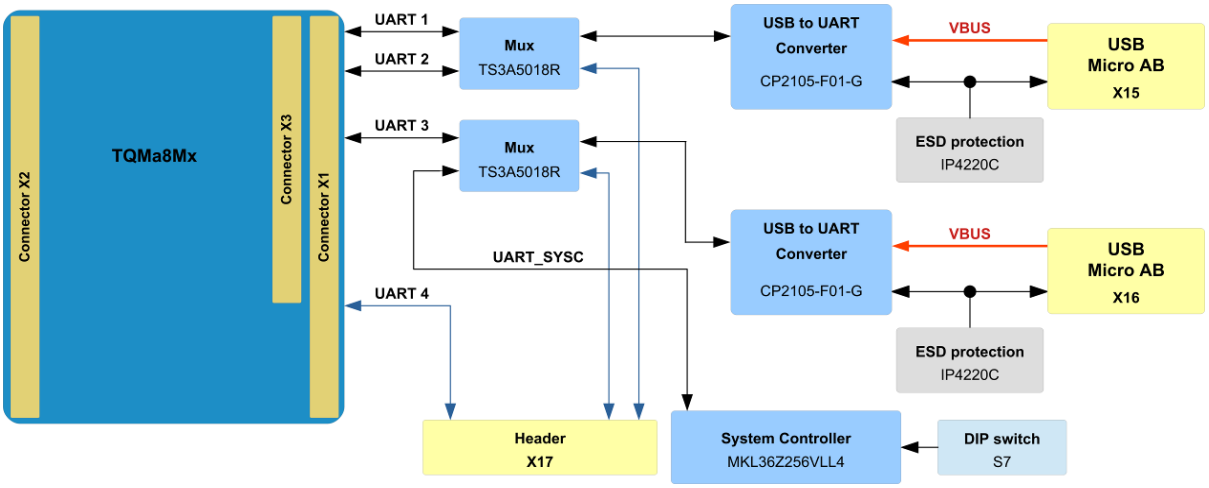


Figure 31: Block diagram UARTs

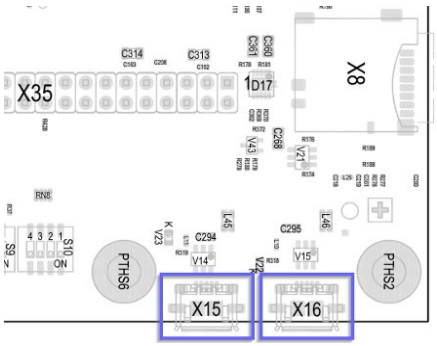


Figure 32: Position of Debug UARTs/USB, X15, X16

Table 31: Pinout Debug USB, X15, X16

Pin	Signal	Remark
1	VBUS	UART1 is converted to USB and routed to X15 UART3 is converted to USB and routed to X16
2	D–	
3	D+	
4	(NC)	
5	DGND	
M1 ~ M6	DGND	

3.2.8 Display interfaces

The i.MX 8M provides the following graphics interfaces:

- HD Transmitter Controller
  - o HDMI
  - o DisplayPort
  - o eDP (no longer equipped since board revision 0301)
- MIPI-DSI Controller

Not all interfaces can be used simultaneously. The interfaces are connected as follows:

- HDMI permanently connected, accessible via standard Type A connector
- MIPI DSI via switch:
  - o Either LVDS via DF19 connector
  - o Or embedded DisplayPort accessible via bridge via DisplayPort connector

3.2.8.1 HDMI

The i.MX 8M provides an HDMI 2.0a interface. This is provided on the MBa8Mx via a standardized interface (HDMI Type A).

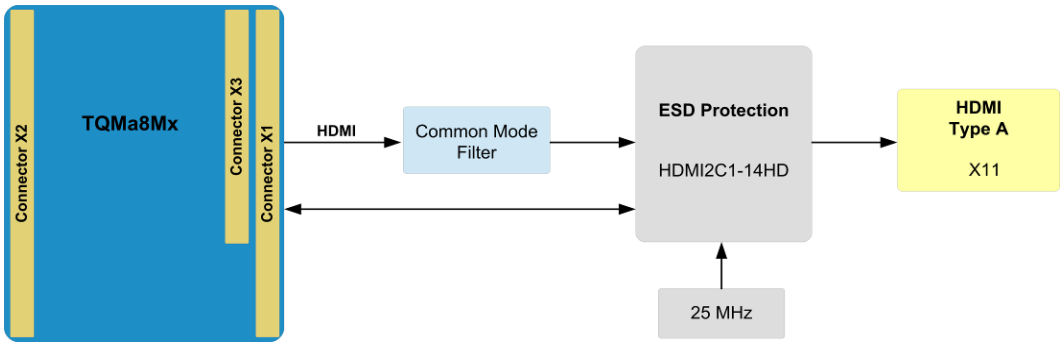


Figure 33: Block diagram HDMI

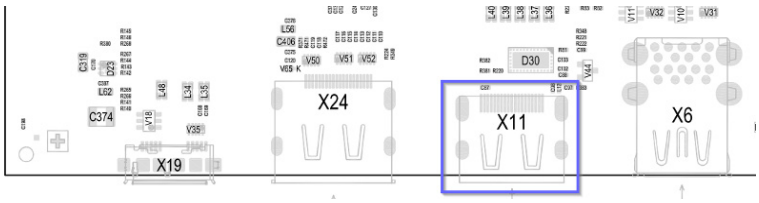


Figure 34: Position of HDMI, X11

3.2.8.1 HDMI (continued)

Table 32: Pinout HDMI connector X11

Pin	Signal	Remark
1	DAT_D2+	100 nF + Common Mode Choke in series + ESD protection
2	DGND	–
3	DAT_D2–	100 nF + Common Mode Choke in series + ESD protection
4	DAT_D1+	100 nF + Common Mode Choke in series + ESD protection
5	DGND	–
6	DAT_D1–	100 nF + Common Mode Choke in series + ESD protection
7	DAT_D0+	100 nF + Common Mode Choke in series + ESD protection
8	DGND	–
9	DAT_D0–	100 nF + Common Mode Choke in series + ESD protection
10	DAT_CK+	100 nF + Common Mode Choke in series + ESD protection
11	DGND	–
12	DAT_CK–	100 nF + Common Mode Choke in series + ESD protection
13	CEC	ESD protection
14	Unity	–
15	SCL	1.8 kΩ to 5V_OUT + ESD protection
16	SDA	1.8 kΩ to 5V_OUT + ESD protection
17	DGND	–
18	5V_OUT	100 nF to DGND + ESD protection
19	HPD	ESD protection
M1…M4	DGND	–

Note: I^2C pull-ups	
	Signals HDMI_DDC_SCL and HDMI_DDC_SDA (X11-15, X11-16) should be pulled-up to 5 V on the carrier board with 1.5 kΩ to 2 kΩ. See above table.

3.2.8.2 MIPI DSI to eDP

Since board revision 0301 eDP is no longer equipped. The MIPI DSI port was switched by a software-controlled switch to an eDP port or an LVDS connector on the MBa8Mx.

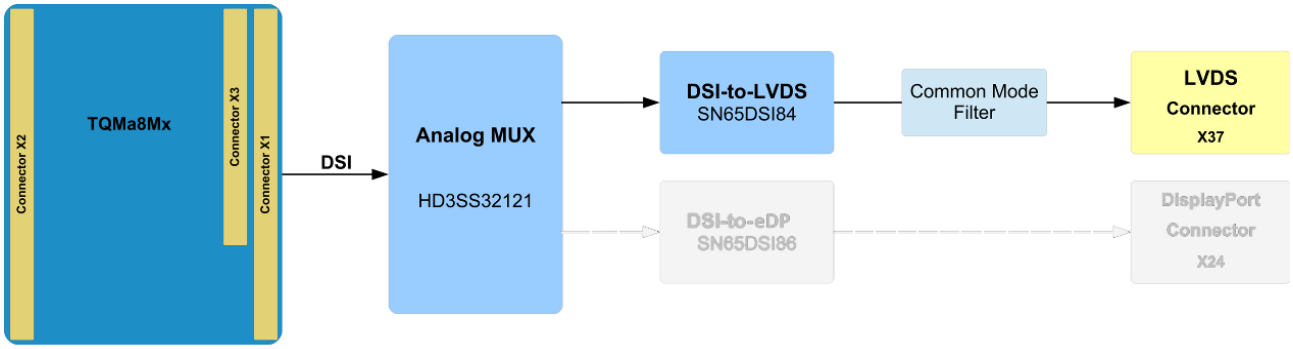


Figure 35: Block diagram eDP

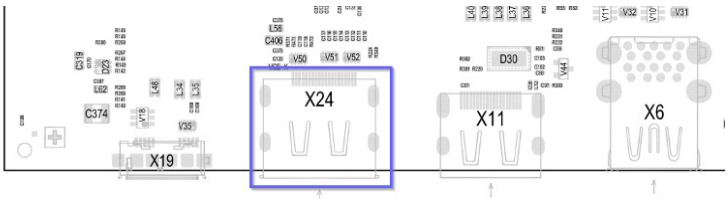


Figure 36: Position of eDP, X24

Table 33: Pinout eDP, X24

Pin	Signal	Remark
1	eDP_ML0+	100 nF in series + ESD protection
2	DGND	–
3	eDP_ML0–	100 nF in series + ESD protection
4	eDP_ML1+	100 nF in series + ESD protection
5	DGND	–
6	eDP_ML1–	100 nF in series + ESD protection
7	eDP_ML2+	100 nF in series + ESD protection
8	DGND	–
9	eDP_ML2–	100 nF in series + ESD protection
10	eDP_ML3+	100 nF in series + ESD protection
11	DGND	–
12	eDP_ML3–	100 nF in series + ESD protection
13	CFG1	1 MΩ to DGND
14	CFG2	0 Ω to DGND
15	eDP_AUX_CH+	100 nF in series + ESD protection + 100 kΩ PD
16	DGND	–
17	eDP_AUX_CH–	100 nF in series + ESD protection + 100 kΩ PU to 3.3 V
18	HPD	51 kΩ in series + ESD protection
19	DGND	–
20	3.3 V	VCC3V3
M1 ~ M4	DGND	–

3.2.8.3 MIPI DSI to LVDS

The MIPI DSI port provided by the TQMa8Mx can be switched by a software-controlled switch to an eDP port, or an LVDS connector on the MBa8Mx.

The LVDS interface is provided via two DF19 connectors. The first connector (30-pin, X37) provides the LVDS data signals as well as 3.3 V and 5 V. The second (20-pin, X23, not shown in the following block diagram) provides additional power supplies, 5 V and 12 V, as well as control lines and USB signals.

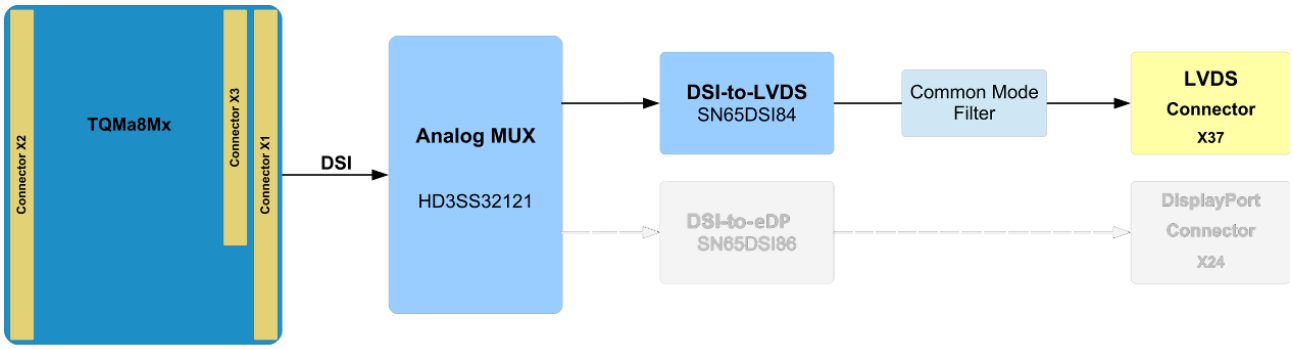


Figure 37: Block diagram LVDS

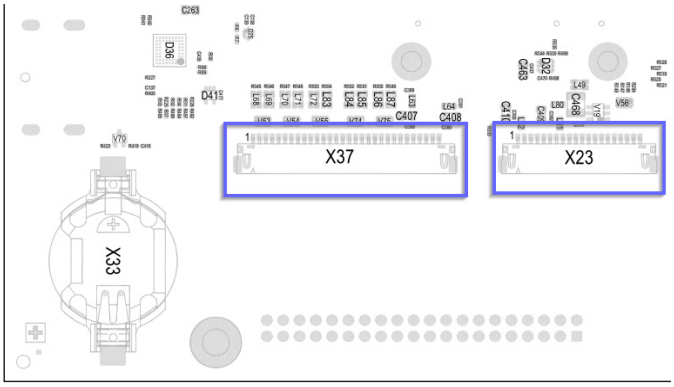


Figure 38: Position of LVDS connectors, X37, X23

3.2.8.3 MIPI DSI to LVDS (continued)

Table 34: Pinout LVDS signal connector, X37

Pin	Signal	Remark
1	MIPI_DSI0_DATA0–	Common Mode Choke in series + ESD protection
2	MIPI_DSI0_DATA0+	Common Mode Choke in series + ESD protection
3	MIPI_DSI0_DATA1–	Common Mode Choke in series + ESD protection
4	MIPI_DSI0_DATA1+	Common Mode Choke in series + ESD protection
5	MIPI_DSI0_DATA2–	Common Mode Choke in series + ESD protection
6	MIPI_DSI0_DATA2+	Common Mode Choke in series + ESD protection
7	DGND	–
8	MIPI_DSI0_CLOCK–	Common Mode Choke in series + ESD protection
9	MIPI_DSI0_CLOCK+	Common Mode Choke in series + ESD protection
10	MIPI_DSI0_DATA3–	Common Mode Choke in series + ESD protection
11	MIPI_DSI0_DATA3+	Common Mode Choke in series + ESD protection
12	MIPI_DSI1_DATA0–	Common Mode Choke in series + ESD protection
13	MIPI_DSI1_DATA0+	Common Mode Choke in series + ESD protection
14	DGND	–
15	MIPI_DSI1_DATA1–	Common Mode Choke in series + ESD protection
16	MIPI_DSI1_DATA1+	Common Mode Choke in series + ESD protection
17	DGND	–
18	MIPI_DSI1_DATA2–	Common Mode Choke in series + ESD protection
19	MIPI_DSI1_DATA2+	Common Mode Choke in series + ESD protection
20	MIPI_DSI1_CLOCK–	Common Mode Choke in series + ESD protection
21	MIPI_DSI1_CLOCK+	Common Mode Choke in series + ESD protection
22	MIPI_DSI1_DATA3–	Common Mode Choke in series + ESD protection
23	MIPI_DSI1_DATA3	Common Mode Choke in series + ESD protection
24	DGND	–
25 … 27	VCC5V_LVDS	5 V, max. 1 A
28 … 30	VCC3V3_LVDS	3.3 V, max. 1 A
M1, M2	DGND	–

Table 35: Pinout LVDS control connector, X23

Pin	Signal	Remark
1 … 3	VCC12V	12 V, max. 1 A
4 … 6	DGND	–
7 … 8	VCC5V_SW	5 V, max. 1 A
9 … 10	DGND	–
11	VBUS_H3	–
12	DGND	–
13	USB_H3_DN	Common Mode Choke in series + ESD protection
14	USB_H3_DP	Common Mode Choke in series + ESD protection
15	DGND	–
16	LCD_RESET#	ESD protection
17	LCD_BLT_EN	ESD protection
18	LCD_PWR_EN	ESD protection
19	PWM3 (LCD_CONTRAST)	ESD protection
20	DGND	–
M1, M2	DGND	–

3.2.9 MIPI CSI

The MIPI CSI port provided by the TQMa8Mx is routed to connector X31 on the MBa8Mx.

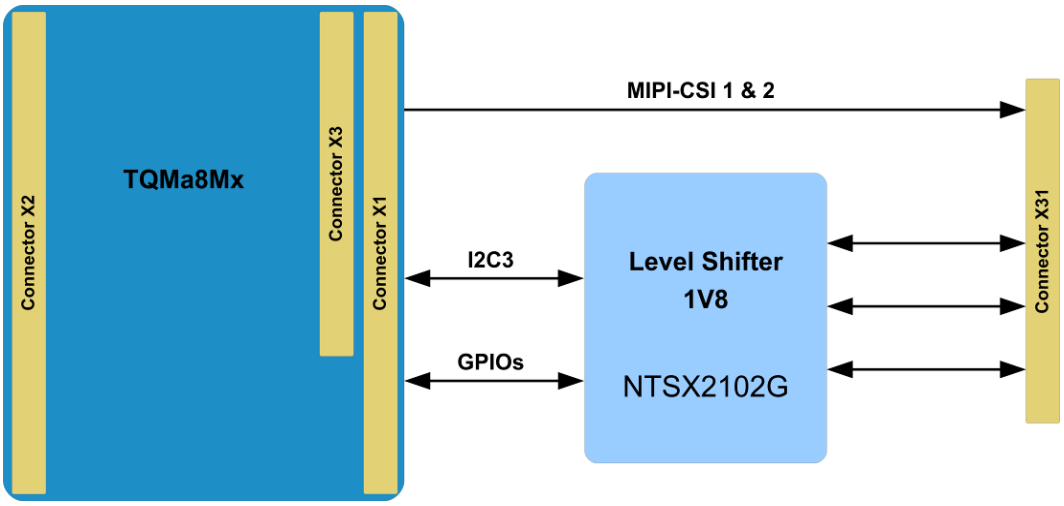


Figure 39: Block diagram MIPI CSI

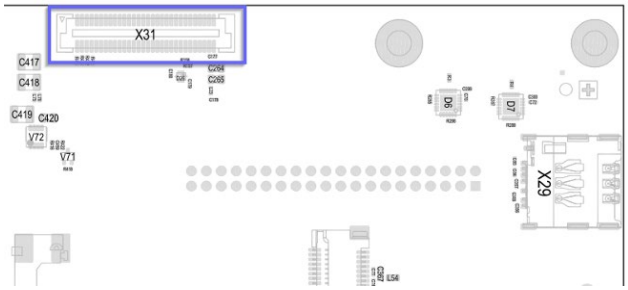


Figure 40: Position of MIPI CSI, X31

3.2.9 MIPI CSI (continued)

Table 36: Pinout MIPI CSI, X31

Remark	Signal	Pin		Signal	Remark
–	GND	1	2	GND	–
–	CAMx_PWR_1V8#	3	4	CAMx_PWR_1V8#	–
–	CAMx_RST_1V8#	5	6	CAMx_RST_1V8#	–
–	CAM0_TRIGGER	7	8	CAM1_TRIGGER	–
–	CAM0_SYNC	9	10	CAM1_SYNC	–
–	(NC)	11	12	(NC)	–
–	DGND	13	14	DGND	–
–	MIPI_CSI1_D3_N	15	16	MIPI_CSI2_D3_N	–
–	MIPI_CSI1_D3_P	17	18	MIPI_CSI2_D3_P	–
–	DGND	19	20	DGND	–
–	MIPI_CSI1_D2_N	21	22	MIPI_CSI2_D2_N	–
–	MIPI_CSI1_D2_P	23	24	MIPI_CSI2_D2_P	–
–	DGND	25	26	DGND	–
–	MIPI_CSI1_D1_N	27	28	MIPI_CSI2_D1_N	–
–	MIPI_CSI1_D1_P	29	30	MIPI_CSI2_D1_P	–
–	DGND	31	32	DGND	–
–	MIPI_CSI1_D0_N	33	34	MIPI_CSI2_D0_N	–
–	MIPI_CSI1_D0_P	35	36	MIPI_CSI2_D0_P	–
–	DGND	37	38	DGND	–
–	MIPI_CSI1_CLK_N	39	40	MIPI_CSI2_CLK_N	–
–	MIPI_CSI1_CLK_P	41	42	MIPI_CSI2_CLK_P	–
–	DGND	43	44	DGND	–
–	I2C3_SCL_1V8	45	46	I2C3_SDA_1V8	–
–	I2C3_SDA_1V8	47	48	I2C3_SCL_1V8	–
–	DGND	49	50	DGND	–
PWM3 optional	SAI1_TXD7 / PWM3	51	52	(NC)	–
–	DGND	53	54	DGND	–
–	(NC)	55	56	5V	VCC5V_SW
–	(NC)	57	58	5V	VCC5V_SW
–	(NC)	59	60	5V	VCC5V_SW

3.2.10 Audio

The i.MX 8M provides up to five SAI audio ports. The protocols I²S, AC97 and TDM are supported. The largest audio path with 16 channels (8Rx / 8Tx) is SAI1, which is fully available on the headers. SAI3 (1Rx / 1Tx) is used on the MBa8Mx.

A Texas Instruments TLV320AIC3204 audio codec is assembled. It is configured as I²S via SAI and controlled by the TQMa8Mx I2C2 bus. The audio codec provides microphone, line in and line out signals at 3.5 mm jacks on the MBa8Mx.

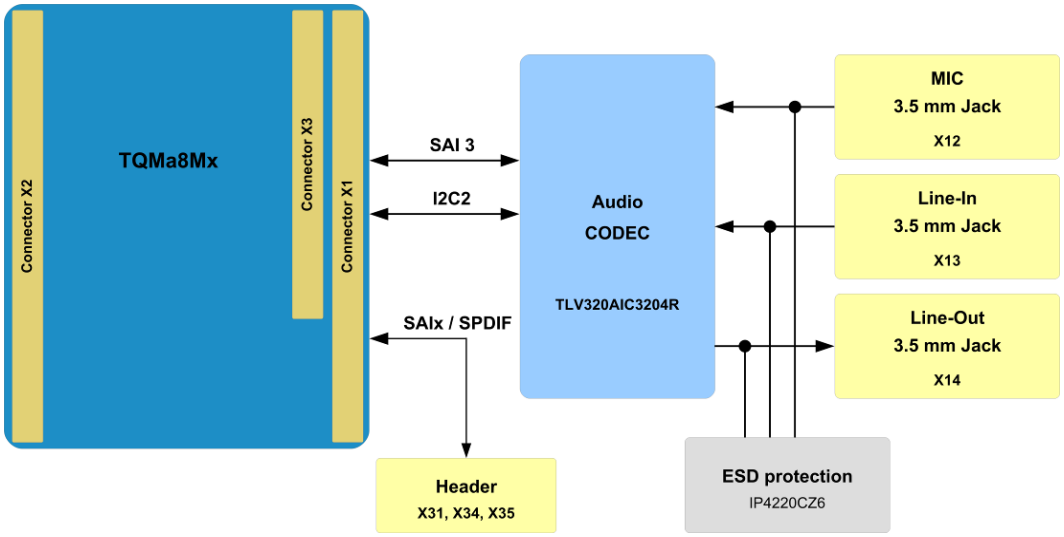


Figure 41: Block diagram audio interface

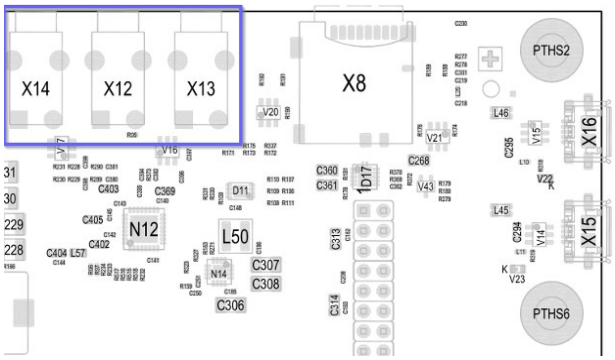


Figure 42: Position of audio jacks, X12, X13, X14

Table 37: Pinout audio connectors, X12, X13, X14

Jack	Pin	Signal	Remark
X12 MIC	1	AGND_AUDIO	–
	2A, 2B	MIC_IN	2.2 kΩ in series to MIC_BIAS; ESD protection
	3	AGND_AUDIO	10 kΩ to AGND_AUDIO, right channel not used
X13 Line-In	1	AGND_AUDIO	–
	2A, 2B	LINE_IN_L	470 nF in series; ESD protection
	3	LINE_IN_R	470 nF in series; ESD protection
X14 Line-Out	1	AGND_AUDIO	–
	2A, 2B	AUDIO_OUT_L	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; ESD protection. Optional connection to HP_L
	3	AUDIO_OUT_R	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; ESD protection. Optional connection to HP_R

3.2.11 mikroBUS™

The MBa8Mx provides a mikroBUS™ for system extensions. The mikroBUS™ is an open standard for which numerous extension boards are available, including:

- 3G modules
- GPS modules
- Stepper motors
- Sensors of all kinds

mikroBUS™ modules require 3.3 V and 5 V, which are provided by the MBa8Mx. PTC fuses limit the current load at 750 mA. No maximum values are specified for the power consumption. Since mikroBUS™ modules are low-power modules, the current consumption is limited to 500 mA per supply rail. The I2C3 bus is used at the mikroBUS™. SPI and UART interfaces are connected via a switch in order to use them on headers or to be able to disconnect the mikroBUS™.

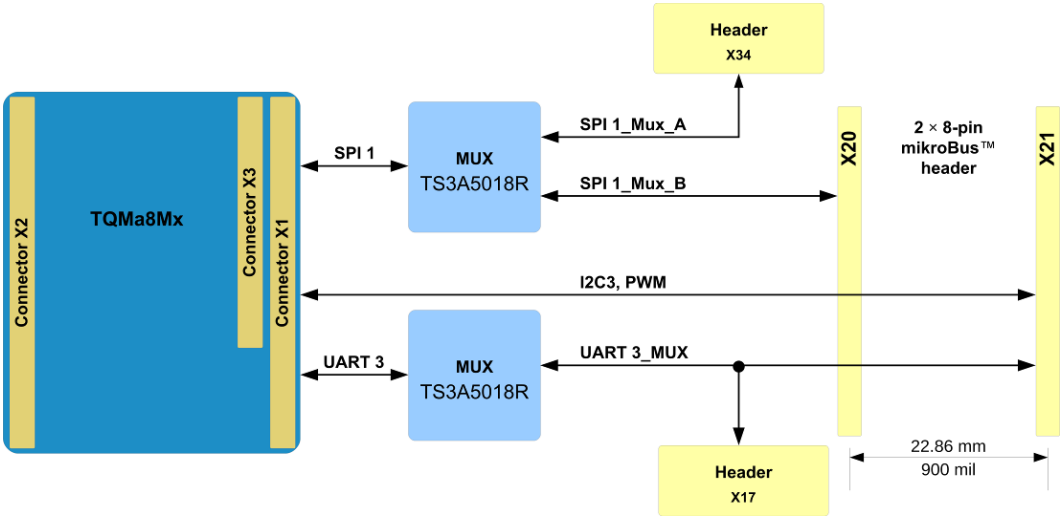


Figure 43: Block diagram mikroBUS™

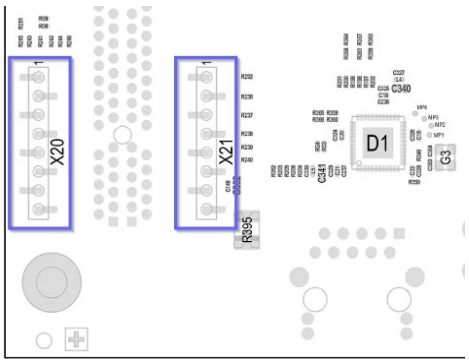


Figure 44: Position of mikroBUS™

3.2.11 mikroBUS™ (continued)

All mikroBUS™ modules, which meet the mikroBUS™ specification can be used on the MBa8Mx.
Dimensions of the mikroBUS™ modules are as follows:

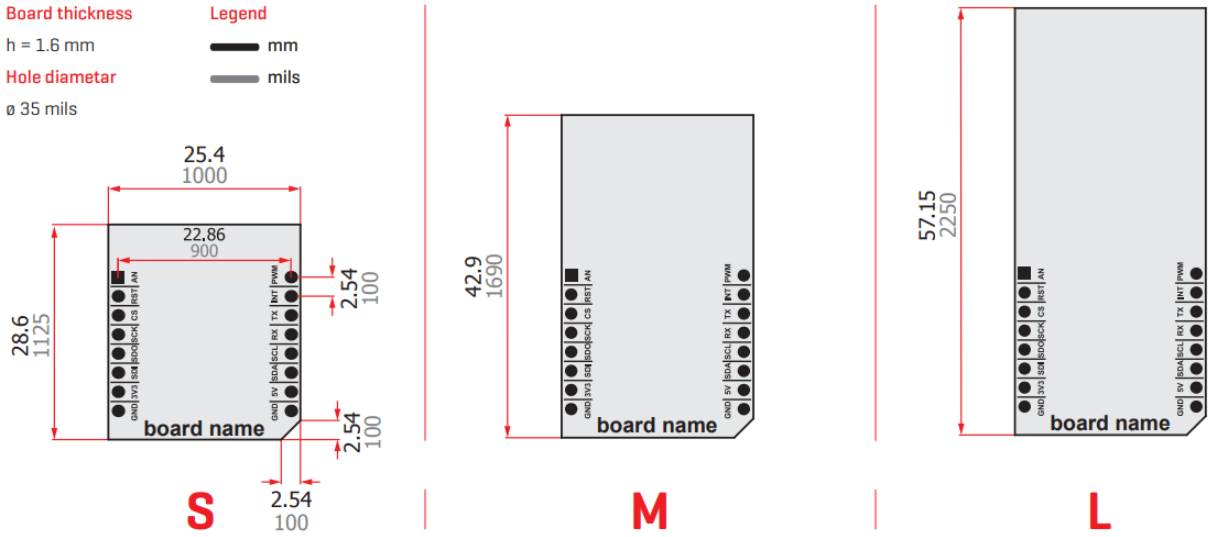


Figure 45: mikroBUS™ module dimensions

The following table shows the signals of mikroBUS™ connectors X20 and X21.

Table 38: Pinout mikroBUS™ connectors, X20, X21

X20			
Remark	Signal	Name	Pin
10 kΩ to DGND optional 10 kΩ to 3.3 V	0 V	AN	1
–	RESET_MIKRO_MODULE#	RST	2
–	SPI1_SS0_MUX_B	CS	3
–	SPI1_SCLK_MUX_B	SCK	4
–	SPI1_MISO_MUX_B	MISO	5
–	SPI1_MOSI_MUX_B	MOSI	6
750 mA PTC fuse	VCC3V3	+3.3V	7
–	DGND	GND	8

X21			
Pin	Name	Signal	Remark
1	PWM	PWM3	100 Ω in series
2	INT	INT_MIKRO_MODULE	–
3	RX	UART3_RXD_MUX	–
4	TX	UART3_TXD_MUX	–
5	SCL	I2C3_SCL	–
6	SDA	I2C3_SDA	–
7	+5V	VCC5V_SW	750 mA PTC fuse
8	GND	DGND	–

All signals except power supply and PWM (which is equipped with 100 Ω in series) are equipped with 0 Ω in series.
This allows signal lines to be reassigned if the pinout is different. Detailed information can be found in the MBa8Mx schematics.

3.2.12 Headers

The MBa8Mx features three 100 mil pin headers. All unused signals are made available on these pin headers.
In addition to the signals, 3.3 V, 5 V and 12 V are available on each pin header.
Each of the three voltage rails can be loaded with 3 A each, i.e. 3 A in total on all three pin headers.

3.2.12 Headers (continued)

Table 39: Pinout Header 1, X17

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
P	3.3 V	Power	VCC3V3	1	2	VCC5V	Power	5 V	P
P	3.3 V	Power	VCC3V3	3	4	VCC5V	Power	5 V	P
P	12 V	Power	VCC12V	5	6	GPIO1_IO02	GPIO	3.3 V	I/O
I/O	3.3 V	GPIO	GPIO1_IO01	7	8	GPIO3_IO18	GPIO	3.3 V	I/O
I/O	3.3 V	GPIO	GPIO1_IO06	9	10	GPIO1_IO03	GPIO	3.3 V	I/O
O	1.8 V	QSPI	QSPI_A_SCLK	11	12	QSPI_B_SCLK	QSPI	1.8 V	O
I/O	1.8 V	QSPI	QSPI_A_DATA0	13	14	QSPI_B_DATA0	QSPI	1.8 V	I/O
I/O	1.8 V	QSPI	QSPI_A_DATA1	15	16	QSPI_B_DATA1	QSPI	1.8 V	I/O
I/O	1.8 V	QSPI	QSPI_A_DATA2	17	18	QSPI_B_DATA2	QSPI	1.8 V	I/O
I/O	1.8 V	QSPI	QSPI_A_DATA3	19	20	QSPI_B_DATA3	QSPI	1.8 V	I/O
I	1.8 V	QSPI	QSPI_A_DQS	21	22	QSPI_B_DQS	QSPI	1.8 V	I
P	0 V	GND	DGND	23	24	DGND	GND	0 V	P
O	1.8 V	QSPI	QSPI_A_SS0#	25	26	QSPI_B_SS0#	QSPI	1.8 V	O
O	1.8 V	QSPI	QSPI_A_SS1#	27	28	QSPI_B_SS1#	QSPI	1.8 V	O
P	0 V	GND	DGND	29	30	UART_SYSC_RXD_MUX	UART	3.3 V	I
I	1.8 / 3.3 V	UART	UART1_RXD_MUX	31	32	UART_SYSC_TXD_MUX	UART	3.3 V	O
O	1.8 / 3.3 V	UART	UART1_TXD_MUX	33	34	DGND	GND	0 V	P
O	1.8 / 3.3 V	UART	UART2_RXD_MUX	35	36	SD2_DATA0_MUX	SD [9]	1.8 / 3.3 V	I/O
I	1.8 / 3.3 V	UART	UART2_TXD_MUX	37	38	SD2_DATA1_MUX	SD [9]	1.8 / 3.3 V	I/O
I/O	3.3 V	GPIO	GPIO1_IO11	39	40	SD2_DATA2_MUX	SD [9]	1.8 / 3.3 V	I/O
O	1.8 / 3.3 V	SD [9]	SD2_CLK_MUX	41	42	SD2_DATA3_MUX	SD [9]	1.8 / 3.3 V	I/O
I/O	1.8 / 3.3 V	SD	SD2_WP	43	44	DGND	GND	0 V	P
O	1.8 / 3.3 V	UART	UART3_RXD_MUX	45	46	SD2_CMD_MUX	SD [9]	1.8 / 3.3 V	I/O
I	1.8 / 3.3 V	UART	UART3_TXD_MUX	47	48	DGND	GND	0 V	P
O	1.8 / 3.3 V	SD	SD2_RST#	49	50	SD2_CD#	SD	1.8 / 3.3 V	I/O
I	3.3 V	Control	TQMa8M_ONOFF	51	52	SDHC2_VSELECT	SD	3.3 V	O
I	3.3 V	Control	TQMa8M_SYS_RST#	53	54	DGND	GND	0 V	P
I/O	1.8 V	MD	MDIO	55	56	UART4_RXD	UART	1.8 / 3.3 V	I
O	1.8 V	MD	MDC	57	58	UART4_TXD	UART	1.8 / 3.3 V	O
P	0 V	GND	DGND	59	60	JTAG_MOD	JTAG	3.3 V	I

9: NC on MBa8Mx revision 03xx.

3.2.12 Headers (continued)

Table 40: Pinout Header 2, X35

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
P	3.3 V	Power	VCC3V3	1	2	VCC12V	Power	12 V	P
P	3.3 V	Power	VCC3V3	3	4	SAI2_RXFS	SAI	3.3 V	I
P	3.3 V	Power	VCC3V3	5	6	SAI2_RXC	SAI	3.3 V	I
P	5 V	Power	VCC5V	7	8	SAI2_RXD0	SAI	3.3 V	I
P	5 V	Power	VCC5V	9	10	SAI2_TXFS	SAI	3.3 V	O
P	5 V	Power	VCC5V	11	12	SAI2_TXC	SAI	3.3 V	O
-	-	(NC)	–	13	14	SAI2_TXD0	SAI	3.3 V	O
I	3.3 V	SAI	SAI5_RXC	15	16	SAI2_MCLK	SAI	3.3 V	O
I	3.3 V	SAI	SAI5_RXD0	17	18	DGND	GND	0 V	P
I	3.3 V	SAI	SAI5_RXD1	19	20	SPDIF_TX	SPDIF	3.3 V	O
I	3.3 V	SAI	SAI5_RXD2	21	22	SPDIF_RX	SPDIF	3.3 V	I
I	3.3 V	SAI	SAI5_RXD3	23	24	DGND	GND	0 V	P
I	3.3 V	SAI	SAI5_RXFS	25	26	SPDIF_EXT_CLK	SPDIF	3.3 V	O
O	3.3 V	SAI	SAI5_MCLK	27	28	DGND	GND	0 V	P
P	0 V	GND	DGND	29	30	I2C3_SCL	I2C	3.3 V	O
O	3.3 V	SPI	SPI2_SCLK	31	32	I2C3_SDA	I2C	3.3 V	I/O
O	3.3 V	SPI	SPI2_MOSI	33	34	DGND	GND	0 V	P
I	3.3 V	SPI	SPI2_MISO	35	36	I2C4_SCL	I2C	3.3 V	O
O	3.3 V	SPI	SPI2_SS0	37	38	I2C4_SDA	I2C	3.3 V	I/O
P	0 V	GND	DGND	39	40	DGND	GND	0 V	P

Table 41: Pinout Header 3, X34

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
P	3.3 V	Power	VCC3V3	1	2	VCC5V	Power	5 V	P
P	3.3 V	Power	VCC3V3	3	4	VCC5V	Power	5 V	P
P	3.3 V	Power	VCC3V3	5	6	VCC5V	Power	5 V	P
P	12 V	Power	VCC12V	7	8	DGND	GND	0 V	P
I	3.3 V	SAI	SAI1_RXC	9	10	SAI1_TXC	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD0	11	12	SAI1_TXD0	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD1	13	14	SAI1_TXD1	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD2	15	16	SAI1_TXD2	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD3	17	18	SAI1_TXD3	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD4	19	20	SAI1_TXD4	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD5	21	22	SAI1_TXD5	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD6	23	24	SAI1_TXD6	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXD7	25	26	SAI1_TXD7	SAI	3.3 V	O
I	3.3 V	SAI	SAI1_RXFS	27	28	SAI1_TXFS	SAI	3.3 V	O
P	0 V	GND	DGND	29	30	DGND	GND	0 V	P
O	3.3 V	SPI	SPI1_SCLK_MUX_A	31	32	SAI1_MCLK	SAI	3.3 V	O
O	3.3 V	SPI	SPI1_MOSI_MUX_A	33	34	DGND	GND	0 V	P
I	3.3 V	SPI	SPI1_MISO_MUX_A	35	36	DGND	GND	0 V	P
O	3.3 V	SPI	SPI1_SS0_MUX_A	37	38	DGND	GND	0 V	P
P	0 V	GND	DGND	39	40	DGND	GND	0 V	P

3.3 Diagnostic and user interfaces

3.3.1 Status LEDs

The MBa8Mx offers 12 diagnosis and status LEDs to signal the system status, which are controlled by GPIOs.
The following table shows the meaning of the LEDs.

Table 42: Status LEDs

Interface	Ref.	Colour	Signal
Debug UART/USB	V22	Green	VBUS Debug UART/USB 1 (lit, when VBUS is active)
	V23	Green	VBUS Debug UART/USB 2 (lit, when VBUS is active)
Ethernet	X9	Green	Link LED
		Yellow	Activity LED
Mini PCIe	V24	Green	Mini PCIe WWAN
	V25	Green	Mini PCIe WLAN
	V26	Green	Mini PCIe WPAN
Power	V67	Red	Status FAIL (lit, when TQMa8Mx is not powered up)
	V68	Blue	Status PGOOD (lit, when TQMa8Mx is powered up)
	V73	Blue	Status 24 V (lit, when supply 24 V is active)
User LEDs	V28	Green	User LED 1
	V27	Green	User LED 2
	V64	Orange	User LED 3

3.3.2 GP and Reset buttons

On the MBa8Mx, three general purpose push buttons are connected to GPIOs of the TQMa8Mx.
The push buttons switch to GND and have 10 kΩ pull-ups to 3.3 V.

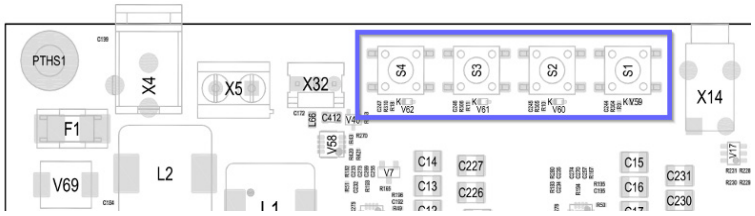


Figure 46: Position of GP buttons, S1, S2, S3 and Reset button, S4

Table 43: GP and Reset buttons, S1 to S4

Button	Signal	Remark
1	USER_BUTTON_1	GPIO1_IO05, X3-1
2	USER_BUTTON_2	GPIO3_IO17, X2-20
3	USER_BUTTON_3	GPIO1_IO07, X3-2
4	RESET	System Controller, D5-52 on MBa8Mx

3.3.3 Buzzer

A buzzer is provided on the MBa8Mx for an acoustic signalling of events. The buzzer is controlled by the CPU. The buzzer is placed on the bottom side of the MBa8Mx.

3.3.4 Fan

To cool the TQMa8Mx, a fan can be connected on the MBa8Mx.

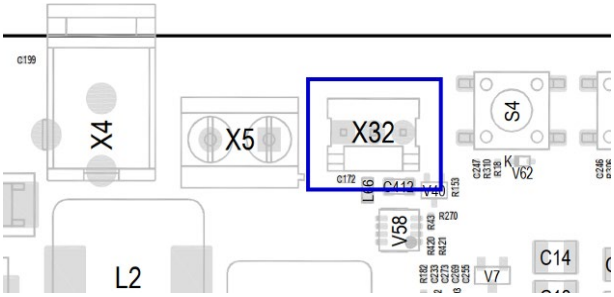


Figure 47: Position of fan connector, X32

Table 44: Pinout fan connector, X32

Pin	Signal	Remark
1	DGND	–
2	VCC_FAN	12 V via R420 on the MBa8Mx (default), optional 5 V via R421 on the MBa8Mx
3	(NC)	–

3.3.5 JTAG®

The JTAG® port of the i.MX 8M is routed to a standard ARM® 20-pin JTAG® connector (X30) on the MBa8Mx.
The pull-ups for the signals TDI, TMS, TRST# and SRST# are populated on the MBa8Mx. All signals have 3.3 V level.
The JTAG® interface is not ESD protected.

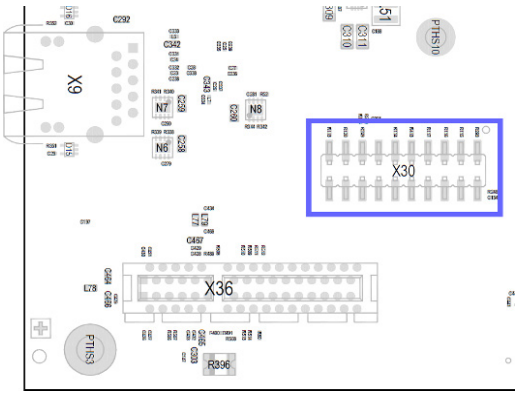


Figure 48: Position of JTAG® connector, X30

The following table shows the JTAG® connector pinout.

Table 45: Pinout JTAG® header, X30

Pin	Signal	Remark
1	JTAG_VREF	100 Ω in series to 3.3 V, use only as reference
2	3.3 V	0 Ω to 3.3 V, I_{max} = 10 mA
3	JTAG_TRST#	10 kΩ PU to 3.3 V
4	DGND	–
5	JTAG_TDI	10 kΩ PU to 3.3 V
6	DGND	–
7	JTAG_TMS	10 kΩ PU to 3.3 V
8	GND_DETECT	Connected to DGND
9	JTAG_TCK	Optional 10 kΩ PD, not assembled
10	DGND	–
11	(NC)	10 kΩ to DGND
12	DGND	–
13	JTAG_TDO	–
14	DGND	–
15	JTAG_SRST#	10 kΩ PU to 3.3 V
16	DGND	–
17	3.3 V	10 kΩ to 3.3 V
18	DGND	–
19	DGND	10 kΩ to DGND
20	DGND	–

4. MBA8MX VARIANTS

The MBa8Mx is available in two versions:

1. Variant MBa8Mx-AA for the TQMa8Mx
2. Variant MBa8Mx-AB for the TQMa8MxML and the TQMa8MxNL

5. SOFTWARE

No software is required for the MBa8Mx.
Suitable software is only required on the TQMa8Mx and is not a part of this User's Manual.
More information can be found in the Support-Wikis:

- TQ-Support Wiki for the TQMa8Mx
- TQ-Support Wiki for the TQMa8MxML
- TQ-Support Wiki for the TQMa8MxNL

6. MECHANICS

6.1 MBa8Mx dimensions

The MBa8Mx has overall dimensions (length × width) of 170 × 170 mm².
The MBa8Mx has a maximum height of approximately 26.4 mm.
The MBa8Mx has six 4.2 mm mounting holes for the housing, and four 3.2 mm mounting holes for a heat sink.
The MBa8Mx weighs approximately 200 grams without TQMa8Mx.

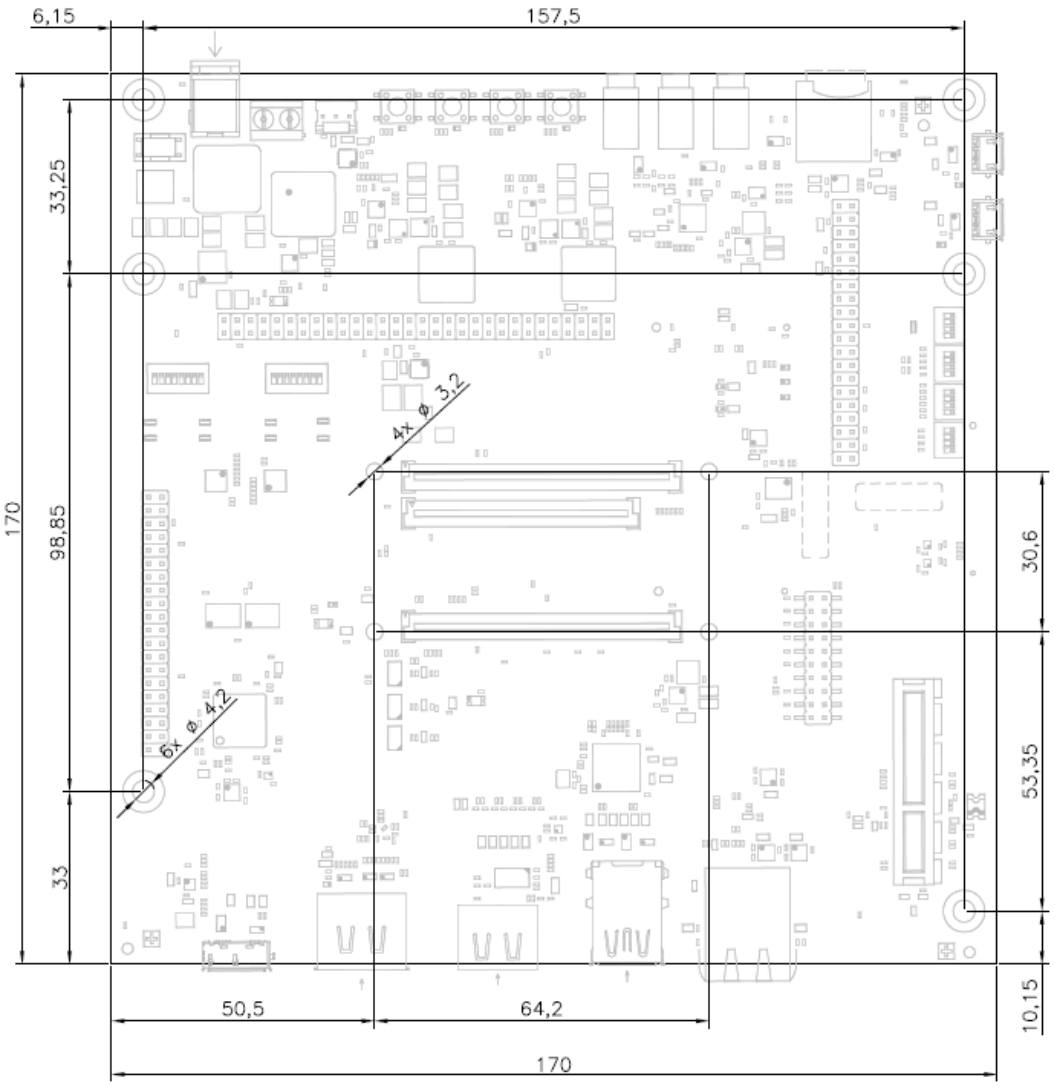


Figure 49: MBa8Mx dimensions

6.2 Notes of treatment

The TQMa8Mx is held in the mating connectors with a retention force of approximately 34 N.

To avoid damaging the TQMa8Mx connectors as well as the carrier board connectors while removing the TQMa8Mx the use of the extraction tool MOZIa8M is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8Mx for the extraction tool MOZIa8M.

6.3 Embedding in the overall system

The MBa8Mx serves as a design base for customer products, as well as a platform to support during development.

6.4 Housing

The form factor and the mounting holes of the MBa8Mx are designed for installation in a standard EURO housing.

6.5 Thermal management

MBa8Mx plus TQMa8Mx have a power consumption of approximately 5 to 8 watts.

Further power consumption occurs mainly at externally connected devices.

Attention: TQMa8Mx heat dissipation	
	The i.MX 8M CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8Mx must be taken into consideration when connecting the heat sink. The TQMa8Mx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Mx or the MBa8Mx and thus malfunction, deterioration or destruction.

6.6 Assembly

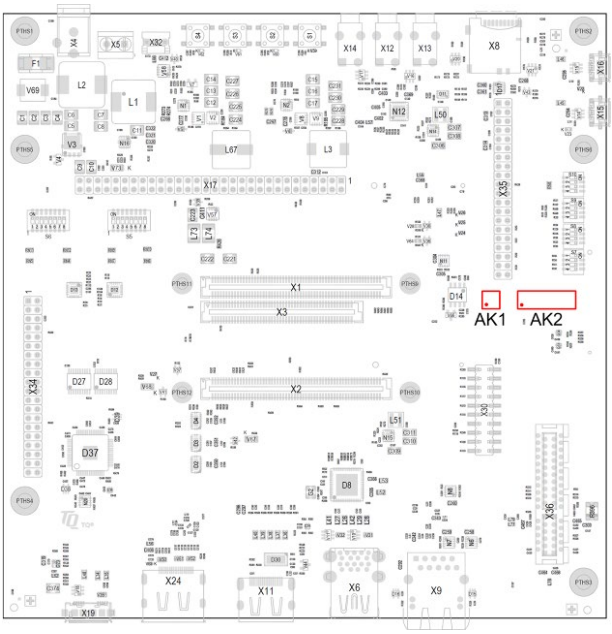


Figure 50: MBa8Mx component placement top, Rev. 02xx

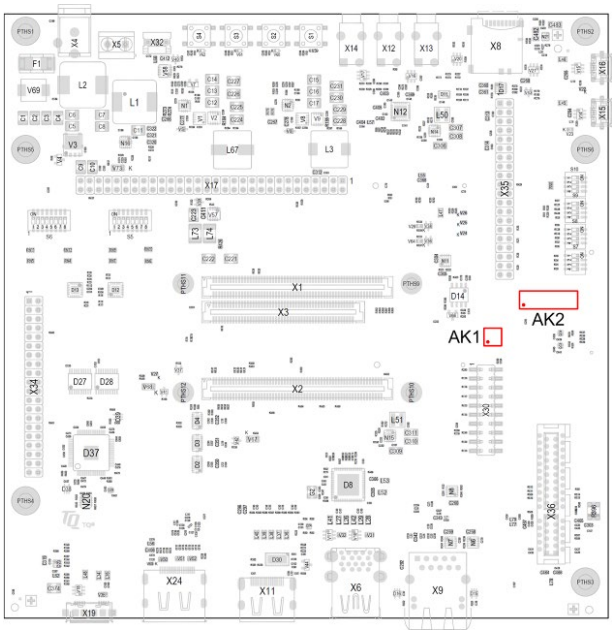


Figure 51: MBa8Mx component placement top, Rev. 03xx

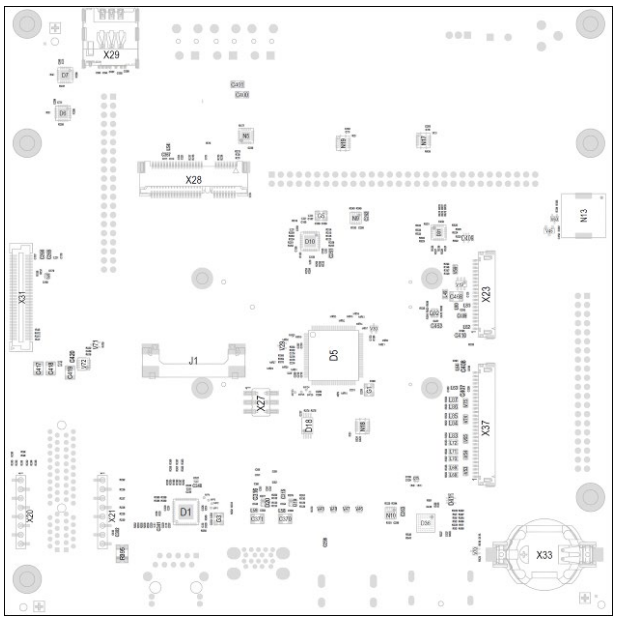


Figure 52: MBa8Mx component placement bot, Rev. 02xx

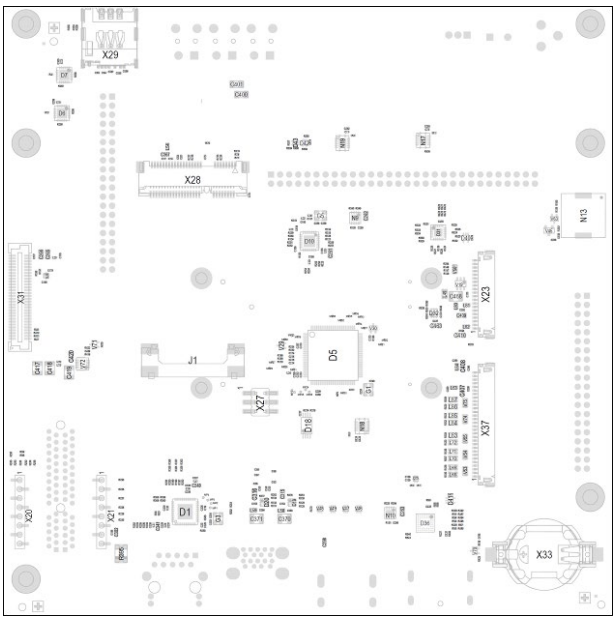


Figure 53: MBa8Mx component placement bot, Rev. 03xx

The labels on the MBa8Mx show the following information:

Table 46: Labels on MBa8Mx

Label	Content
AK1	Serial number
AK2	MBa8Mx version and revision, tests performed

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Since the MBa8Mx is a development platform, no EMC tests have been performed.
During the development of the MBa8Mx the standard DIN EN 55022:2010 limit class A was taken into account.

7.2 ESD

ESD protection is provided on most interfaces of the MBa8Mx.
The MBa8Mx schematics show, which interfaces provide ESD protection.

7.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 47: Climatic and operational conditions MBa8Mx

Parameter	Range	Remark
Ambient temperature	0 °C to +60 °C	With Lithium battery
Ambient temperature	0 °C to +70 °C	Without Lithium battery
Storage temperature	–10 °C to +60 °C	With Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa8Mx heat dissipation	
	The i.MX 8M CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8Mx must be taken into consideration when connecting the heat sink. The TQMa8Mx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Mx and thus malfunction, deterioration or destruction.

8.1 Protection against external effects

Protection class IP00 was defined for the MBa8Mx. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa8Mx.
The MBa8Mx is designed to be insensitive to vibration and impact.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBa8Mx is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa8Mx was designed to be recyclable and easy to repair.

9.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

9.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa8Mx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa8Mx enable compliance with EuP requirements for the MBa8Mx.

9.5 Packaging

The MBa8Mx is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for the MBa8Mx. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa8Mx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa8Mx is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 48: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BSP	Board Support Package
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR4	Double Data Rate 4
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DNC	Do Not Connect
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HD	High Density (graphics)
HDMI	High-Definition Multimedia Interface
I/O	Input/Output
I²C	Inter-Integrated Circuit
I²S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MAC	Media Access Controller
MCU	Memory Control Unit
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)

10.1 Acronyms and definitions (continued)

Table 48: Acronyms (continued)

Acronym	Meaning
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean operating Time Between Failures
n/a	Not Available
NAND	Not-And (flash memory)
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PTC	Positive Temperature Coefficient
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
R/W	Read/Write
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TDM	Time Division Multiplexing
UART	Universal Asynchronous Receiver/Transmitter
UN	United Nations
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

10.2 References

Table 49: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8M Dual / QuadLite /Quad of Applications Processors Data Sheet (Filename: IMX8MDQLQIEC_Ind_Rev0.1.pdf)	0.1, 05/2018	NXP
(2)	i.MX 8M Dual/ QuadLite /Quad of Applications Processors Data Sheet (Filename: IMX8MDQLQCEC_Cons_Rev0.1.pdf)	0.1, 05/2018	NXP
(3)	i.MX 8M Dual Applications Processor Reference Manual (Filename: IMX8MDQLQRM.pdf)	0, 01/2018	NXP
(4)	Mask Set Errata i.MX 8MD & i.MX 8MQ (Filename: IMX8MDQLQRM.pdf)	0.1, 01/2018	NXP
(5)	Single-Channel MIPI® DSI to Dual-Link LVDS Bridge (Filename: sn65dsi84-q1-1.pdf)	-, 08/2018	TI
(6)	Single-Chip USB to Dual UART Bridge (Filename: CP2105.pdf)	1.1, 11/2013	Silicon Labs
(7)	mikroBUS™ Standard specifications (Filename: mikrobus-standard-specification-v200.pdf)	2.0, 05/2015	MikroElektronika
(8)	TQMa8Mx User's Manual	– current –	TQ-Systems
(9)	TQMa8Mx Support Wiki	– current –	TQ-Systems
(10)	TQMa8MxML Support Wiki	– current –	TQ-Systems
(11)	TQMa8MxNL Support Wiki	– current –	TQ-Systems

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