MBa7x
User's Manual

MBa7x UM 0101
26.10.2020

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TABLE DIRECTORY

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FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	23.10.2019	Petz		First issue
0101	26.10.2020	Petz	All 4.1.1.3 4.1.1.3, 4.1.1.4 Figure 54 Table 71	Links updated “Connectors on MBa7x” split into “Pinout TQMa7S“, “Pinout TQMa7D“ Updated Added

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1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa7x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa7x circuit diagram
- TQMa7x User's Manual
- IMX7DRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa7x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa7x Rev. ≥0200. The MBa7x is designed as a carrier board for the TQMa7x. The figures in this User's Manual refer to the TQMa7x. All interfaces provided by the TQMa7x are available on the MBa7x. The function of the i.MX7 can be evaluated, and therefore the software development for a TQMa7x project can start immediately. The MBa7x supports all TQMa7x modules with i.MX7S (Solo) or i.MX7D (Dual) CPU.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 MBa7x Block diagram

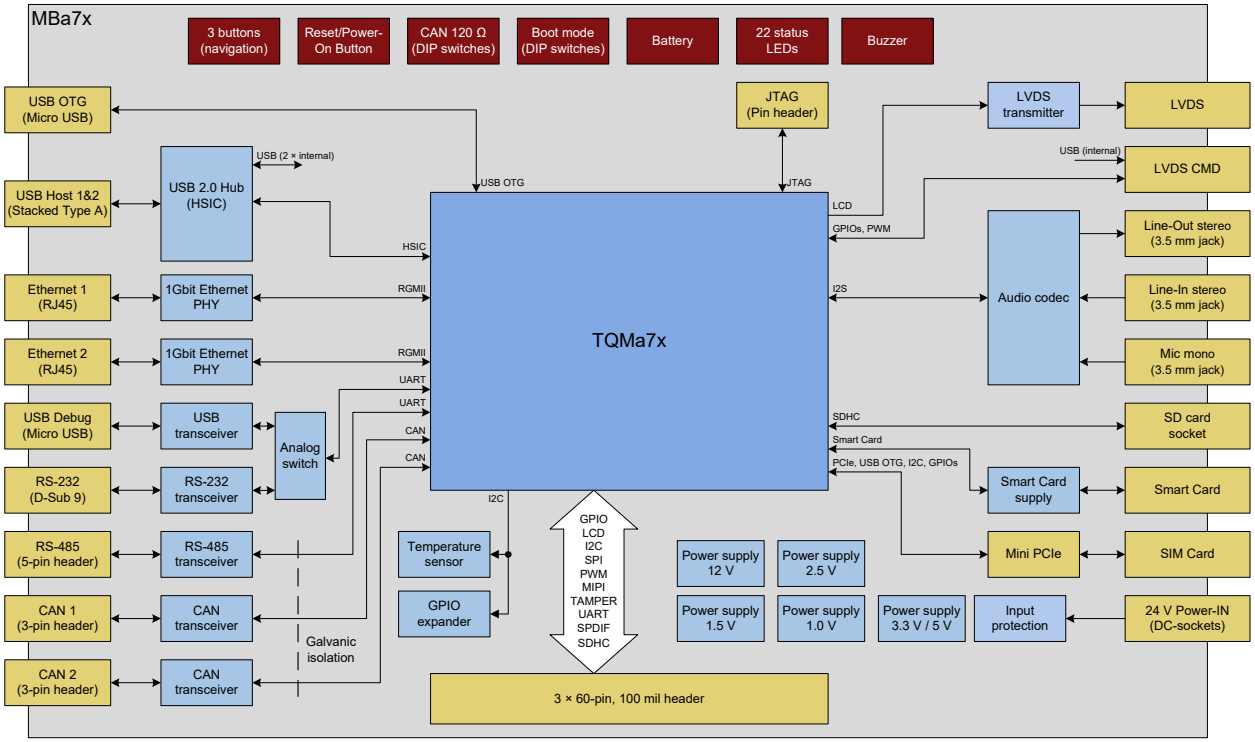

Figure 1: Block diagram MBa7x

3.1.2 Functionality

Core of the system is the TQMa7x with an NXP i.MX7. In addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, etc. all other available signals of the TQMa7x are routed to 100 mil standard headers.
The MBa7x provides the following interfaces and functions:

Table 2: Overview interfaces

Interface	Qty.	Connector type	Remark
USB 2.0 Hi-Speed host	2	USB receptacle, Type A	Stacked, right angle
USB 2.0 Hi-Speed host	1	100 mil header	–
USB 2.0 Hi-Speed host	1	DF19 receptacle	–
USB 2.0 Hi-Speed OTG	1	USB receptacle Micro AB	–
USB 2.0 Hi-Speed OTG	1	Mini PCIE slot	Only with TQMa7D
Ethernet 1000BASE-T	1	RJ45 receptacle	Receptacle with integrated magnetics
Ethernet 1000BASE-T	1	RJ45 receptacle	Receptacle with integrated magnetics, only with TQMa7D
CAN	2	Phoenix connector, 3-pin	Straight version, galvanically isolated
RS-485	1	Phoenix connector, 5-pin	Straight version, galvanically isolated
RS-232	1	D-Sub 9 connector	Right angle, Debug-UART
LVDS	1	DF19 receptacle	LVDS display signals
LVDS-CMD	1	DF19 receptacle	LVDS control signals
Audio	3	Jack 3.5 mm	1 × Line-Out (stereo) 1 × Line-In (stereo) 1 × Mic (mono)
SD card	1	Push-Pull-Type	–
Smart card	1	Smart card reader	Chip card size
PCIe	1	Mini PCIe	–
	1	SIM card holder	–
Headers	3	100 mil header	Power-Out (12 V, 5 V, 3.3 V) LCD interface (parallel) 2 × I^2C 3 × ECSPI 2 × ADC (4 channels each) 2 × CCM (In-/Output) 3 × UART 10 × TAMPER 1 × DSI 1 × CSI 1 × WDOG 1 × PWM 1 × USB OTG 1 × PCIe-REFCLK input 1 × QSPI 4 × GPIO
Power In	1	DC jack (2.5 mm / 5.5 mm)	V_{IN} = 24 V DC ±5 %
	1	2-pin screw terminal block	
Battery holder	1	CR2032 holder	Backup battery for RTC on TQMa7x

3.1.2 Functionality (continued)

Table 3: Overview diagnostic and user's interfaces

Interface	Qty.	Component	Remark
Status-LEDs	5	Green LED	4 × VBUS USB Host 1 × VBUS USB-OTG
	3	Green LED	Mini-PCIe WWAN, WLAN, WPAN
	2	Green LED	GPIO LEDs at port expander
	5	Green LED	Power LEDs (24 V, 12 V, 5 V, 3.3 V, PCIe-3.3 V)
	2	Green LED	Debug LEDs for USB debug interface
	1	Red LED	Reset LED
	4	Green / yellow LED	Ethernet-LEDs (Activity / Speed)
Temperature sensor	1	–	I^2C temperature sensor
Power / Reset buttons	3	Push button	i.MX7- / PMIC Reset, i.MX7-ONOFF
Navigation buttons	3	Push button	GPIO push button at port expander
Boot Mode configuration	16 + 2	DIP switch	2 × Boot Mode configuration 16 × Boot Device configuration
CAN and RS-485 termination	4	DIP switch	–
Signal generator	1	–	Buzzer at GPIO expander
JTAG	1	20-pin header, 100 mil pitch	–

4. ELECTRONICS

4.1 System components

4.1.1 TQMa7x

4.1.1.1 Overview TQMa7x

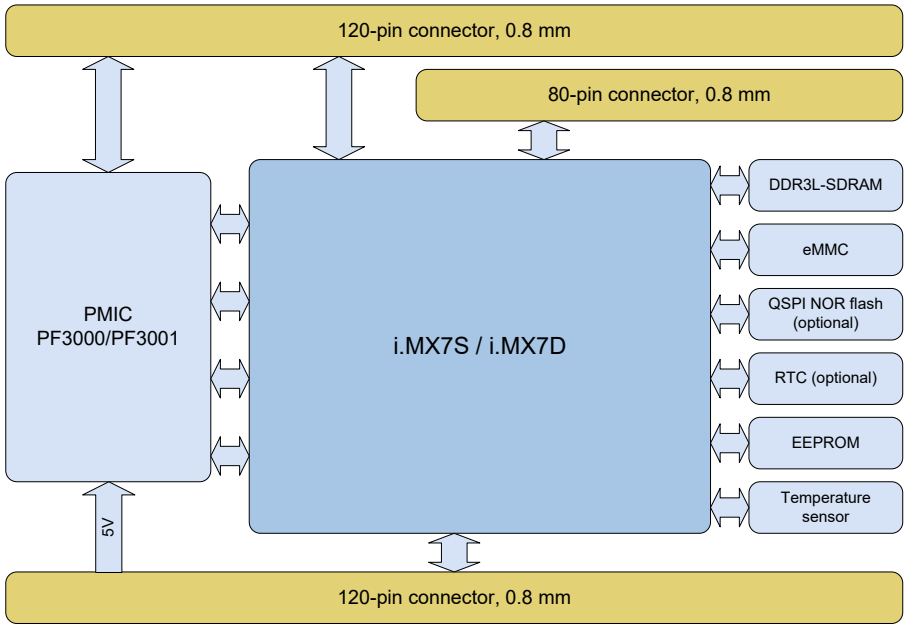

Figure 2: Block diagram TQMa7x

The TQMa7x with the i.MX7 is the central system component. It provides DDR3L SDRAM, eMMC, NOR flash and EEPROM memory.
All voltages required by the TQMa7x are derived from the supply voltage of 5 V.
More information is to be taken from the TQMa7x User's Manual.
The boot behaviour of the TQMa7x can be customised.
The required boot-mode configuration can be set with DIP switches on the MBa7x, see chapter 4.3.5.

4.1.1.2 Connectors X1, X2, X3

The available signals are routed to three connectors on the MBa7x.

Note:	TQMa7x interfaces
	Depending on the selected TQMa7x, not all interfaces are available. Available interfaces are to be taken from the TQMa7x User's Manual and the pinout tables in chapters 4.1.1.3, and 4.1.1.4.

The pin assignments listed in Table 4 to Table 9 refer to the BSP provided by TQ-Systems GmbH.
The signals at connectors X1 and X2 are identical, some signals at X3 have a different function at the TQMa7S and the TQMa7D.
The differences are indicated through different colour coding.

4.1.1.3 Pinout TQMa7S

Table 4: Pinout connector X1, TQMa7S

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	5 V	Power	VCC5V	1	2	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	3	4	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	5	6	VCC5V	Power	5 V	P	–
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	9	10	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	11	12	DGND	Power	0 V	P	–
–	P	3.3 V	Power	VCC3V3_REFOUT	13	14	VCC_SD	Power	1.8 / 3.3 V	P	–
–	P	3.3 V	Power	VCC3V3_VLDO3	15	16	VSNVS	Power	3.0 V	P	–
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	I	3.0 V	Config	LICELL	19	20	RESET_OUT#	Config	3.3 V	O	–
–	I	3.3 V	Config	PMIC_PWRON	21	22	RESET_IN#	Config	3.3 V	I	–
–	P	0 V	Power	DGND	23	24	IMX_ONOFF	Config	3.3 V	I	AC8
K1	I/O	3.3 V	I2C	I2C1_SDA	25	26	VCC3V3_MB_EN	Power	1.5 V	P	–
J2	O	3.3 V	I2C	I2C1_SCL	27	28	RFU (1)	–	–	–	–
–	P	0 V	Power	DGND	29	30	DGND	Power	0 V	P	–
K3	I/O	3.3 V	I2C	I2C2_SDA	31	32	ECSPI1_MOSI	SPI	3.3 V	O	G5
K2	O	3.3 V	I2C	I2C2_SCL	33	34	ECSPI1_MISO	SPI	3.3 V	I	H4
–	P	0 V	Power	DGND	35	36	ECSPI1_SS0#	SPI	3.3 V	O	H5
K6	I/O	3.3 V	I2C	I2C3_SDA	37	38	ECSPI1_SS1#	SPI	3.3 V	O	L3
K5	O	3.3 V	I2C	I2C3_SCL	39	40	ECSPI1_SS2#	SPI	3.3 V	O	L4
–	P	0 V	Power	DGND	41	42	ECSPI1_SS3#	SPI	3.3 V	O	L5
N2	O	3.3 V	PWM	LCD_CONTRAST	43	44	DGND	Power	0 V	P	–
N3	O	3.3 V	PWM	LCD_PWR_EN	45	46	ECSPI1_SCLK	SPI	3.3 V	O	H3
–	P	0 V	Power	DGND	47	48	DGND	Power	0 V	P	–
N5	O	3.3 V	PWM	PWM3_OUT	49	50	CCM_CLK1_P	CCM	1.8 V	I/O	Y2
N1	O	3.3 V	WDOG	WDOG1#	51	52	CCM_CLK1_N	CCM	1.8 V	I/O	Y1
–	P	0 V	Power	DGND	53	54	DGND	Power	0 V	P	–
W3	I	1.8 V	CCM	CCM_CLK2	55	56	UART3_CTS#	UART	3.3 V	O	M6
–	P	0 V	Power	DGND	57	58	UART3_RTS#	UART	3.3 V	I	M5
L1	I	3.3 V	UART	UART5_RX	59	60	UART3_RX	UART	3.3 V	I	M1
L2	O	3.3 V	UART	UART5_TX	61	62	UART3_TX	UART	3.3 V	O	M2
–	P	0 V	Power	DGND	63	64	DGND	Power	0 V	P	–
–	P	1.8 V	Power	VCC1V8_OUT	65	66	VCC1V8_IN	Power	1.8 V	P	–
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AC1	A	1.8 V	ADC	ADC2_IN0	69	70	ADC1_IN0	ADC	1.8 V	A	AD1
AC2	A	1.8 V	ADC	ADC2_IN1	71	72	ADC1_IN1	ADC	1.8 V	A	AD3
AB1	A	1.8 V	ADC	ADC2_IN2	73	74	ADC1_IN2	ADC	1.8 V	A	AE2
AB2	A	1.8 V	ADC	ADC2_IN3	75	76	ADC1_IN3	ADC	1.8 V	A	AE3
–	P	0 V	Power	DGND	77	78	DGND	Power	0 V	P	–
P4	I	3.3 V	BOOT	BOOT_MODE0	79	80	GPIO1_IO09	GPIO	3.3 V	I/O	R2
P5	I	3.3 V	BOOT	BOOT_MODE1	81	82	GPIO2_IO28	GPIO	3.3 V	I/O	K24
–	P	0 V	Power	DGND	83	84	GPIO2_IO29	GPIO	3.3 V	I/O	K23
U2	I	3.3 V	JTAG	JTAG_TRST#	85	86	GPIO2_IO30	GPIO	3.3 V	I/O	H24
U4	I	3.3 V	JTAG	JTAG_TMS	87	88	GPIO2_IO31	GPIO	3.3 V	I/O	K20
U3	I	3.3 V	JTAG	JTAG_TDI	89	90	GPIO4_IO03	GPIO	3.3 V	I/O	L6
U6	O	3.3 V	JTAG	JTAG_TDO	91	92	GPIO5_IO12	GPIO	3.3 V	I/O	E3
U1	I	3.3 V	JTAG	JTAG_MOD	93	94	GPIO7_IO12	GPIO	3.3 V	I/O	D16
U5	I	3.3 V	JTAG	JTAG_TCK	95	96	GPIO7_IO15	GPIO	3.3 V	I/O	D19
–	P	0 V	Power	DGND	97	98	DGND	Power	0 V	P	–
AA3	I	1.8 V	TAMPER	TAMPER8	99	100	TAMPER9	TAMPER	1.8 V	I	Y3
AA4	I	1.8 V	TAMPER	TAMPER6	101	102	TAMPER7	TAMPER	1.8 V	I	Y4
AA5	I	1.8 V	TAMPER	TAMPER4	103	104	TAMPER5	TAMPER	1.8 V	I	Y5
AB6	I	1.8 V	TAMPER	TAMPER2	105	106	TAMPER3	TAMPER	1.8 V	I	Y7
AA7	I	1.8 V	TAMPER	TAMPER0	107	108	TAMPER1	TAMPER	1.8 V	I	Y8
–	P	0 V	Power	DGND	109	110	DGND	Power	0 V	P	–
M23	I	3.3 V	UART	UART6_RX	111	112	UART7_RX	UART	3.3 V	I	L22
L25	O	3.3 V	UART	UART6_TX	113	114	UART7_TX	UART	3.3 V	O	L21
L23	O	3.3 V	UART	UART6_CTS#	115	116	UART7_CTS#	UART	3.3 V	O	K25
L24	I	3.3 V	UART	UART6_RTS#	117	118	UART7_RTS#	UART	3.3 V	I	L20
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

1: Reserved pin without function. Do not connect!

4.1.1.3 Pinout TQMa7S (continued)

Table 5: Pinout connector X2, TQMa7S

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
B4	O	1.8 / 3.3 V	USDHC	SD1_RESET#	3	4	PMIC_SD_VSEL	Config	3.3 V	O	R1
A5	I/O	1.8 / 3.3 V	USDHC	SD1_DATA0	5	6	SD1_CMD	USDHC	1.8 / 3.3 V	I/O	C5
A4	I/O	1.8 / 3.3 V	USDHC	SD1_DATA2	7	8	SD1_DATA1	USDHC	1.8 / 3.3 V	I/O	D6
B5	O	1.8 / 3.3 V	USDHC	SD1_CLK	9	10	SD1_DATA3	USDHC	1.8 / 3.3 V	I/O	D5
–	P	0 V	Power	DGND	11	12	SD1_WP	USDHC	1.8 / 3.3 V	I	C4
J5	O	3.3 V	SPI	ECSPI2_SCLK	13	14	SD1_CD#	USDHC	1.8 / 3.3 V	I	C6
H6	I	3.3 V	SPI	ECSPI2_MISO	15	16	DGND	Power	0 V	P	–
N6	I	3.3 V	USB_OTG	USB_OTG1_OC	17	18	ECSPI2_MOSI	SPI	3.3 V	O	G6
P1	I	3.3 V	USB_OTG	USB_OTG1_PWR	19	20	ECSPI2_SS0#	SPI	3.3 V	O	J6
C8	P	5 V	Power	USB_OTG1_VBUS	21	22	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	23	24	USB_OTG1_CHD#	USB_OTG	3.3 V	O	C7
A8	I/O	3.3 V	USB_OTG	USB_OTG1_DN	25	26	USB_OTG1_ID	USB_OTG	3.3 V	I	B7
B8	I/O	3.3 V	USB_OTG	USB_OTG1_DP	27	28	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	29	30	SAI1_TX_DATA	SAI	3.3 V	O	E11
B12	I/O	3.3 V	HSIC	USB_HOST_STROBE	31	32	SAI1_TX_BCLK	SAI	3.3 V	O	C11
–	P	0 V	Power	DGND	33	34	SAI1_TX_SYNC	SAI	3.3 V	O	D11
A12	I/O	3.3 V	HSIC	USB_HOST_DATA	35	36	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	37	38	SAI1_RX_DATA	SAI	3.3 V	I	E12
E10	O	3.3 V	SAI	SAI1_MCLK	39	40	SAI1_RX_BCLK	SAI	3.3 V	I	D12
–	P	0 V	Power	DGND	41	42	SAI1_RX_SYNC	SAI	3.3 V	I	C12
D15	O	3.3 V	WDOG	WDOG2#	43	44	DGND	Power	0 V	P	–
E19	I	3.3 V	WDOG	WDOG2_RESET#	45	46	ENET1_MDC	ENET	3.3 V	O	T1
–	P	0 V	Power	DGND	47	48	ENET1_MDIO	ENET	3.3 V	I/O	R5
F16	O	3.3 V	RGMII	RGMII1_TXC	49	50	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	51	52	RGMII1_RXC	RGMII	3.3 V	I	F15
F17	O	3.3 V	RGMII	RGMII1_TD0	53	54	DGND	Power	0 V	P	–
E17	O	3.3 V	RGMII	RGMII1_TD1	55	56	RGMII1_RD0	RGMII	3.3 V	I	E14
E18	O	3.3 V	RGMII	RGMII1_TD2	57	58	RGMII1_RD1	RGMII	3.3 V	I	F14
D18	O	3.3 V	RGMII	RGMII1_TD3	59	60	RGMII1_RD2	RGMII	3.3 V	I	D13
E16	O	3.3 V	RGMII	RGMII1_TX_CTL	61	62	RGMII1_RD3	RGMII	3.3 V	I	E13
–	P	0 V	Power	DGND	63	64	RGMII1_RX_CTL	RGMII	3.3 V	I	E15
F6	I/O	3.3 V	SIM	SIM_TRXD	65	66	DGND	Power	0 V	P	–
E5	O	3.3 V	SIM	SIM_RST#	67	68	LCD_ENABLE	LCD	3.3 V	O	F25
F5	O	3.3 V	SIM	SIM_SVEN	69	70	DGND	Power	0 V	P	–
E6	O	3.3 V	SIM	SIM_PD	71	72	LCD_CLK	LCD	3.3 V	O	E20
E4	O	3.3 V	SIM	SIM_CLK	73	74	DGND	Power	0 V	P	–
C21	O	3.3 V	LCD	LCD_RESET#	75	76	LCD_HSYNC	LCD	3.3 V	O	E25
–	P	0 V	Power	DGND	77	78	LCD_VSYNC	LCD	3.3 V	O	F24
D21	O	3.3 V	LCD	LCD_DATA00	79	80	DGND	Power	0 V	P	–
B22	O	3.3 V	LCD	LCD_DATA02	81	82	LCD_DATA01	LCD	3.3 V	O	A22
C22	O	3.3 V	LCD	LCD_DATA04	83	84	LCD_DATA03	LCD	3.3 V	O	A23
A24	O	3.3 V	LCD	LCD_DATA06	85	86	LCD_DATA05	LCD	3.3 V	O	B23
–	P	0 V	Power	DGND	87	88	LCD_DATA07	LCD	3.3 V	O	F20
E21	O	3.3 V	LCD	LCD_DATA08	89	90	DGND	Power	0 V	P	–
B24	O	3.3 V	LCD	LCD_DATA10	91	92	LCD_DATA09	LCD	3.3 V	O	C23
F21	O	3.3 V	LCD	LCD_DATA12	93	94	LCD_DATA11	LCD	3.3 V	O	G20
D23	O	3.3 V	LCD	LCD_DATA14	95	96	LCD_DATA13	LCD	3.3 V	O	E22
–	P	0 V	Power	DGND	97	98	LCD_DATA15	LCD	3.3 V	O	C24
B25	O	3.3 V	LCD	LCD_DATA16	99	100	DGND	Power	0 V	P	–
E23	O	3.3 V	LCD	LCD_DATA18	101	102	LCD_DATA17	LCD	3.3 V	O	G21
C25	O	3.3 V	LCD	LCD_DATA20	103	104	LCD_DATA19	LCD	3.3 V	O	D24
D25	O	3.3 V	LCD	LCD_DATA22	105	106	LCD_DATA21	LCD	3.3 V	O	E24
–	P	0 V	Power	DGND	107	108	LCD_DATA23	LCD	3.3 V	O	G23
M20	O	3.3 V	QSPI	QSPI_SCLK	109	110	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	111	112	QSPI_DATA0	QSPI	3.3 V	I/O	P20
M21	O	3.3 V	QSPI	QSPI_SS0#	113	114	QSPI_DATA1	QSPI	3.3 V	I/O	P21
M22	O	3.3 V	QSPI	QSPI_SS1#	115	116	QSPI_DATA2	QSPI	3.3 V	I/O	N20
N22	O	3.3 V	QSPI	QSPI_RESET#	117	118	QSPI_DATA3	QSPI	3.3 V	I/O	N21
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

4.1.1.3 Pinout TQMa7S (continued)

Table 6: Pinout connector X3, TQMa7S

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
T5	I	3.3 V	CAN	CAN2_RX	3	4	CAN1_RX	CAN	3.3 V	I	T2
T6	O	3.3 V	CAN	CAN2_TX	5	6	CAN1_TX	CAN	3.3 V	O	T3
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
P3	I/O	3.3 V	GPIO	GPIO1_IO07	9	10	UART4_CTS#	UART	3.3 V	O	E9
P2	I/O	3.3 V	GPIO	GPIO1_IO06	11	12	UART4_RTS#	UART	3.3 V	I	E8
B11	–	–	NC	NC	13	14	UART4_RX	UART	3.3 V	I	D9
C10	–	–	NC	NC	15	16	UART4_TX	UART	3.3 V	O	D8
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	–	–	–	RFU (2)	19	20	NC	NC	–	–	A10
–	–	–	–	RFU (2)	21	22	NC	NC	–	–	B10
–	–	–	–	RFU (2)	23	24	DGND	Power	0 V	P	–
–	–	–	–	RFU (2)	25	26	CSI_D1_N	MIPI	1.8 V	I	A14
–	P	0 V	Power	DGND	27	28	CSI_D1_P	MIPI	1.8 V	I	B14
A18	O	1.8 V	MIPI	DSI_D1_N	29	30	DGND	Power	0 V	P	–
B18	O	1.8 V	MIPI	DSI_D1_P	31	32	CSI_CLK_N	MIPI	1.8 V	I	A15
–	P	0 V	Power	DGND	33	34	CSI_CLK_P	MIPI	1.8 V	I	B15
A19	O	1.8 V	MIPI	DSI_CLK_N	35	36	DGND	Power	0 V	P	–
B19	O	1.8 V	MIPI	DSI_CLK_P	37	38	CSI_D0_N	MIPI	1.8 V	I	A16
–	P	0 V	Power	DGND	39	40	CSI_D0_P	MIPI	1.8 V	I	B16
A20	O	1.8 V	MIPI	DSI_D0_N	41	42	DGND	Power	0 V	P	–
B20	O	1.8 V	MIPI	DSI_D0_P	43	44	TQMa7x 01xx: RFU (2)	–	–	–	–
							TQMa7x 02xx: TEMP_EVENT# (3)	–	3.3 V	O	–
–	P	0 V	Power	DGND	45	46	RFU (2)	–	–	–	–
D3	I/O	3.3 V	GPIO	GPIO5_IO09	47	48	RFU (2)	–	–	–	–
C3	I/O	3.3 V	GPIO	GPIO5_IO10	49	50	RFU (2)	–	–	–	–
–	P	0 V	Power	DGND	51	52	DGND	Power	0 V	P	–
H25	I/O	3.3 V	GPIO	GPIO2_IO27	53	54	GPIO2_IO21	GPIO	3.3 V	I/O	G24
–	P	0 V	Power	DGND	55	56	DGND	Power	0 V	P	–
H23	I/O	3.3 V	GPIO	GPIO2_IO22	57	58	GPIO2_IO16	GPIO	3.3 V	I/O	J21
H22	I/O	3.3 V	GPIO	GPIO2_IO23	59	60	GPIO2_IO17	GPIO	3.3 V	I/O	J20
J25	I/O	3.3 V	GPIO	GPIO2_IO24	61	62	GPIO2_IO18	GPIO	3.3 V	I/O	H21
J24	I/O	3.3 V	GPIO	GPIO2_IO25	63	64	GPIO2_IO19	GPIO	3.3 V	I/O	H20
K21	I/O	3.3 V	GPIO	GPIO2_IO26	65	66	GPIO2_IO20	GPIO	3.3 V	I/O	G25
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AE11	–	–	NC	NC	69	70	NC	NC	–	–	AC11
AD11	–	–	NC	NC	71	72	NC	NC	–	–	AB11
–	P	0 V	Power	DGND	73	74	DGND	Power	0 V	P	–
AE10	–	–	NC	NC	75	76	NC	NC	–	–	AC10
AD10	–	–	NC	NC	77	78	NC	NC	–	–	AB10
–	P	0 V	Power	DGND	79	80	DGND	Power	0 V	P	–

2: Reserved pin without function. Do not connect!
3: Pull-Up on carrier board required.

4.1.1.4 Pinout TQMa7D

Table 7: Pinout connector X1, TQMa7D

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	5 V	Power	VCC5V	1	2	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	3	4	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	5	6	VCC5V	Power	5 V	P	–
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	9	10	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	11	12	DGND	Power	0 V	P	–
–	P	3.3 V	Power	VCC3V3_REFOUT	13	14	VCC_SD	Power	1.8 / 3.3 V	P	–
–	P	3.3 V	Power	VCC3V3_VLDO3	15	16	VSNVS	Power	3.0 V	P	–
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	I	3.0 V	Config	LICELL	19	20	RESET_OUT#	Config	3.3 V	O	–
–	I	3.3 V	Config	PMIC_PWRON	21	22	RESET_IN#	Config	3.3 V	I	–
–	P	0 V	Power	DGND	23	24	IMX_ONOFF	Config	3.3 V	I	AC8
K1	I/O	3.3 V	I2C	I2C1_SDA	25	26	VCC3V3_MB_EN	Power	1.5 V	P	–
J2	O	3.3 V	I2C	I2C1_SCL	27	28	RFU (4)	–	–	–	–
–	P	0 V	Power	DGND	29	30	DGND	Power	0 V	P	–
K3	I/O	3.3 V	I2C	I2C2_SDA	31	32	ECSPI1_MOSI	SPI	3.3 V	O	G5
K2	O	3.3 V	I2C	I2C2_SCL	33	34	ECSPI1_MISO	SPI	3.3 V	I	H4
–	P	0 V	Power	DGND	35	36	ECSPI1_SS0#	SPI	3.3 V	O	H5
K6	I/O	3.3 V	I2C	I2C3_SDA	37	38	ECSPI1_SS1#	SPI	3.3 V	O	L3
K5	O	3.3 V	I2C	I2C3_SCL	39	40	ECSPI1_SS2#	SPI	3.3 V	O	L4
–	P	0 V	Power	DGND	41	42	ECSPI1_SS3#	SPI	3.3 V	O	L5
N2	O	3.3 V	PWM	LCD_CONTRAST	43	44	DGND	Power	0 V	P	–
N3	O	3.3 V	PWM	LCD_PWR_EN	45	46	ECSPI1_SCLK	SPI	3.3 V	O	H3
–	P	0 V	Power	DGND	47	48	DGND	Power	0 V	P	–
N5	O	3.3 V	PWM	PWM3_OUT	49	50	CCM_CLK1_P	CCM	1.8 V	I/O	Y2
N1	O	3.3 V	WDOG	WDOG1#	51	52	CCM_CLK1_N	CCM	1.8 V	I/O	Y1
–	P	0 V	Power	DGND	53	54	DGND	Power	0 V	P	–
W3	I	1.8 V	CCM	CCM_CLK2	55	56	UART3_CTS#	UART	3.3 V	O	M6
–	P	0 V	Power	DGND	57	58	UART3_RTS#	UART	3.3 V	I	M5
L1	I	3.3 V	UART	UART5_RX	59	60	UART3_RX	UART	3.3 V	I	M1
L2	O	3.3 V	UART	UART5_TX	61	62	UART3_TX	UART	3.3 V	O	M2
–	P	0 V	Power	DGND	63	64	DGND	Power	0 V	P	–
–	P	1.8 V	Power	VCC1V8_OUT	65	66	VCC1V8_IN	Power	1.8 V	P	–
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AC1	A	1.8 V	ADC	ADC2_IN0	69	70	ADC1_IN0	ADC	1.8 V	A	AD1
AC2	A	1.8 V	ADC	ADC2_IN1	71	72	ADC1_IN1	ADC	1.8 V	A	AD3
AB1	A	1.8 V	ADC	ADC2_IN2	73	74	ADC1_IN2	ADC	1.8 V	A	AE2
AB2	A	1.8 V	ADC	ADC2_IN3	75	76	ADC1_IN3	ADC	1.8 V	A	AE3
–	P	0 V	Power	DGND	77	78	DGND	Power	0 V	P	–
P4	I	3.3 V	BOOT	BOOT_MODE0	79	80	GPIO1_IO09	GPIO	3.3 V	I/O	R2
P5	I	3.3 V	BOOT	BOOT_MODE1	81	82	GPIO2_IO28	GPIO	3.3 V	I/O	K24
–	P	0 V	Power	DGND	83	84	GPIO2_IO29	GPIO	3.3 V	I/O	K23
U2	I	3.3 V	JTAG	JTAG_TRST#	85	86	GPIO2_IO30	GPIO	3.3 V	I/O	H24
U4	I	3.3 V	JTAG	JTAG_TMS	87	88	GPIO2_IO31	GPIO	3.3 V	I/O	K20
U3	I	3.3 V	JTAG	JTAG_TDI	89	90	GPIO4_IO03	GPIO	3.3 V	I/O	L6
U6	O	3.3 V	JTAG	JTAG_TDO	91	92	GPIO5_IO12	GPIO	3.3 V	I/O	E3
U1	I	3.3 V	JTAG	JTAG_MOD	93	94	GPIO7_IO12	GPIO	3.3 V	I/O	D16
U5	I	3.3 V	JTAG	JTAG_TCK	95	96	GPIO7_IO15	GPIO	3.3 V	I/O	D19
–	P	0 V	Power	DGND	97	98	DGND	Power	0 V	P	–
AA3	I	1.8 V	TAMPER	TAMPER8	99	100	TAMPER9	TAMPER	1.8 V	I	Y3
AA4	I	1.8 V	TAMPER	TAMPER6	101	102	TAMPER7	TAMPER	1.8 V	I	Y4
AA5	I	1.8 V	TAMPER	TAMPER4	103	104	TAMPER5	TAMPER	1.8 V	I	Y5
AB6	I	1.8 V	TAMPER	TAMPER2	105	106	TAMPER3	TAMPER	1.8 V	I	Y7
AA7	I	1.8 V	TAMPER	TAMPER0	107	108	TAMPER1	TAMPER	1.8 V	I	Y8
–	P	0 V	Power	DGND	109	110	DGND	Power	0 V	P	–
M23	I	3.3 V	UART	UART6_RX	111	112	UART7_RX	UART	3.3 V	I	L22
L25	O	3.3 V	UART	UART6_TX	113	114	UART7_TX	UART	3.3 V	O	L21
L23	O	3.3 V	UART	UART6_CTS#	115	116	UART7_CTS#	UART	3.3 V	O	K25
L24	I	3.3 V	UART	UART6_RTS#	117	118	UART7_RTS#	UART	3.3 V	I	L20
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

4: Reserved pin without function. Do not connect!

4.1.1.4 Pinout TQMa7D (continued)

Table 8: Pinout connector X2, TQMa7D

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
B4	O	1.8 / 3.3 V	USDHC	SD1_RESET#	3	4	PMIC_SD_VSEL	Config	3.3 V	O	R1
A5	I/O	1.8 / 3.3 V	USDHC	SD1_DATA0	5	6	SD1_CMD	USDHC	1.8 / 3.3 V	I/O	C5
A4	I/O	1.8 / 3.3 V	USDHC	SD1_DATA2	7	8	SD1_DATA1	USDHC	1.8 / 3.3 V	I/O	D6
B5	O	1.8 / 3.3 V	USDHC	SD1_CLK	9	10	SD1_DATA3	USDHC	1.8 / 3.3 V	I/O	D5
–	P	0 V	Power	DGND	11	12	SD1_WP	USDHC	1.8 / 3.3 V	I	C4
J5	O	3.3 V	SPI	ECSPI2_SCLK	13	14	SD1_CD#	USDHC	1.8 / 3.3 V	I	C6
H6	I	3.3 V	SPI	ECSPI2_MISO	15	16	DGND	Power	0 V	P	–
N6	I	3.3 V	USB_OTG	USB_OTG1_OC	17	18	ECSPI2_MOSI	SPI	3.3 V	O	G6
P1	I	3.3 V	USB_OTG	USB_OTG1_PWR	19	20	ECSPI2_SS0#	SPI	3.3 V	O	J6
C8	P	5 V	Power	USB_OTG1_VBUS	21	22	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	23	24	USB_OTG1_CHD#	USB_OTG	3.3 V	O	C7
A8	I/O	3.3 V	USB_OTG	USB_OTG1_DN	25	26	USB_OTG1_ID	USB_OTG	3.3 V	I	B7
B8	I/O	3.3 V	USB_OTG	USB_OTG1_DP	27	28	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	29	30	SAI1_TX_DATA	SAI	3.3 V	O	E11
B12	I/O	3.3 V	HSIC	USB_HOST_STROBE	31	32	SAI1_TX_BCLK	SAI	3.3 V	O	C11
–	P	0 V	Power	DGND	33	34	SAI1_TX_SYNC	SAI	3.3 V	O	D11
A12	I/O	3.3 V	HSIC	USB_HOST_DATA	35	36	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	37	38	SAI1_RX_DATA	SAI	3.3 V	I	E12
E10	O	3.3 V	SAI	SAI1_MCLK	39	40	SAI1_RX_BCLK	SAI	3.3 V	I	D12
–	P	0 V	Power	DGND	41	42	SAI1_RX_SYNC	SAI	3.3 V	I	C12
D15	O	3.3 V	WDOG	WDOG2#	43	44	DGND	Power	0 V	P	–
E19	I	3.3 V	WDOG	WDOG2_RESET#	45	46	ENET1_MDC	ENET	3.3 V	O	T1
–	P	0 V	Power	DGND	47	48	ENET1_MDIO	ENET	3.3 V	I/O	R5
F16	O	3.3 V	RGMII	RGMII1_TXC	49	50	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	51	52	RGMII1_RXC	RGMII	3.3 V	I	F15
F17	O	3.3 V	RGMII	RGMII1_TD0	53	54	DGND	Power	0 V	P	–
E17	O	3.3 V	RGMII	RGMII1_TD1	55	56	RGMII1_RD0	RGMII	3.3 V	I	E14
E18	O	3.3 V	RGMII	RGMII1_TD2	57	58	RGMII1_RD1	RGMII	3.3 V	I	F14
D18	O	3.3 V	RGMII	RGMII1_TD3	59	60	RGMII1_RD2	RGMII	3.3 V	I	D13
E16	O	3.3 V	RGMII	RGMII1_TX_CTL	61	62	RGMII1_RD3	RGMII	3.3 V	I	E13
–	P	0 V	Power	DGND	63	64	RGMII1_RX_CTL	RGMII	3.3 V	I	E15
F6	I/O	3.3 V	SIM	SIM_TRXD	65	66	DGND	Power	0 V	P	–
E5	O	3.3 V	SIM	SIM_RST#	67	68	LCD_ENABLE	LCD	3.3 V	O	F25
F5	O	3.3 V	SIM	SIM_SVEN	69	70	DGND	Power	0 V	P	–
E6	O	3.3 V	SIM	SIM_PD	71	72	LCD_CLK	LCD	3.3 V	O	E20
E4	O	3.3 V	SIM	SIM_CLK	73	74	DGND	Power	0 V	P	–
C21	O	3.3 V	LCD	LCD_RESET#	75	76	LCD_HSYNC	LCD	3.3 V	O	E25
–	P	0 V	Power	DGND	77	78	LCD_VSYNC	LCD	3.3 V	O	F24
D21	O	3.3 V	LCD	LCD_DATA00	79	80	DGND	Power	0 V	P	–
B22	O	3.3 V	LCD	LCD_DATA02	81	82	LCD_DATA01	LCD	3.3 V	O	A22
C22	O	3.3 V	LCD	LCD_DATA04	83	84	LCD_DATA03	LCD	3.3 V	O	A23
A24	O	3.3 V	LCD	LCD_DATA06	85	86	LCD_DATA05	LCD	3.3 V	O	B23
–	P	0 V	Power	DGND	87	88	LCD_DATA07	LCD	3.3 V	O	F20
E21	O	3.3 V	LCD	LCD_DATA08	89	90	DGND	Power	0 V	P	–
B24	O	3.3 V	LCD	LCD_DATA10	91	92	LCD_DATA09	LCD	3.3 V	O	C23
F21	O	3.3 V	LCD	LCD_DATA12	93	94	LCD_DATA11	LCD	3.3 V	O	G20
D23	O	3.3 V	LCD	LCD_DATA14	95	96	LCD_DATA13	LCD	3.3 V	O	E22
–	P	0 V	Power	DGND	97	98	LCD_DATA15	LCD	3.3 V	O	C24
B25	O	3.3 V	LCD	LCD_DATA16	99	100	DGND	Power	0 V	P	–
E23	O	3.3 V	LCD	LCD_DATA18	101	102	LCD_DATA17	LCD	3.3 V	O	G21
C25	O	3.3 V	LCD	LCD_DATA20	103	104	LCD_DATA19	LCD	3.3 V	O	D24
D25	O	3.3 V	LCD	LCD_DATA22	105	106	LCD_DATA21	LCD	3.3 V	O	E24
–	P	0 V	Power	DGND	107	108	LCD_DATA23	LCD	3.3 V	O	G23
M20	O	3.3 V	QSPI	QSPI_SCLK	109	110	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	111	112	QSPI_DATA0	QSPI	3.3 V	I/O	P20
M21	O	3.3 V	QSPI	QSPI_SS0#	113	114	QSPI_DATA1	QSPI	3.3 V	I/O	P21
M22	O	3.3 V	QSPI	QSPI_SS1#	115	116	QSPI_DATA2	QSPI	3.3 V	I/O	N20
N22	O	3.3 V	QSPI	QSPI_RESET#	117	118	QSPI_DATA3	QSPI	3.3 V	I/O	N21
–	P	0 V	Power	DGND	119	120	DGND	Power	0 V	P	–

4.1.1.4 Pinout TQMa7D (continued)

Table 9: Pinout connector X3, TQMa7D

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	Power	DGND	1	2	DGND	Power	0 V	P	–
T5	I	3.3 V	CAN	CAN2_RX	3	4	CAN1_RX	CAN	3.3 V	I	T2
T6	O	3.3 V	CAN	CAN2_TX	5	6	CAN1_TX	CAN	3.3 V	O	T3
–	P	0 V	Power	DGND	7	8	DGND	Power	0 V	P	–
P3	I	3.3 V	USB_OTG	USB_OTG2_PWR	9	10	UART4_CTS#	UART	3.3 V	O	E9
P2	I	3.3 V	USB_OTG	USB_OTG2_OC	11	12	UART4_RTS#	UART	3.3 V	I	E8
B11	I	3.3 V	USB_OTG	USB_OTG2_ID	13	14	UART4_RX	UART	3.3 V	I	D9
C10	P	3.3 V	Power	USB_OTG2_VBUS	15	16	UART4_TX	UART	3.3 V	O	D8
–	P	0 V	Power	DGND	17	18	DGND	Power	0 V	P	–
–	–	–	–	RFU (5)	19	20	USB_OTG2_DN	USB_OTG	3.3 V	I/O	A10
–	–	–	–	RFU (5)	21	22	USB_OTG2_DP	USB_OTG	3.3 V	I/O	B10
–	–	–	–	RFU (5)	23	24	DGND	Power	0 V	P	–
–	–	–	–	RFU (5)	25	26	CSI_D1_N	MIPI	1.8 V	I	A14
–	P	0 V	Power	DGND	27	28	CSI_D1_P	MIPI	1.8 V	I	B14
A18	O	1.8 V	MIPI	DSI_D1_N	29	30	DGND	Power	0 V	P	–
B18	O	1.8 V	MIPI	DSI_D1_P	31	32	CSI_CLK_N	MIPI	1.8 V	I	A15
–	P	0 V	Power	DGND	33	34	CSI_CLK_P	MIPI	1.8 V	I	B15
A19	O	1.8 V	MIPI	DSI_CLK_N	35	36	DGND	Power	0 V	P	–
B19	O	1.8 V	MIPI	DSI_CLK_P	37	38	CSI_D0_N	MIPI	1.8 V	I	A16
–	P	0 V	Power	DGND	39	40	CSI_D0_P	MIPI	1.8 V	I	B16
A20	O	1.8 V	MIPI	DSI_D0_N	41	42	DGND	Power	0 V	P	–
B20	O	1.8 V	MIPI	DSI_D0_P	43	44	TQMa7x 01xx: RFU (5)	–	–	–	–
							TQMa7x 02xx: TEMP_EVENT# (6)	–	3.3 V	O	–
–	P	0 V	Power	DGND	45	46	RFU (5)	–	–	–	–
D3	I/O	3.3 V	ENET	ENET2_MDIO	47	48	RFU (5)	–	–	–	–
C3	O	3.3 V	ENET	ENET2_MDC	49	50	RFU (5)	–	–	–	–
–	P	0 V	Power	DGND	51	52	DGND	Power	0 V	P	–
H25	O	3.3 V	RGMII	RGMII2_TXC	53	54	RGMII2_RXC	RGMII	3.3 V	I	G24
–	P	0 V	Power	DGND	55	56	DGND	Power	0 V	P	–
H23	O	3.3 V	RGMII	RGMII2_TD0	57	58	RGMII2_RD0	RGMII	3.3 V	I	J21
H22	O	3.3 V	RGMII	RGMII2_TD1	59	60	RGMII2_RD1	RGMII	3.3 V	I	J20
J25	O	3.3 V	RGMII	RGMII2_TD2	61	62	RGMII2_RD2	RGMII	3.3 V	I	H21
J24	O	3.3 V	RGMII	RGMII2_TD3	63	64	RGMII2_RD3	RGMII	3.3 V	I	H20
K21	O	3.3 V	RGMII	RGMII2_TX_CTL	65	66	RGMII2_RX_CTL	RGMII	3.3 V	I	G25
–	P	0 V	Power	DGND	67	68	DGND	Power	0 V	P	–
AE11	I	1.8 V	PCIE	PCIE_RX_N	69	70	PCIE_TX_N	PCIE	1.8 V	O	AC11
AD11	I	1.8 V	PCIE	PCIE_RX_P	71	72	PCIE_TX_P	PCIE	1.8 V	O	AB11
–	P	0 V	Power	DGND	73	74	DGND	Power	0 V	P	–
AE10	I	1.8 V	PCIE	PCIE_REFCLK_IN_N	75	76	PCIE_REFCLK_OUT_N	PCIE	1.8 V	O	AC10
AD10	I	1.8 V	PCIE	PCIE_REFCLK_IN_P	77	78	PCIE_REFCLK_OUT_P	PCIE	1.8 V	O	AB10
–	P	0 V	Power	DGND	79	80	DGND	Power	0 V	P	–

5: Reserved pin without function. Do not connect!
6: Pull-Up on carrier board required.

4.1.2 I²C address mapping

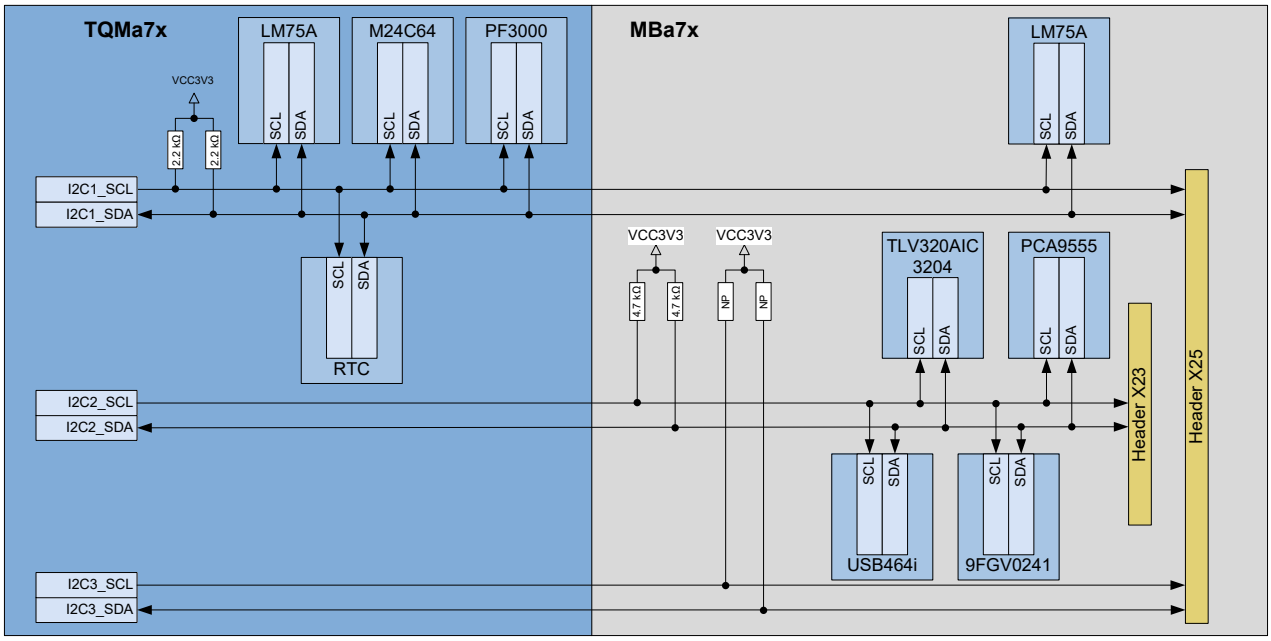

Figure 3: Block diagram I²C buses

I2C1 and I2C2 are used on the MBa7x. I2C3 is freely available.
The LM75A temperature sensors on the MBa7x and the TQMa7x are connected to I2C1.
Audio codec TLV320AIC3204, port expander PCA9555, HSIC USB hub USB4604i and PCIe clock generator 9FGV0241 are connected at I2C2. All three I²C buses are also routed to 100 mil headers X23 and X25 on the MBa7x.
The following table shows the I²C addresses used.

Table 10: I²C address assignment

I²C bus	Used on	Device	Reference	7-bit address	Remark
I2C1	TQMa7x	EEPROM (M24C64)	–	0x50 / 101 0000b	–
		Temperature sensor (LM75A)	–	0x48 / 100 1000b	–
		RTC (DS1339U)	–	0x68 / 110 1000b	(Assembly option)
		PMIC (PF3000 / PF3001)	–	0x08 / 000 1000b	Should not be altered
	MBa7x	Temperature sensor (LM75A)	D2102	0x49 / 100 1001b	–
I2C2		Audio codec (TLV320AIC3204)	N2000	0x18 / 001 1000b	–
		GPIO expander (PCA9555)	D2100	0x20 / 010 0000b	–
		HSIC HUB (USB4604i)	D800	0x2D / 010 1101b	–
		Clock generator (9FGV0241)	D1900	0x6A / 110 1010b	–

Attention:	I2C1 bus
	Attention when using I2C1. Since the PMIC can be addressed on I2C1, errors on the bus can lead to instabilities of the TQMa7x!

4.1.3 Temperature sensor

An LM75A sensor is available on the TQMa7x and a second one on the MBa7x.
Both sensors are connected to I2C1 and have different addresses, see 4.1.2.
The address of the sensor on the MBa7x can be changed by reassembling configuration resistors.
If the address is changed, care has to be taken to avoid address conflicts with other I²C devices.

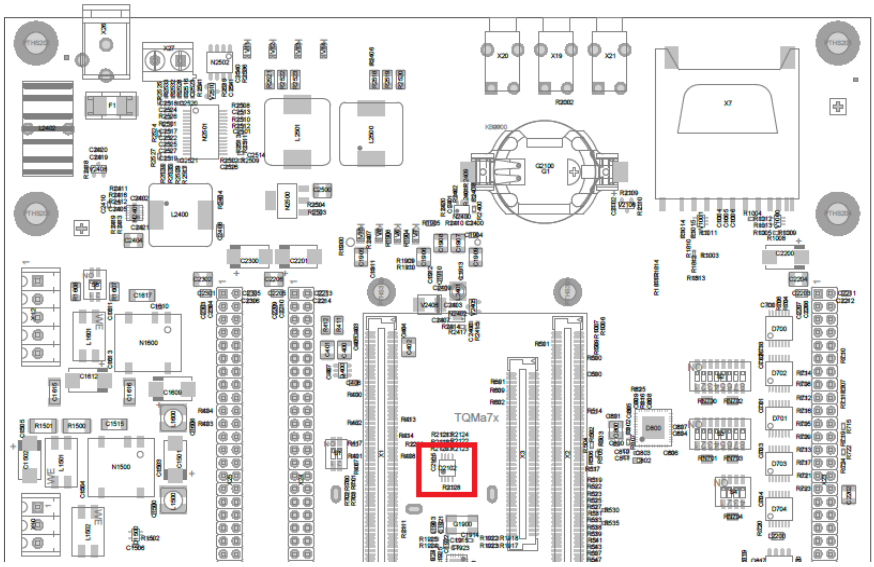

Figure 4: Position of temperature sensor LM75 on MBa7x

Table 11: Electrical characteristics LM75A

Manufacturer	Resolution	Accuracy	Temperature range	Error
NXP	0.125 °C	11 bit	–25 °C to +100 °C –55 °C to +125 °C	±2 °C ±3 °C

➢ The temperature sensor on the MBa7x has I²C address `0x49 / 100 1001b`.

4.1.4 RTC backup

A CR2032 lithium battery with very low self-discharge is populated on the MBa7x to back-up the RTC on the TQMa7x.
The TQMa7x provides an i.MX7-internal RTC and an optional, discrete RTC.
Both RTCs are supplied by the lithium battery via pin LICELL of the TQMa7x.

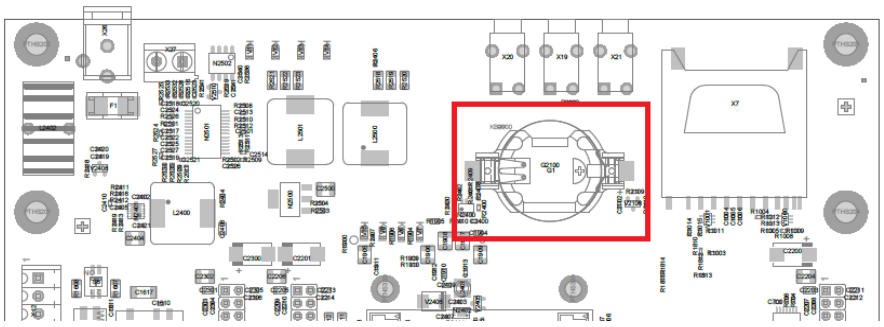

Figure 5: Position of RTC backup battery

The increased current consumption must be considered, if the RTC in the i.MX7 is used. This leads to a fast discharge of the battery. More information can be found in the TQMa7x User's Manual.

The following tables show details of the RTC backup supply.

Table 12: Electrical characteristics RTC backup supply

Parameter	Value	Remark
Coin cell voltage	2.1 V to 3.7 V	3.0 V typical
Current consumption i.MX7 RTC	7.1 µA typical	10 µA maximal @ T_{amb} = +25 °C
Current consumption discrete RTC DS1339U-33	440 nA typical	7 µA maximal @ T_{amb} = +25 °C

Table 13: RTC backup supply, components

Manufacturer / Number	Description
Sony / CR2032	Lithium battery 3.0 V, 220 mAh
RENATA / SMTU2032	CR2032 battery holder

4.1.5 Port Expander

The 16-port port expander PCA9555 is used to control several components on the MBa7x. These include the alarm buzzer, User LEDs, User GPIOs, configuration signals for Mini PCIe and navigation buttons.

The port expander is configured via I2C2. The sensor address can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices. In the initial state after power-on, all ports are set as input and the connected component is thus deactivated.

The following tables show details of port expander D2100.

Table 14: Functions of port expander D2100

Port	Signal	Dir. [7]	Default [8]	Remark
IO0_0	BUZZER	O	Low	Buzzer On / Off
IO0_1	LVDS_SHDN#	O	High	Enable for LVDS transceiver SN75LVD
IO0_2	SC_MOD_VCC	O	Low	Supply voltage 1.8 V / 3 V for Smart card (X6)
IO0_3	PE_GPIO3	I/O	High	GPIO3 at X25-40
IO0_4	PE_GPIO4	I/O	High	GPIO4 at X25-42
IO0_5	PE_GPIO5	I/O	High	GPIO5 at X25-44
IO0_6	PE_GPIO6	I/O	High	GPIO6 at X25-46
IO0_7	PE_GPIO7	I/O	High	NC (only routed to test point TP2132 on MBa7x)
IO1_0	LED1	O	Low	Green LED On / Off
IO1_1	LED2	O	Low	Green LED On / Off
IO1_2	VCC3V3_MPCIE_EN	O	Low	Enable-Signal for 3.3 V PCIe supply voltage
IO1_3	VCC12V_EN	O	Low	Enable-Signal for 12 V supply voltage
IO1_4	VCC1V5_MPCIE_EN	O	Low	Enable-Signal for 1.5 V PCIe supply voltage
IO1_5	SWITCH_A#	I	High	Input for navigation push button “A“
IO1_6	SWITCH_B#	I	High	Input for navigation push button “B“
IO1_7	SWITCH_C#	I	High	Input for navigation push button “C“

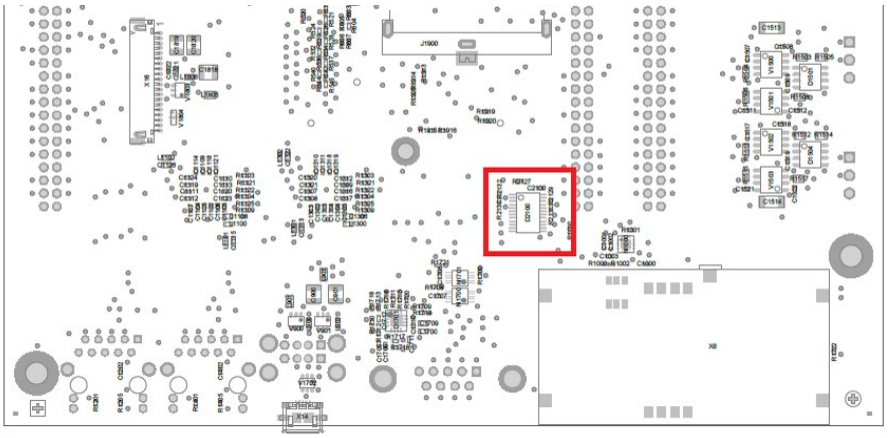

Figure 6: Position of port expander D2100

7: Planned port configuration.
8: Initial state for Off/Inactive mode.

4.1.6 Power Management and Reset

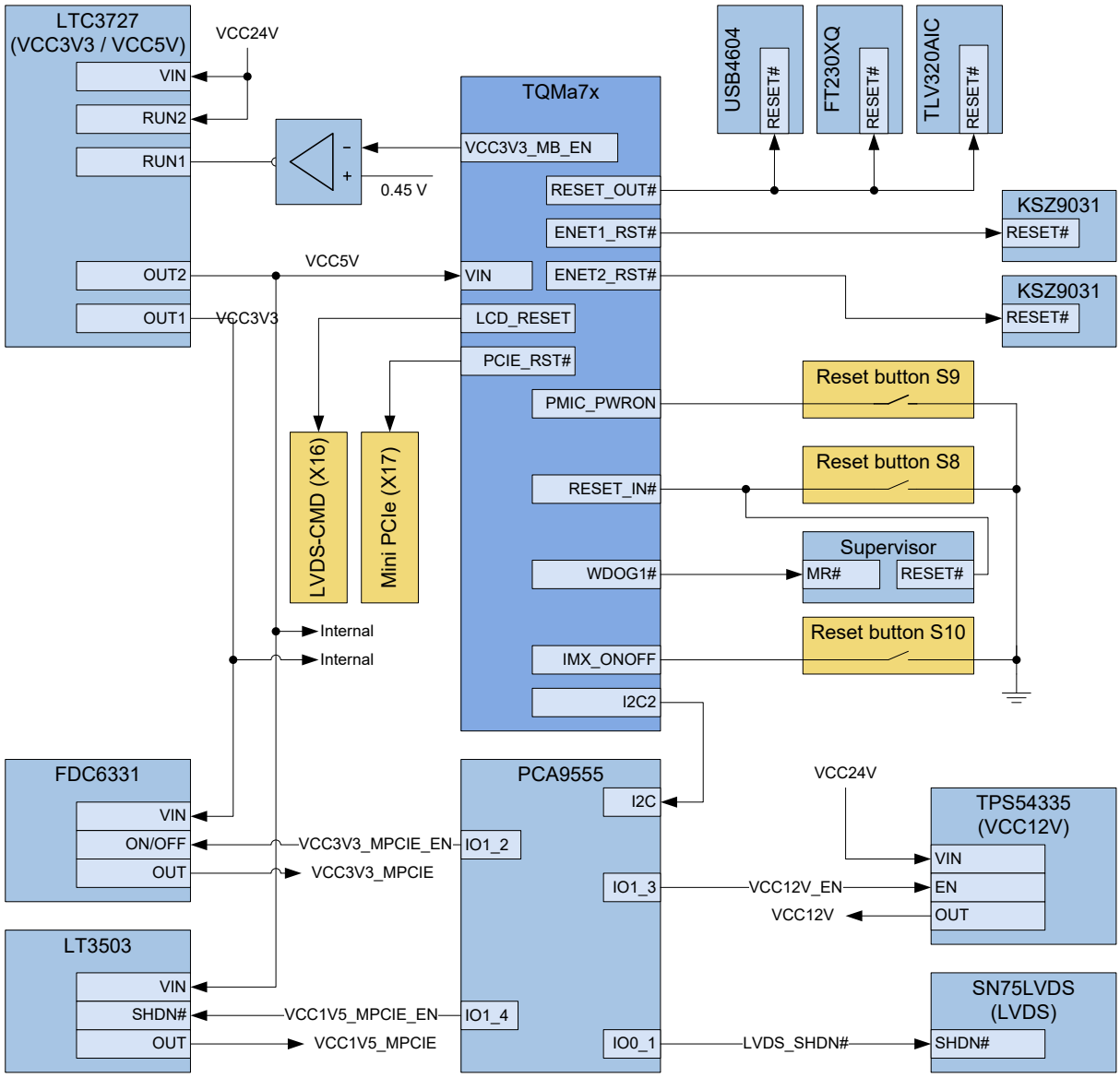

Figure 7: Block diagram Power and Reset

4.1.6 Power Management and Reset (continued)

The MBa7x provides several options to trigger a complete or partial reset of the MBa7x.
The following table shows the signals used.

Table 15: MBa7x Reset signals

Signal	Source	Dir.	Default	Remark
VCC3V3_MB_EN	TQMa7x ⇨ PMIC	O	Low	• Switches on the carrier board control for 3.3 V.
LCD_RESET	TQMa7x ⇨ i.MX7	O	High	• See User's Manual TQMa7x. • To be configured as reset signal by driver.
PCIE_RST#	TQMa7x ⇨ i.MX7	O	High	
VCC3V3_MPCIE_EN	Port-Expander IO1_2	O	Low	• Enable for Mini PCIe power supply
VCC1V5_MPCIE_EN	Port-Expander IO1_4	O	Low	• Enable for Mini PCIe power supply
VCC12V_EN	Port-Expander IO1_3	O	Low	• Enable for 12 V supply (display)
LVDS_SHDN#	Port-Expander IO0_1	O	High	• Reset for LVDS Transceiver
PMIC_PWRON	TQMa7x ⇨ PMIC	I	High	• See User's Manual TQMa7x. • Usable by user button S9.
RESET_IN#	TQMa7x ⇨ i.MX7	I	High	• See User's Manual TQMa7x. • Usable by user button S8.
IMX_ONOFF#	TQMa7x ⇨ i.MX7	I	High	• See User's Manual TQMa7x. • Usable by user button S10.
RESET_OUT#	TQMa7x	O	High	• See User's Manual TQMa7x. • Becomes active when i.MX7 reset is active. • Reset for peripherals on carrier board.
ENET1_RST#	TQMa7x ⇨ i.MX7	O	High	• Reset for Ethernet PHY 1 • Can be configured as reset signal by driver.
ENET2_RST#	TQMa7x ⇨ i.MX7	O	High	• Reset for Ethernet PHY 2 • Can be configured as reset signal by driver.
WDOG1#	TQMa7x ⇨ i.MX7	O	High	• Used for software/warm reset. • Controls the reset input of the module. • To be configured as WDOG signal by driver.

4.1.7 Power supply

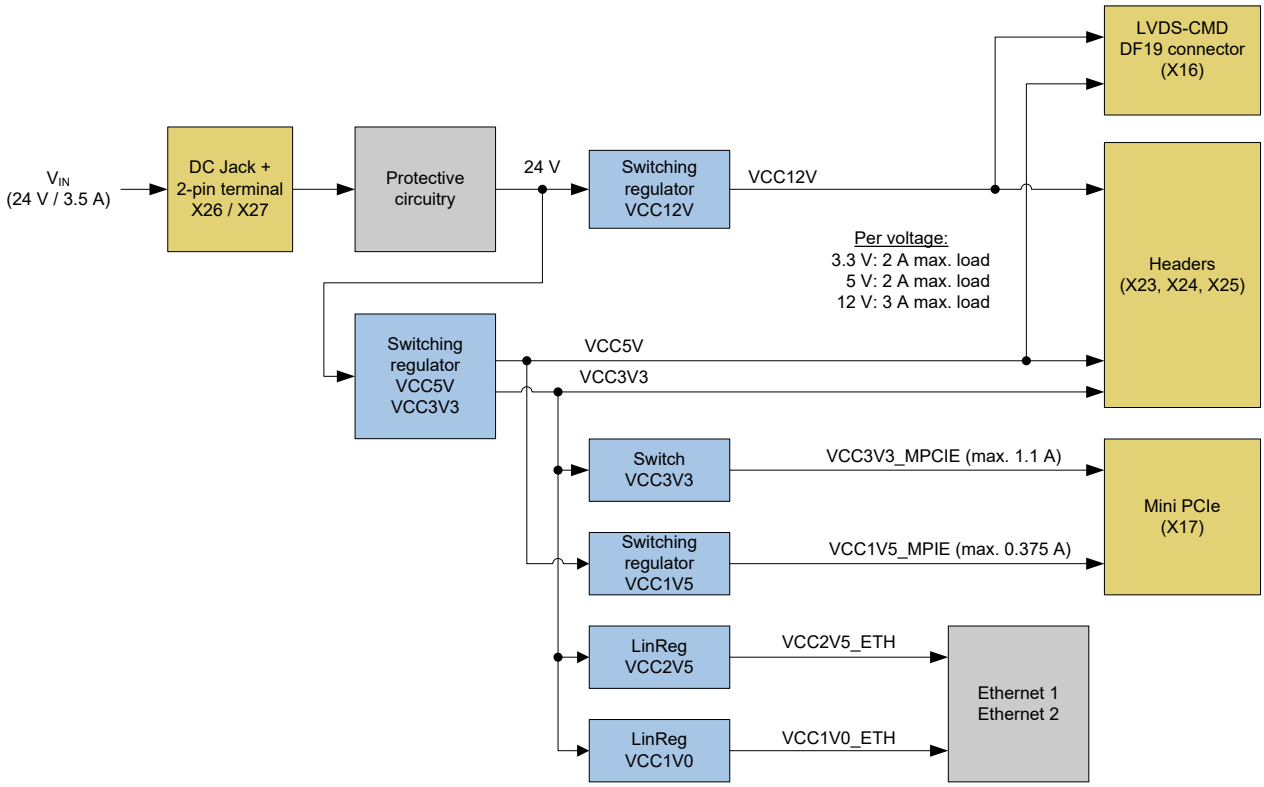

Figure 8: Block diagram power supply

The MBa7x is supplied with 24 V via X26 or X27. From this voltage 1.0 V, 1.5 V, 2.5 V, 3.3 V, 5 V and 12 V are generated on the MBa7x. These voltages are used to supply the components on the MBa7x.

Additionally, 3.3 V, 5 V and 12 V are available at each of the three headers (X23, X24, and X25). 5 V and 12 V are available at the LVDS-CMD connector (X16). All five connectors share the available power (2 A @ 3.3 V, 2 A @ 5 V, 3 A @ 12 V).

The PCIe connector is supplied with 1.5 V and 3.3 V. 1.5 V is generated from 5 V and is only available at the PCIe connector. The 1.5 V rail can supply 0.375 A, the 3.3 V rail can supply 1.1 A.

When VCC12V_EN is High, VCC12V is powered. When VCC12V_EN is Low, VCC12V is switched off.

Attention:	Usage of VCC3V3_MB_EN
	The VCC3V3 power supply on the carrier board should be switched with signal VCC3V3_MB_EN by the TQMa7x, to avoid cross supply and errors in the power-up/down sequence. [9]

9: Attention: When the PMIC is switched off, the voltage VCC3V3_REFOUT (from the TQMa7x) drops to approx. 2.7 V due to cross-supply effects of the still activated 3.3 V (on the MBa7x). It must be ensured that the circuitry can respond to this level.

4.1.7.1 Protective circuitry

V_{IN} of the MBa7x also supplies the 3.3 V / 5 V and the 12 V buck regulators on the MBa7x.
The protective circuit (Figure 9) has the following characteristics:

- Fuse, 4 A, slow blow
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

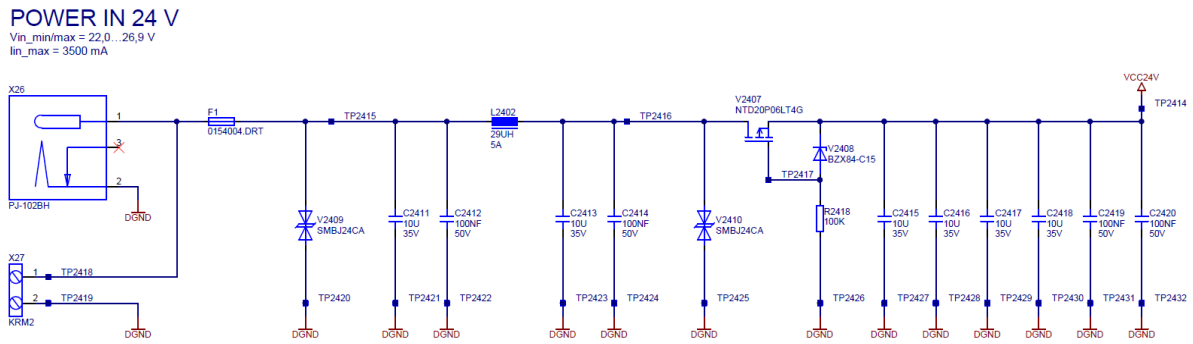

Figure 9: Protective circuit for V_{IN}

Table 16: Characteristics of protective circuit

Parameter	Min.	Typ.	Max.
Overcurrent limitation by fuse (slow blow)	–	4 A	–
Excess voltage limitation by SMBJ24CA	26.7 V	–	26.9 V

4.1.7.2 Power consumption

When operating the MBa7x with the TQMa7x, power peaks of up to approx. 85 W can occur if all supply voltages from external modules at the headers are loaded with maximum current. The power supply used must be designed accordingly.

At 100 % CPU load MBa7x and TQMa7x consume approx. 6.5 W.

To measure the power consumption of the TQMa7x, two 50 mΩ resistors connected in parallel are assembled on the MBa7x.

The following figures show circuitry and position of the two 50 mΩ resistors on the MBa7x.

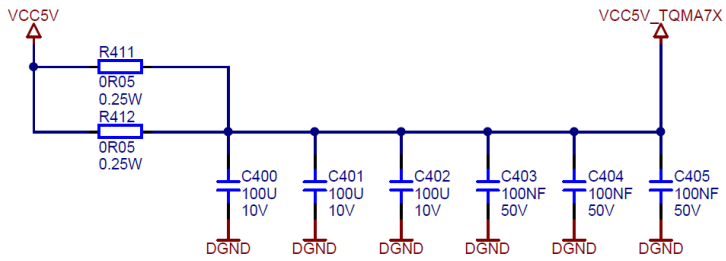

Figure 10: Schematics of shunts on MBa7x

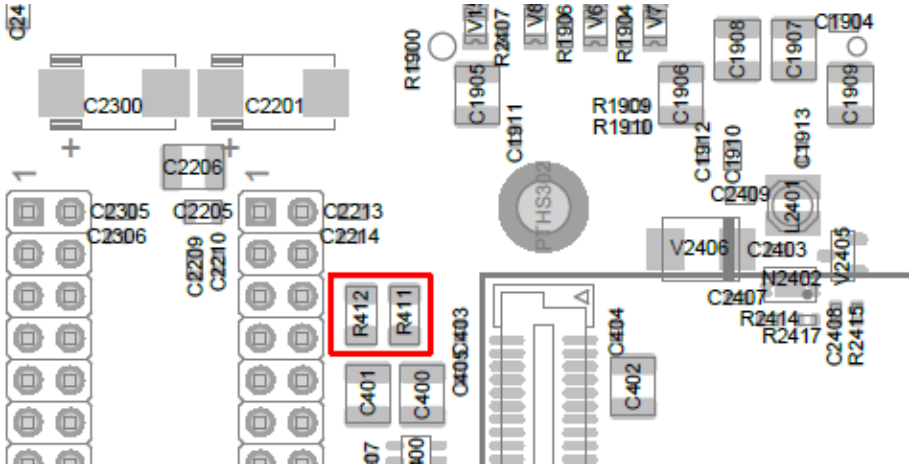

Figure 11: Position of shunts on MBa7x

4.1.7.3 Power supply connectors

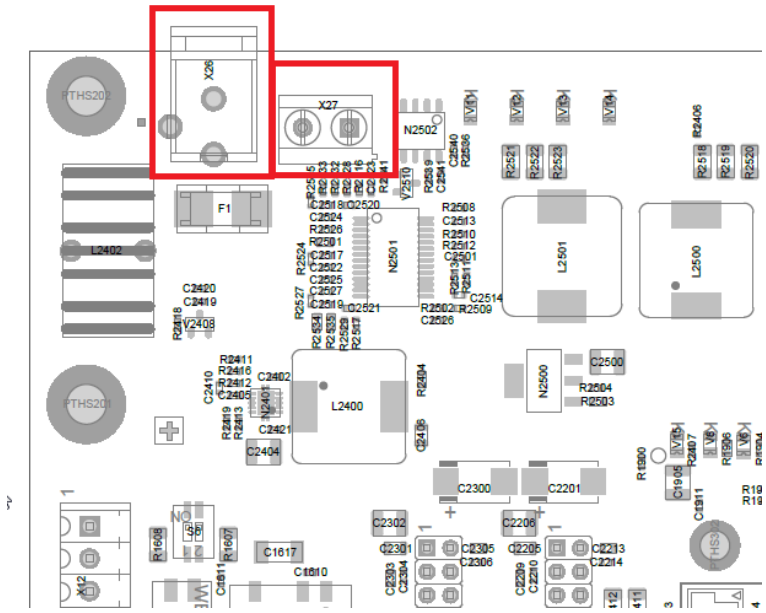

Figure 12: Position of power supply connectors – X26, X27

Table 17: Types of power supply connectors

Connector	Manufacturer / Number	Description
X26	Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V
X27	Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A

4.2 Communication interfaces

4.2.1 USB 2.0 Hi-Speed Host

The TQMa7x provides a chip-to-chip connection for USB via HSIC.
The HSIC USB hub USB4604 offers four USB 2.0 Hi-Speed host interfaces. (One upstream port, four downstream ports.)
The USB connectors are supplied with 5 V via power distribution switches. These switches provide current monitoring and can switch off the bus voltage in case of an overload and/or overheating.
For detailed information, refer to the MIC2026 switch Data Sheets.

- USB Hosts 1 & 2 are connected to the stacked USB Type A socket X4
  USB Host 1 is the lower Type A connector, USB Host 2 is the upper Type A connector
- USB Host 3 is routed to LVDS-CMD connector X16
- USB Host 4 is routed to header X23

The firmware required by the USB hub is loaded by default from its own internal memory. As an assembly option, the USB hub can be connected to the I2C2 bus on the MBa7x. In this case, the firmware can also be loaded into the hub via this bus when the system is started. Further information can be found in the Data Sheets of the USB4604 (9) and the current MBa7x circuit diagram.

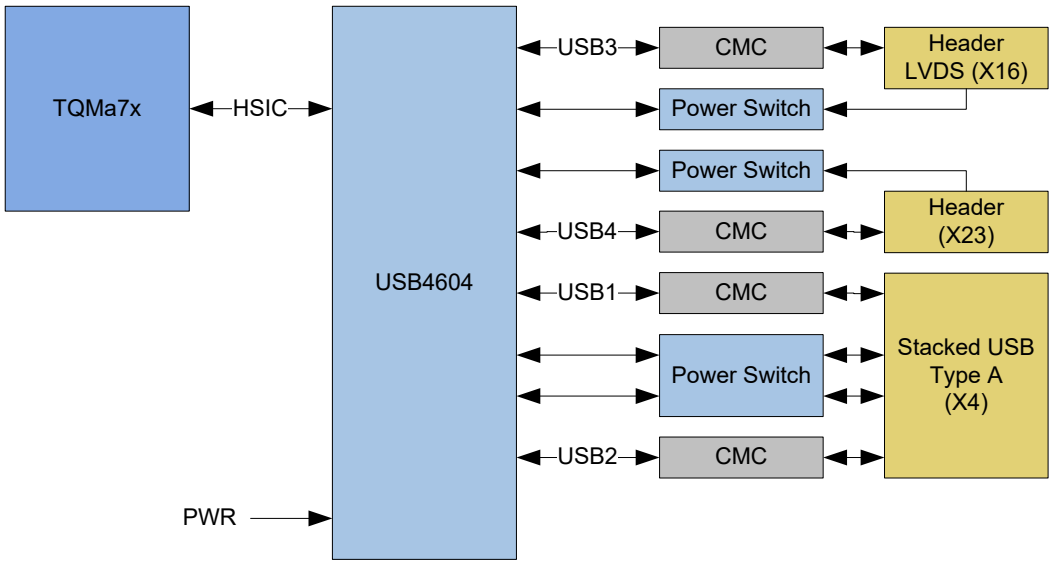

Figure 13: Block diagram USB-Hosts

The USB Host port of the TQMa7x provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

Table 18: Characteristics USB Host

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	–
Current	–	500	900	mA	–
Load step change	–	–90	–	mV	Load step of 500 mA
Read rate	–	27	–	Mbyte/s	USB-HDD at Port 2: 2 Gbyte file, 10 Mbyte block size
Write rate	–	22	–	Mbyte/s	USB-HDD at Port 2: 2 Gbyte file, 16 Mbyte block size

4.2.1 USB 2.0 Hi-Speed Host (continued)

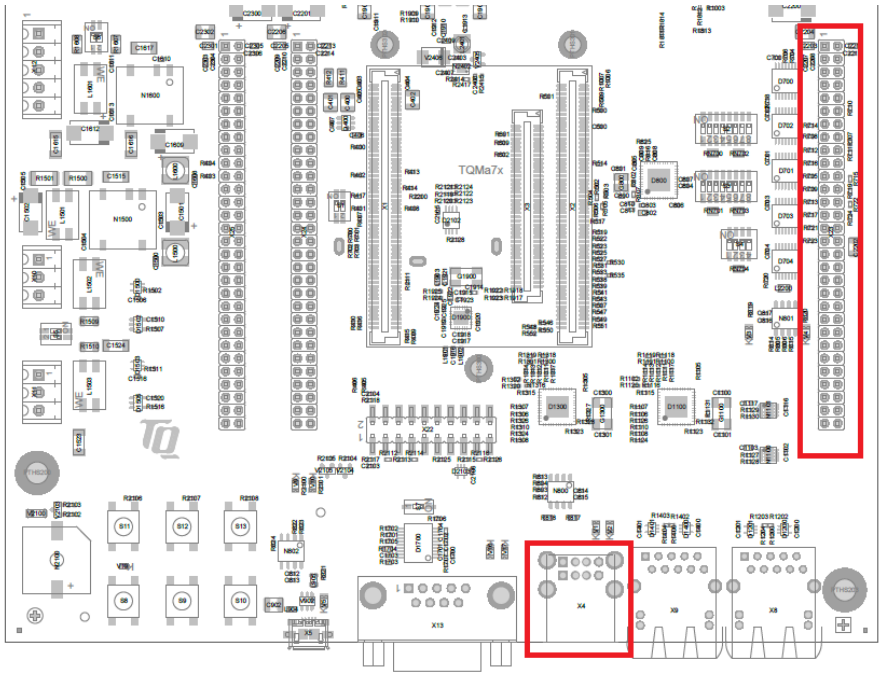

Figure 14: Position of USB-Host Top

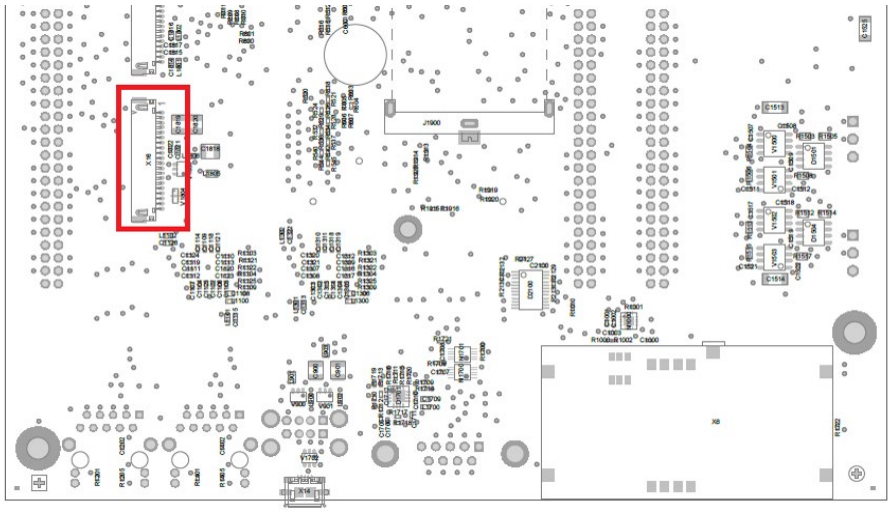

Figure 15: Position of USB-Host Bottom

4.2.1 USB 2.0 Hi-Speed Host (continued)

Table 19: Types of USB connectors

Manufacturer / Number	Description
Yamaichi / USB-A-002A	Dual port USB receptacle, Type-A, U_N=30 V AC_{RMS} / I_N=1 A
Hirose / DF19G-20P-1H	Board-to-Cable connector 20-pin, 1 mm pitch

Table 20: Pinout USB-Host 1 & 2 (stacked)

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H1_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H1_D_N	I/O	Common Mode Choke in series
3A	D+	USB_H1_D_P	I/O	Common Mode Choke in series
4A	DGND	DGND	P	–
1B	VBUS	USB_H2_VBUS	P	100 µF to DGND; EMI filter
2B	D–	USB_H2_D_N	I/O	Common Mode Choke in series
3B	D+	USB_H2_D_P	I/O	Common Mode Choke in series
4B	DGND	DGND	P	–
M1-4	DGND	DGND	P	–

Table 21: Pinout USB-Host 3 (LVDS-CMD X16)

Pin	Pin name	Signal	Dir.	Remark
11	VBUS	USB_H6_VBUS	P	100 µF to DGND; EMI filter
12	DGND	DGND	P	–
13	D–	USB_H3_D_N	I/O	Common Mode Choke in series
14	D+	USB_H3_D_P	I/O	Common Mode Choke in series
15	DGND	DGND	P	–

Table 22: Pinout USB-Host 4 (Header X23)

Pin	Pin name	Signal	Dir.	Remark
34	VBUS	USB_H4_VBUS	P	100 µF to DGND; EMI filter
36	D–	USB_H4_D_N	I/O	Common Mode Choke in series
37	DGND	DGND	P	–
38	D+	USB_H4_D_P	I/O	Common Mode Choke in series

4.2.2 USB 2.0 Hi-Speed OTG

Both USB-OTG interfaces of the TQMa7x are provided on the MBa7x. OTG1 is available with all module variants as 5-pin Micro AB socket. OTG2 is only available at the Mini PCIe connector when the TQMa7D is used.

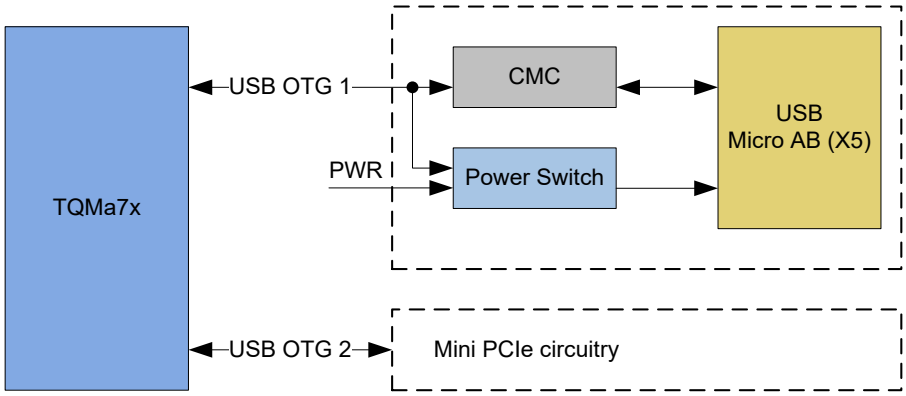

Figure 16: Block diagram USB 2.0 Hi-Speed OTG

The interface can be a client or a host. To use this feature the appropriate software support is necessary, however.
The OTG port provides a theoretical data rate of 480 Mbit/s. The data rate can significantly deviate depending on the hardware and software used.

Table 23: Characteristics USB 2.0 Hi-Speed OTG

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	–
Current	–	500	900	mA	–
Load step change	–	–85	–	mV	Load step of 500 mA
Read rate	–	27.6	–	Mbyte/s	USB-HDD at USB-OTG: 2 Gbyte file, 10 Mbyte block size
Write rate	–	22	–	Mbyte/s	USB-HDD at USB-OTG: 2 Gbyte file, 10 Mbyte block size

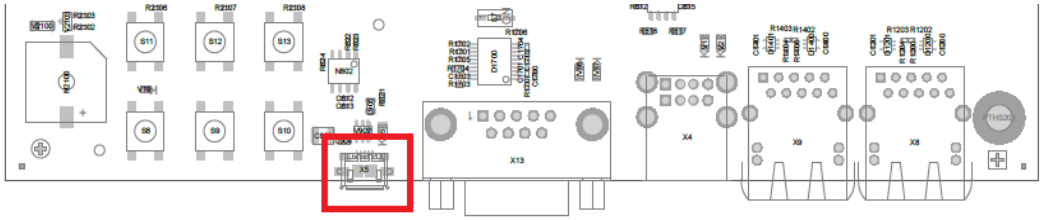

Figure 17: Position of USB 2.0 Hi-Speed OTG, X5

4.2.2 USB 2.0 Hi-Speed OTG (continued)

Table 24: Type of USB Micro AB receptacle

Manufacturer / Number	Description
TE Connectivity / 1981584-1	USB receptacle, type Micro AB

Table 25: Pinout USB-OTG1 (USB Micro AB, X5)

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB_OTG1_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
2	D–	USB_OTG1_D_N	I/O	Common Mode Choke in series
3	D+	USB_OTG1_D_P	I/O	Common Mode Choke in series
4	ID	USB_OTG1_ID	I	–
5	DGND	DGND	P	–
M1-6	DGND	DGND	P	–

Table 26: Pinout USB-OTG2 (USB Mini PCIe, X17)

Pin	Pin name	Signal	Dir.	Remark
34	VBUS	USB_OTG2_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
36	D–	USB_OTG2_D_N	I/O	Common Mode Choke in series
38	D+	USB_OTG2_D_P	I/O	Common Mode Choke in series
40	ID	USB_OTG2_ID	I	–

4.2.3 Ethernet 1000BASE-T

Both Ethernet MACs of the TQMa7x are connected on the MBa7x via RGMII to two TI PHYs DP83867.
The TQMa7D offers both MACs and thus both Ethernet interfaces, the TQMa7S offers only one Ethernet interface.
The PHY DP83867 is started via boot straps with default values. All boot straps can be customized with assembly options.
Further information can be found in the current circuit diagram of the MBa7x.

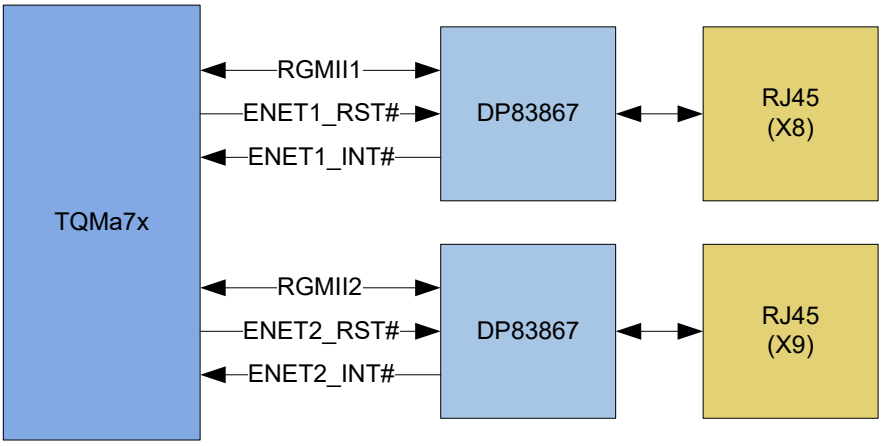

Figure 18: Block diagram Ethernet 100 BASE-T

RJ45 connectors X8 and X9 provide integrated magnetics and two status LEDs each.

This Ethernet interface corresponds to the IEEE 802.3 standard and offers an Auto-MDI-X detection.
The data throughput depends on the system load and the software used. With the BSP provided by TQ-Systems GmbH, the following transfer rates can be achieved on the MBa7x.

Table 27: Characteristics Ethernet 1000BASE-T

Parameter	Min.	Typ.	Max.	Unit	Remark
Upstream	–	578	1000	Mbit/s	Remote station: Full Duplex 1 Gbit Eth-IF over CAT 5e
Downstream	–	722	1000	Mbit/s	

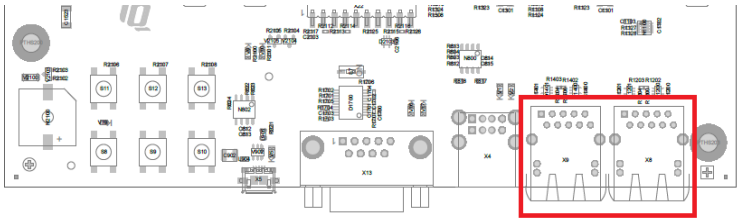

Figure 19: Position of Ethernet 1000BASE-T – X8, X9

Table 28: Type of Ethernet 1000BASE-T connectors

Manufacturer / Number	Description
Würth / 7499111449	RJ45 receptacle, 10/100/1000Base-T integrated magnetics

4.2.3 Ethernet 1000BASE-T (continued)

The following tables show the pin assignment of the RJ45 Ethernet jacks:

Table 29: Pinout Ethernet 1000BASE-T

Connector	Pin	Pin name	Signal
X8	1	D1+	ENET1_A_P
	2	D1–	ENET1_A_N
	3	D2+	ENET1_B_P
	4	D3+	ENET1_C_P
	5	D3–	ENET1_C_N
	6	D2–	ENET1_B_N
	7	D4+	ENET1_D_P
	8	D4–	ENET1_D_N
X9	1	D1+	ENET2_A_P
	2	D1–	ENET2_A_N
	3	D2+	ENET2_B_P
	4	D3+	ENET2_C_P
	5	D3–	ENET2_C_N
	6	D2–	ENET2_B_N
	7	D4+	ENET2_D_P
	8	D4–	ENET2_D_N

4.2.4 CAN

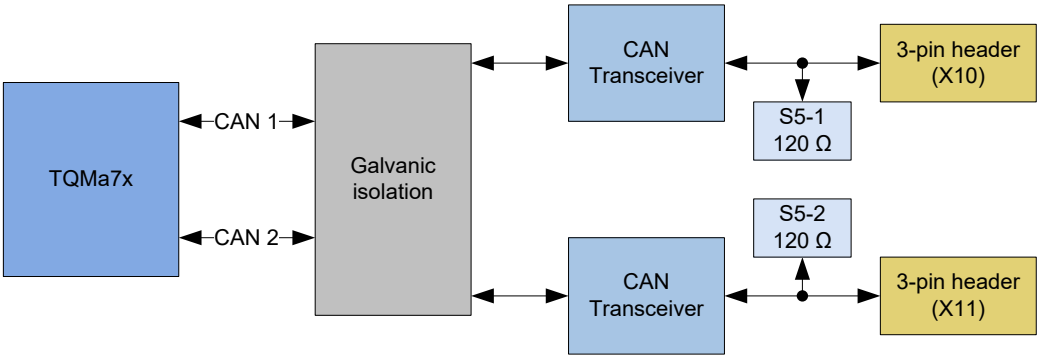

Figure 20: Block diagram CAN

Both CAN interfaces on the MBa7x are directly connected to the CAN ports of the TQMa7x and made available at the 3-pin connectors X10 and X11. Both interfaces are galvanically isolated with a dielectric strength of 1 kV.
The CAN interfaces are galvanically not isolated from each other.

The High-Speed mode is configured by default using a configuration resistor at the input RS of the CAN transceiver MCP2551 (390 Ω to Ground ⇨ maximum slew rate).

The High-Speed mode supports data rates up to 2 Mbit/s or maximum cable length. When required, the resistor at the RS input can be increased (10 … 120 kΩ) to reduce the slew rate. [10]

The CAN signals can be terminated with 120 Ω using DIP switches S5-1 and S5-2.

Table 30: CAN termination, DIP switch S5 settings

Switch	Interface	ON	OFF
S5-1	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated
S5-2	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated

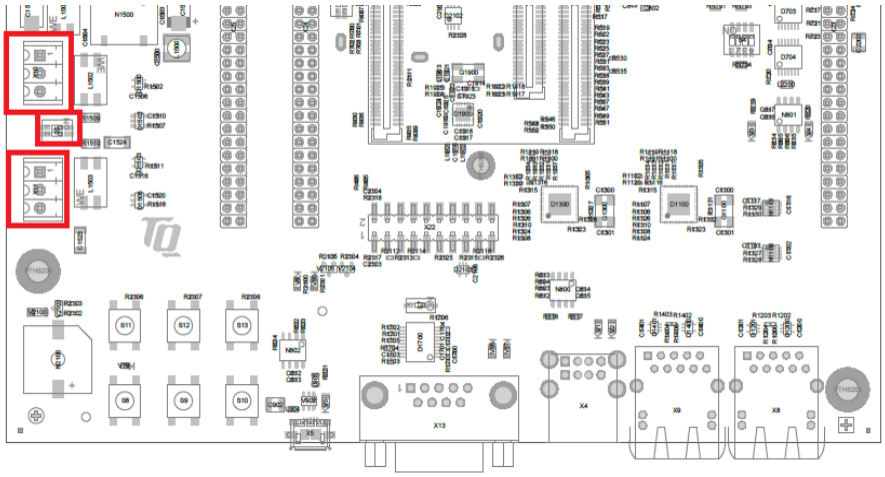

Figure 21: Position of CAN – X10, X11, S5

10: See data sheet MCP2551.

4.2.4 CAN (continued)

Table 31: Type of CAN connector

Manufacturer / Number	Description
Phoenix Contact / MCV 1,5/3-G-3,5	3-pin housing, 160 V / 8 A, 3.5 mm pitch

Table 32: Pinout CAN1 – X10

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN1_H	I/O	Galvanically isolated
2	CAN_L	CAN1_L	I/O	Galvanically isolated
3	DGND	DGND_CAN	P	Galvanically isolated

Table 33: Pinout CAN2 – X11

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN2_H	I/O	Galvanically isolated
2	CAN_L	CAN2_L	I/O	Galvanically isolated
3	DGND	DGND_CAN	P	Galvanically isolated

The following characteristics apply to the CAN interfaces:

Table 34: CAN characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	2.0	Mbaud	–
Line length	–	–	100	m	CAT.6 cable at 0.5 Mbaud
Line length	–	–	0.1	m	CAT.5 cable at 2 Mbaud
Dielectric strength	–	–	1.0	kV	–
Output voltage CANL	0.5	1.6	2.25	V	Dominant
Output voltage CANL	2.0	2.58	3.0	V	Recessive
Output voltage CANH	2.75	3.7	4.5	V	Dominant
Output voltage CANH	2.0	2.58	3.0	V	Recessive
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

4.2.5 RS-485

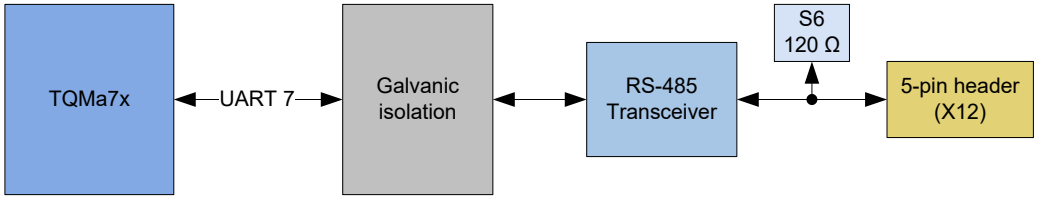

Figure 22: Block diagram RS-485

The TQMa7x UART7 interface is routed to an RS-485 transceiver (SP491), which provides the signals at the 9-pin D-Sub connector X12. The RS-485 interface is galvanically isolated with 1 kV.
The interface is configured for full duplex operation by default, but can be switched to half duplex by an assembly option.
In this case, the receiver is controlled by UART7.CTS#. The assembly option is described in the current circuit diagram.

Table 35: RS-485 mode settings

Mode	R1511	R1512	Remark
Full-duplex	(NP)	0 Ω	Receiver always active (default)
Half-duplex	0 Ω	(NP)	Receiver controlled by CTS# (UART4.CTS#)

The RS-485 signals can be terminated with 120 Ω using DIP switches S6-1 and S6-2.

Table 36: RS-485 termination, DIP switch S6 settings

Switch	ON	OFF
S6-1	Receive path terminated with 120 Ω	Receive path not terminated
S6-2	Transmit path terminated with 120 Ω	Transmit path not terminated

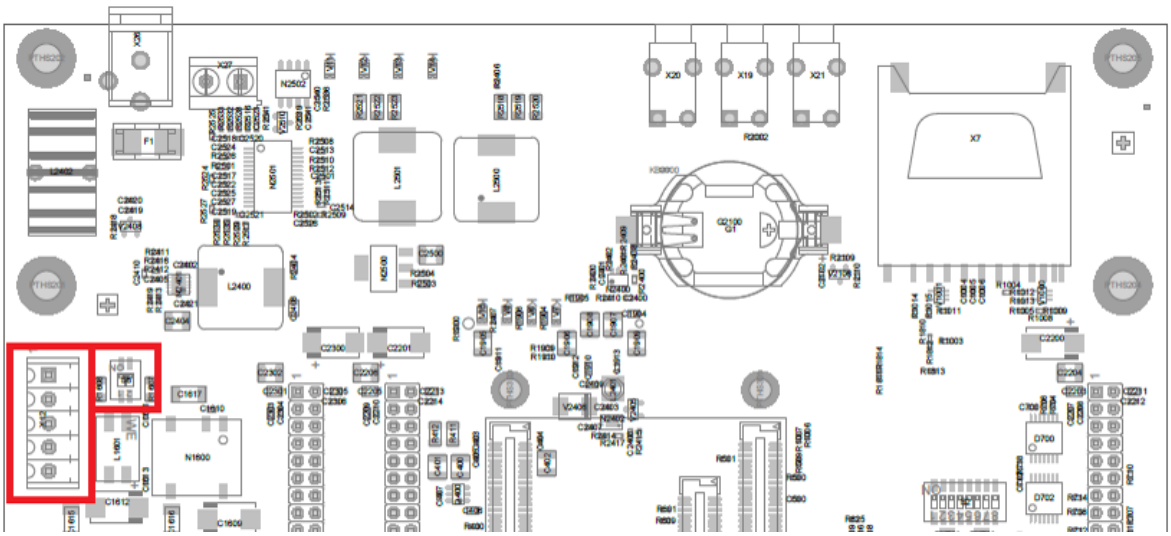

Figure 23: Position of RS-485 – X12

4.2.5 RS-485 (continued)

Table 37: Type of RS-485 connector

Manufacturer / Number	Description
Phoenix Contact / MCV1,5/5-G-3,5	5-pin housing , 160 V / 8 A, 3.5 mm pitch

Table 38: Pinout RS-485 – X12

Pin	Pin name	Signal	Dir.	Remark
1	A	RS-485_A	I	Galvanically isolated
2	B	RS-485_B	I	Galvanically isolated
3	Y	RS-485_Y	O	Galvanically isolated
4	Z	RS-485_Z	O	Galvanically isolated
5	DGND	DGND_RS-485	P	Galvanically isolated

The following characteristics apply to the interface:

Table 39: Characteristics RS-485

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	921.6	kbit/s	–
Dielectric strength	–	–	1	kV	–
Output swing RS-485_Y/Z	–	10.6	–	V	High-Level (No load)
Output swing RS-485_Y/Z	–	4.44	–	V	High-Level (27 Ω load)
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

4.2.6 Debug interfaces RS-232 / USB

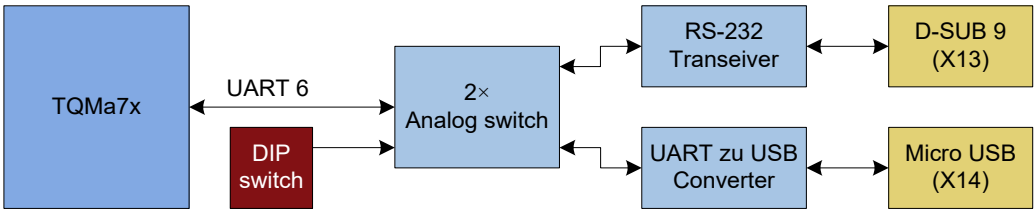

Figure 24: Block diagram RS-232 / Debug

The debug interface is implemented on the MBa7x as RS-232 and USB device interface. In both cases the UART6 interface of the TQMa7x is used. No software configuration is necessary. The interface is selected with the DIP switch S7, see Table 41.

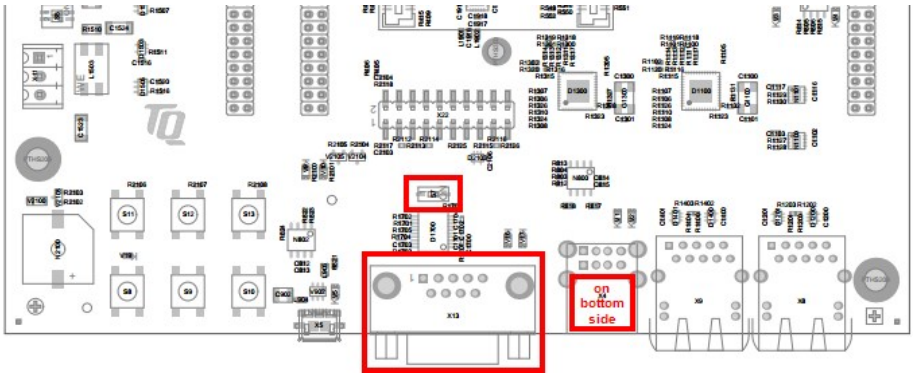

Figure 25: Position of RS-232 (X13), USB (X14)

Table 40: Type of RS-232 connector

Manufacturer / Number	Description
Yamaichi / DRA-09P11-ZN	D-Sub-9 connector
Tyco / 1981584-1	USB connector, Micro AB

The debug interface can be set to RS-232 or USB with DIP switch S7.

Table 41: Debug interface, DIP switch S7 settings

Switch	ON	OFF
S7	Debug-Interface USB-Device at X14	Debug-Interface RS-232 at X13

4.2.6 Debug interfaces RS-232 / USB (continued)

Table 42: Pinout Debug RS-232, D-Sub-9 – X13

Pin	Signal
1, 4, 6, 9	NC
2	RS-232_RXD
3	RS-232_TXD
7	RS-232_RTS#
8	RS-232_CTS#
5	DGND
M1, M2	DGND

Table 43: Pinout Debug USB, USB Micro AB – X14

Pin	Signal
1	VBUS_SENSE
2	USB_DBG_D_N
3	USB_DBG_D_P
4	NC
5	DGND
M1-6	DGND

4.2.7 LVDS

An LVDS display can be connected to the MBa7x (4× TX pairs). Since the i.MX7 processor does not have a native LVDS interface, the LVDS signals are generated by the SN75LVDS83B transceiver connected to the parallel LCD interface.
The LVDS interface is routed to two DF19 connectors.
The first connector (30-pin, X15) provides the LVDS data signals as well as 3.3 V and 5 V.
The second connector (20-pin, X16) provides control lines and USB signals as well as 12 V and 5 V.
A High level at LVDS_SHDN# switches the LVDS transceiver on, a Low level at LVDS_SHDN# switches the LVDS transceiver off.
The LVDS transceiver is configured for 8-bit FORMAT-1 mode and operates at 65 MHz [11].

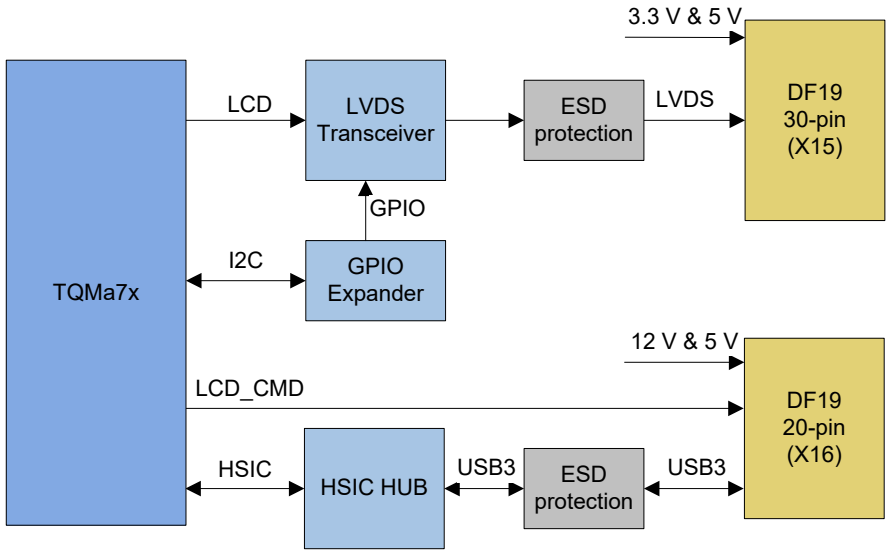

Figure 26: Block diagram LVDS

The characteristics of the interface are determined by the LVDS transmitter in the i.MX7.
More information can be taken from the Reference Manual of the respective i.MX7.

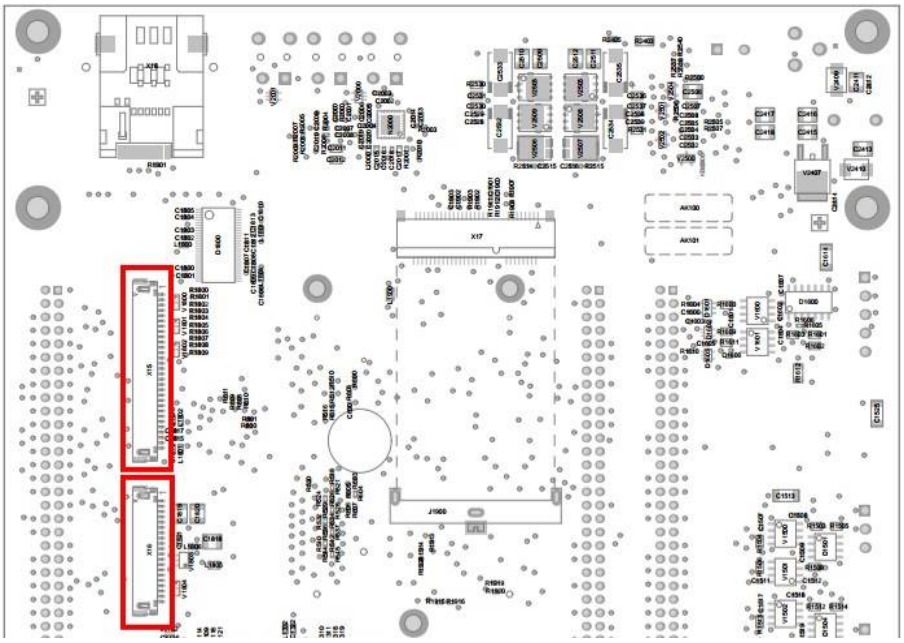

Figure 27: Position of LVDS connectors – X15, X16

11: See Texas Instruments Data Sheet SN75LVDS83B.

4.2.7 LVDS (continued)

Table 44: Type of LVDS connectors

Connector	Manufacturer / Number	Description
X15	Hirose / DF19G-30P-1H	Board-to-Cable FFC connector, 30-pin, 1 mm pitch
X16	Hirose / DF19G-20P-1H	Board-to-Cable FFC connector, 20-pin, 1 mm pitch

Table 45: Pinout LVDS – X15

Pin	Signal	Remark
1	LVDS0_TX0_N	ESD protection
2	LVDS0_TX0_P	ESD protection
3	LVDS0_TX1_N	ESD protection
4	LVDS0_TX1_P	ESD protection
5	LVDS0_TX2_N	ESD protection
6	LVDS0_TX2_P	ESD protection
7	DGND	–
8	LVDS0_CLK_N	ESD protection
9	LVDS0_CLK_P	ESD protection
10	LVDS0_TX3_N	ESD protection
11	LVDS0_TX3_P	ESD protection
12	NC	–
13	NC	–
14	DGND	–
15	NC	–
16	NC	–
17	DGND	–
18	NC	–
19	NC	–
20	NC	–
21	NC	–
22	NC	–
23	NC	–
24	DGND	–
25	5 V	–
26	5 V	–
27	5 V	–
28	3.3 V	–
29	3.3 V	–
30	3.3 V	–
M1-2	DGND	–

4.2.7 LVDS (continued)

Table 46: Pinout LVDS-CMD – X16

Pin	Signal	Remark
1	12 V	–
2	12 V	–
3	12 V	–
4	DGND	–
5	DGND	–
6	DGND	–
7	5 V	–
8	5 V	–
9	DGND	–
10	DGND	–
11	USB_H3_VBUS	ESD protection
12	DGND	–
13	USB_H3_D_N	ESD protection + Common Mode Choke in series
14	USB_H3_D_P	ESD protection + Common Mode Choke in series
15	DGND	–
16	#LCD_RESET	ESD protection
17	LCD_BLT_EN	ESD protection
18	LCD_PWR_EN	ESD protection
19	LCD_CONTRAST	ESD protection
20	DGND	–
M1	DGND	–
M2	DGND	–

4.2.8 Audio

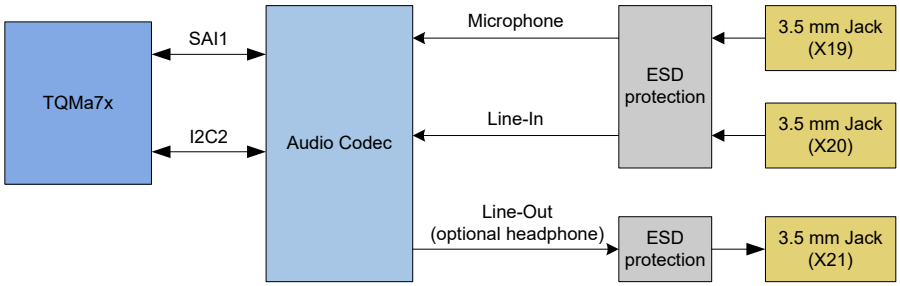

Figure 28: Block diagram audio

Audio input and outputs are provided by the audio codec TLV320AIC. It is connected to the TQMa7x via SAI (configured as I²S) and I²C. The audio codec provides microphone, line in and line out signals. The signals are routed to 3.5 mm jacks.
An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 47: Configuration Line-Out / headphone

Mode	R2005	R2007	R2008	R2009	Remark
Line-Out	0 Ω	0 Ω	NP	NP	Default
Headphone (optional)	NP	NP	0 Ω	0 Ω	–

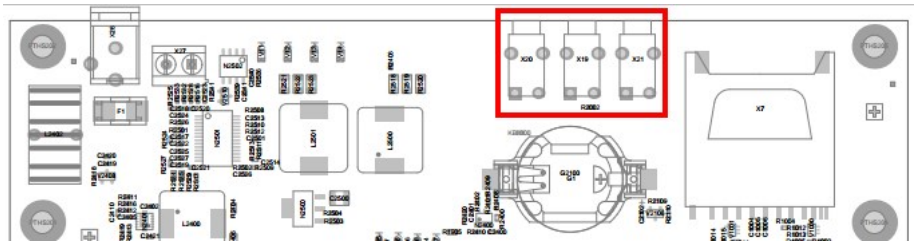

Figure 29: Position of audio connectors – X19, X20, X21

4.2.8 Audio (continued)

Table 48: Type of audio jack

Manufacturer / Number	Description
Yamaichi / LJE3530K	Jack 3.5 mm

Table 49: Pinout Microphone – X19

Pin	Signal	Remark
1	AGND_AUDIO	–
2A,2B	MIC_IN	2.2 kΩ in series to MIC_BIAS; ESD protection
3	AGND_AUDIO	10 kΩ to AGND_AUDIO, right channel not used

Table 50: Pinout Line-In – X20

Pin	Signal	Remark
1	AGND_AUDIO	–
2A,2B	LINE_IN_L	470 nF in series; ESD protection
3	LINE_IN_R	470 nF in series; ESD protection

Table 51: Pinout Line-Out – X21

Pin	Signal	Remark
1	AGND_AUDIO	–
2A,2B	AUDIO_OUT_L	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; ESD protection. Optional connection to HP_L
3	AUDIO_OUT_R	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; ESD protection. Optional connection to HP_R

4.2.9 SD card

The SD card slot is directly connected with the SDHC controller of the TQMa7x with a 4-bit interface.
The SDHC controller in the TQMa7x supports the UHS-I mode, which is not used on the MBa7x.
The maximum available mode is High-Speed. Booting from SD card is possible, see chapter 4.3.5.
All data lines are ESD protected.

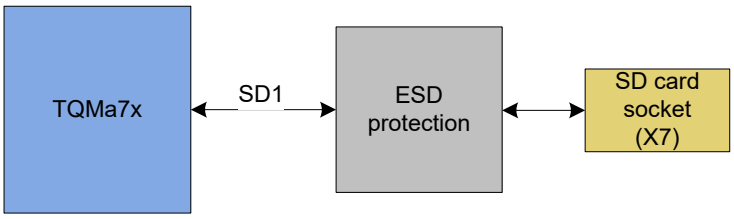

Figure 30: Block diagram SD card

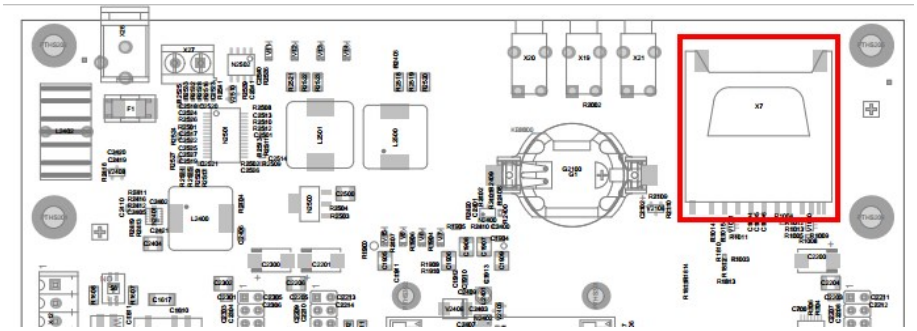

Figure 31: Position of SD card – X7

Table 52: Type of SD card connector

Manufacturer / Number	Description
Yamaichi / FPS009-2405-0	SD-/MMC card connector

Table 53: Pinout SD card – X7

Pin	Pin name	Signal	Remark
1	CD/DAT3/CS	SD1_DATA3	ESD protection
2	CMD/DI	SD1_CMD	10 kΩ Pull-Up to VCC3V3 + ESD protection
3	VSS1	DGND	–
4	VDD	VCC3V3	–
5	CLK	SD1_CLK	ESD protection
6	VSS2	DGND	–
7	DAT0/DO	SD1_DATA0	ESD protection
8	DAT1	SD1_DATA1	ESD protection
9	DAT2	SD1_DATA2	ESD protection
CDS	CARD_DETECT	SD1.CD#	10 kΩ Pull-Up to VCC3V3 + ESD protection
COM	COMMON	DGND	–
WP	WRITE_PROTECT	SD1.WP	10 kΩ Pull-Up to VCC3V3 + ESD protection
M1-2	SHIELD	DGND	SHIELD

4.2.10 Mini PCIe

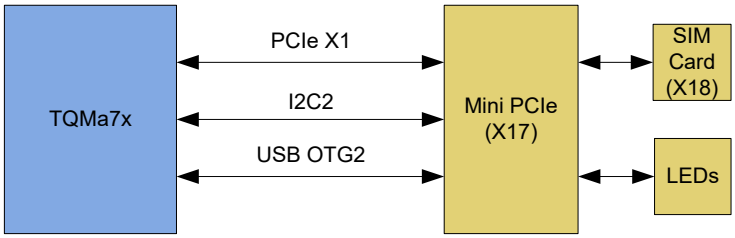

Figure 32: Block diagram Mini PCIe

A Mini PCIe slot (PCIe ×1) for full-size cards is available on the MBa7x. Pin assignment see Table 56.
Any standard compliant Mini PCIe card can be used.
An additional SIM card holder is installed to use a GSM card, see chapter 4.2.11.

- A high level at VCC3V3_MPCIE_EN switches VCC3V3_MPCIE on, a low level switches VCC3V3_MPCIE off.
- A high level at VCC1V5_MPCIE_EN switches VCC1V5_MPCIE on, a low level switches VCC1V5_MPCIE off.

Both voltages are switched off by default.

Table 54: Max currents, Mini PCIe

Parameter	Min.	Typ.	Max.
Current @ 3.3 V	–	–	1.1 A
Current @ 1.5 V	–	–	0.375 A

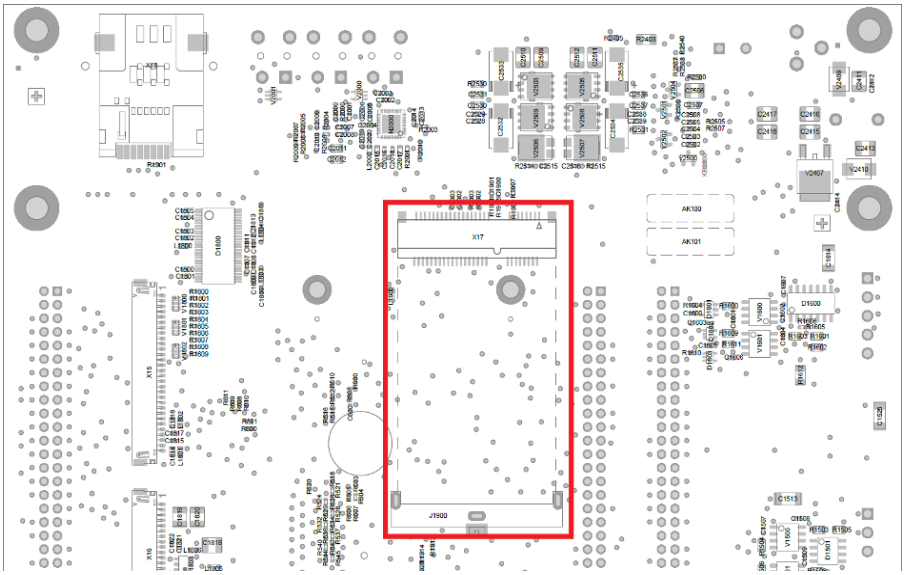

Figure 33: Position of Mini PCIe – X17, J1900

4.2.10 Mini PCIe (continued)

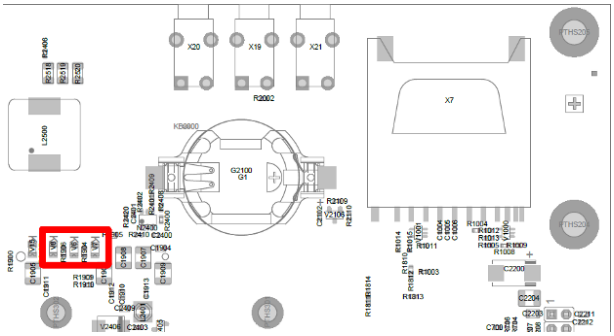

Figure 34: Position of Mini PCIe Status LEDs, V6, V7, V8

Table 55: Mini PCIe interface, components

Manufacturer / Number	Description
Nexus / 5020HB56R	Mini PCIe connector
Nexus / 5022M56R	Mini PCIe retainer

Attention:	Mini PCIe card, dimensions, max. current
	When using PCIe cards, the distance between the board and the card must be taken into account. The connector for the card is located 3.7 mm above the board. With a heat sink screw connection with a maximum protrusion of 2 mm, the space defined in the PCIe specification is available. The voltages provided for the Mini PCIe card may be loaded with the maximum currents specified in Table 54.

Note:	TQMa7x interfaces
	The Mini-PCIe interface can only be used with the TQMa7D, since the TQMa7S does not offer the interfaces PCIe and USB-OTG2.

4.2.10 Mini PCIe (continued)

Table 56: Pinout Mini PCIe – X17

Pin	Signal	Remark
1	PCIE_WAKE#	–
2	VCC3V3_MPCIE	See Table 54
3	NC	–
4	DGND	–
5	NC	–
6	VCC1V5_MPCIE	See Table 54
7	NC	–
8	UIM_PWR	SIM card signal, see Table 58
9	DGND	-
10	UIM_DATA	SIM card signal, see Table 58
11	PCIE_REFCLK_N	Optional CLK source: CPU or oscillator. 49.9 Ω to DGND, see 4.2.11
12	UIM_CLK	SIM card signal, see Table 58
13	PCIE_REFCLK_P	Optional CLK source: CPU or oscillator. 49.9 Ω to DGND, see 4.2.11
14	UIM_RST	SIM card signal, see Table 58
15	DGND	-
16	UIM_VPP	SIM card signal, see Table 58
17	NC	–
18	DGND	–
19	NC	–
20	PCIE_DIS#	–
21	DGND	–
22	PCIE_RST#	–
23	PCIE_RX_N	
24	VCC3V3_MPCIE	See Table 54
25	PCIE_RX_P	
26	DGND	–
27	DGND	–
28	VCC1V5_MPCIE	See Table 54
29	DGND	–
30	I2C2.SCL	–
31	PCIE_TX_N	100 nF in series
32	I2C2.SDA	I2C2 address mapping see Table 10
33	PCIE_TX_P	100 nF in series
34	DGND	–
35	DGND	–
36	USB_OTG2_D_N	Common Mode Choke in series
37	DGND	–
38	USB_OTG2_D_P	Common Mode Choke in series
39	VCC3V3_MPCIE	See Table 54
40	DGND	–
41	VCC3V3_MPCIE	See Table 54
42	LED_WWAN#	Connected to VCC3V3_MPCIE with 330 Ω and green LED
43	DGND	–
44	LED_WLAN#	Connected to VCC3V3_MPCIE with 330 Ω and green LED
45	NC	–
46	LED_WPAN	Connected to VCC3V3_MPCIE with 330 Ω and green LED
47	NC	–
48	VCC1V5_MPCIE	See Table 54
49	NC	–
50	DGND	–
51	NC	–
52	VCC3V3_MPCIE	See Table 54

4.2.11 SIM card

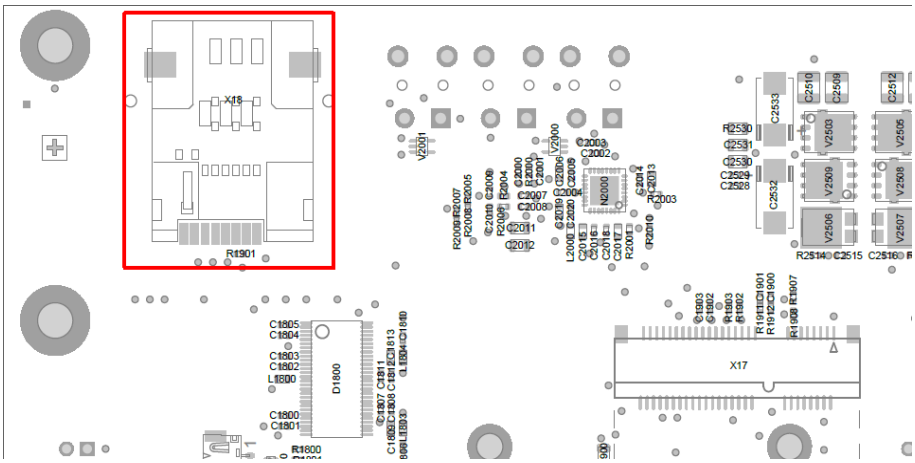

Figure 35: Position of SIM card – X18

Table 57: Type of SIM card

Manufacturer / Number	Description
YAMAICHI / FMS006Z-2101-0	SIM card slot

Table 58: Pinout SIM card – X18

Pin	Pin name	Signal
C1	PWR	UIM_PWR
C2	RST	UIM_RST
C3	CLK	UIM_CLK
C4	(NA)	–
C5	DGND	DGND
C6	VPP	UIM_VPP
C7	DATA	UIM_DATA
SW1-2	–	–

4.2.12 PCIe clock generator

The i.MX7 internal clock is not PCIe compliant. For this reason, a PCIe compliant clock can be generated on the MBa7x with a 9FGV0241AKILF clock generator as an assembly option. Figure 36, Figure 37 and Figure 38 show possible clock supplies. Detailed information can be found in the MBa7x schematics.

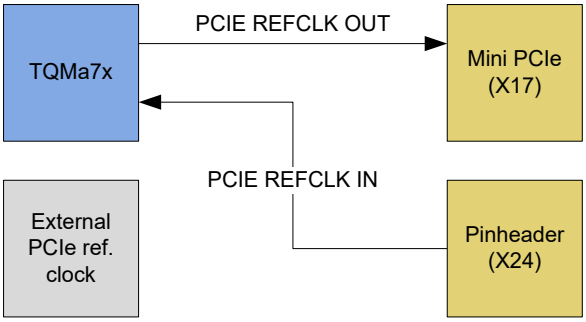

Figure 36: Clock supply PCIe assembly option 1 (default)

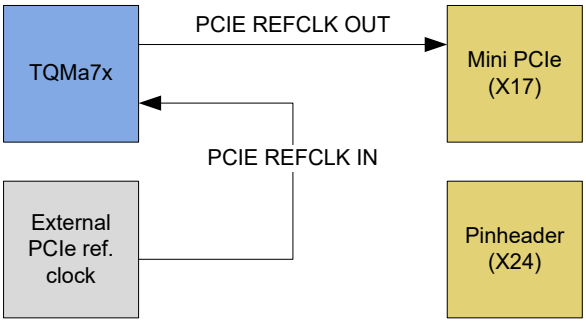

Figure 37: Clock supply PCIe assembly option 2

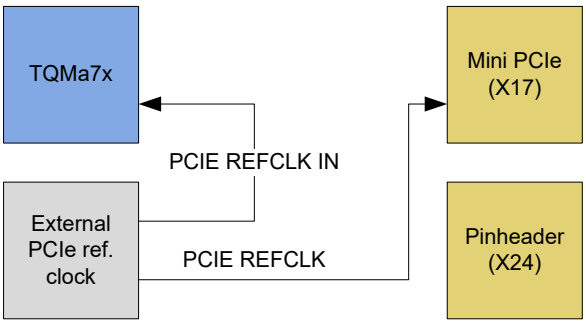

Figure 38: Clock supply PCIe assembly option 3

4.2.13 Smart card X6

The smart card interface on the MBa7x supports Class B (3.0 V) and Class C (1.8 V) cards according to ISO/IEC 7816.
It is not switched automatically between Class B and C, this can be done by software.
(GPIO on Port-Expander 2, SC_MOD_VCC, see Table 14).

- A high level on SC_MOD_VCC switches SIM_VCC to 3 V, a low level switches SIM_VCC to 1.8 V.

SC_MOD_VCC is set to Low by default ⇨ SIM_VCC = 1.8 V.

Note:	5 V Smart cards
	SIM cards that require 5 V supply/signal level are not supported.

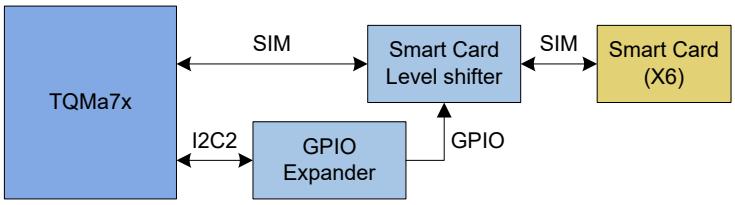

Figure 39: Block diagram Smart card

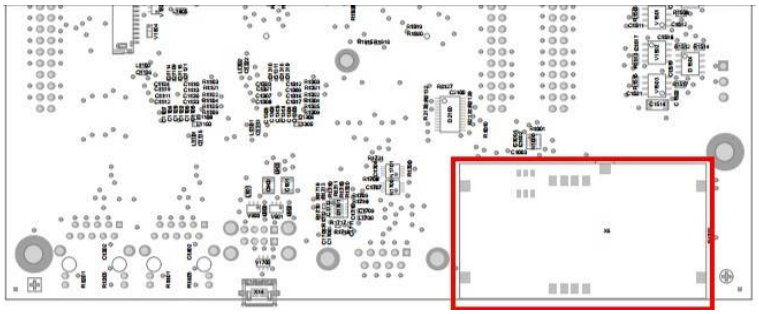

Figure 40: Position of Smart card X6

Table 59: Type of Smart card connector

Manufacturer / Number	Description
Amphenol / C702 10M008 252 40	Smart card connector

Table 60: Pinout Smart card – X6

Pin	Signal	Remark
C1	SIM_PWR	–
C2	SIM_RST	–
C3	SIM_CLK	–
C4	NC	–
C5	DGND	–
C6	NC	–
C7	SIM_DATA	–
C8	NC	–
S1	SIM.PD	10 kΩ Pull-Up to VCC3V3. Connected to DGND with inserted card
S2	DGND	–
M1-M5	DGND	Shield

4.2.14 100 mil Headers

All unused signals are routed to the headers X23, X24, X25 on the MBa7x, to permit a comprehensive evaluation of the TQMa7x modules. All headers are 60-pin with 100 mil pitch.
The headers are positioned in such a way, that adaptor boards which additional electronics and connectors can be plugged in.

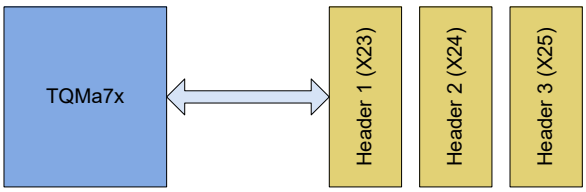

Figure 41: Block diagram headers X23, X24, X25

In addition to the signals, 3.3 V, 5 V and 12 V are available on each header.
Each voltage rail can be loaded with 3 A. The maximum current of a voltage is divided between all headers.

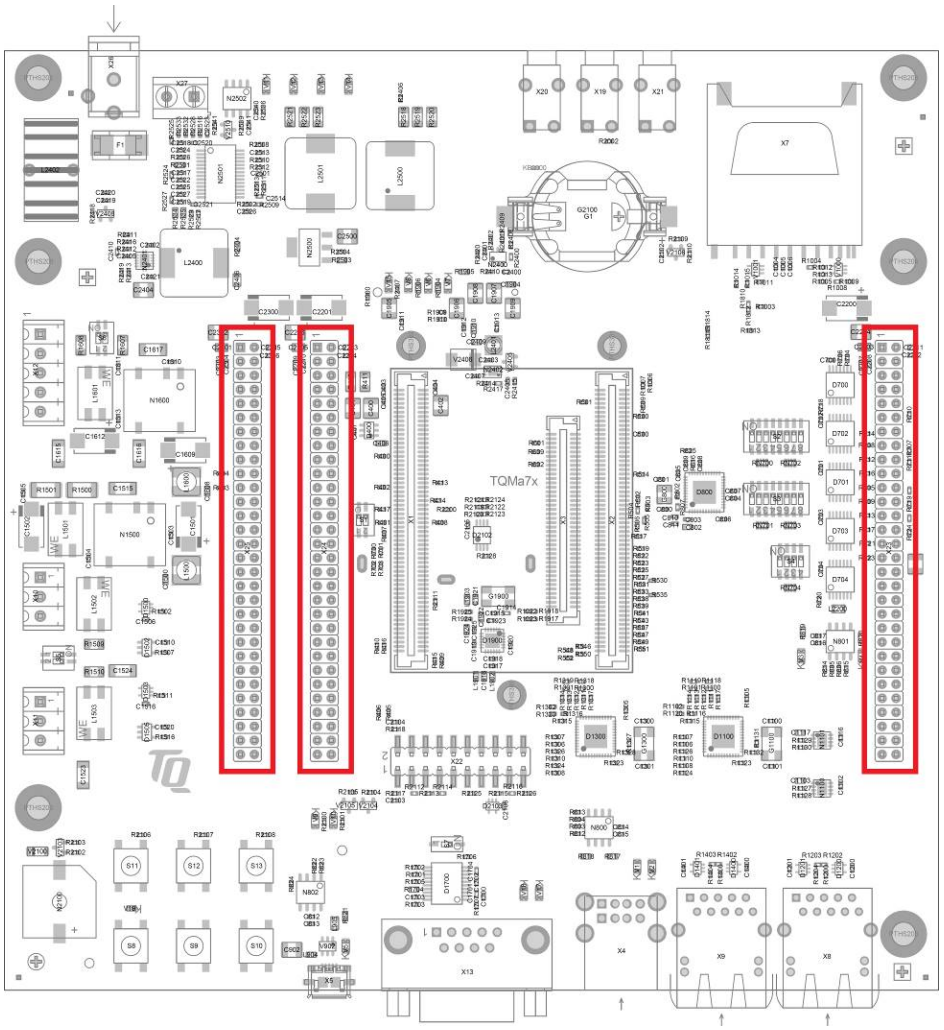

Figure 42: Position of headers – X23, X24, X25

Table 61: Type of 100 mil headers

Manufacturer / Number	Description
Fischer Elektronik / SL 22 124 60 G	Header, 100 mil pitch, 2 × 30 pins

4.2.14 100 mil Headers (continued)

Table 62: Pinout Header 1 – X23

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
LCD	LCD.CLK	7	8	LCD.ENABLE	LCD
LCD	LCD.HSYNC	9	10	LCD.DATA01	LCD
LCD	LCD.VSYNC	11	12	LCD.DATA03	LCD
LCD	LCD.DATA00	13	14	LCD.DATA05	LCD
LCD	LCD.DATA02	15	16	LCD.DATA07	LCD
LCD	LCD.DATA04	17	18	LCD.DATA09	LCD
LCD	LCD.DATA06	19	20	LCD.DATA11	LCD
LCD	LCD.DATA08	21	22	LCD.DATA13	LCD
LCD	LCD.DATA10	23	24	LCD.DATA15	LCD
LCD	LCD.DATA12	25	26	LCD.DATA17	LCD
LCD	LCD.DATA14	27	28	LCD.DATA19	LCD
LCD	LCD.DATA16	29	30	LCD.DATA21	LCD
LCD	LCD.DATA18	31	32	LCD.DATA23	LCD
LCD	LCD.DATA20	33	34	USB_H4_VBUS	Power
LCD	LCD.DATA22	35	36	USB_H4_D_N	USB4
Power	DGND	37	38	USB_H4_D_P	USB4
I2C2	I2C2.SCL	39	40	DGND	Power
I2C2	I2C2.SDA	41	42	ECSPI1.SS2#	SPI1
SPI1	ECSPI1.MOSI	43	44	ECSPI1.MISO	SPI1
SPI1	ECSPI1.SS0#	45	46	ECSPI1.SCLK	SPI1
SPI1	ECSPI1.SS1#	47	48	DGND	Power
LCD	LCD_PWR_EN	49	50	LCD_BLT_EN	LCD
LCD	LCD_RESET#	51	52	LCD_CONTRAST	LCD
Power	DGND	53	54	DGND	Power
Touch	ADC2_IN0	55	56	ADC2_IN2	Touch
Touch	ADC2_IN1	57	58	ADC2_IN3	Touch
Power	DGND	59	60	DGND	Power

4.2.14 100 mil Headers (continued)

Table 63: Pinout Header 2 – X24

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
Power	DGND	7	8	DGND	Power
CCM	CCM_CLK1_P	9	10	DSI.CLK_N	DSI
CCM	CCM_CLK1_N	11	12	DSI.CLK_P	DSI
Power	DGND	13	14	DGND	Power
CCM	CCM_CLK2	15	16	DGND	Power
Power	DGND	17	18	DSI.D0_N	DSI
UART4	UART4.CTS#	19	20	DSI.D0_P	DSI
UART4	UART4.RTS#	21	22	DGND	Power
UART4	UART4.RX	23	24	DSI.D1_N	DSI
UART4	UART4.TX	25	26	DSI.D1_P	DSI
Power	DGND	27	28	DGND	Power
CSI	CSI.D1_P	29	30	PCIE_EXT.REFCLK_IN_N	PCIE_EXT
CSI	CSI.D1_N	31	32	PCIE_EXT.REFCLK_IN_P	PCIE_EXT
Power	DGND	33	34	DGND	Power
CSI	CSI.D0_P	35	36	USB_OTG2_PWR	USB_OTG_2
CSI	CSI.D0_N	37	38	USB_OTG2_OC	USB_OTG_2
Power	DGND	39	40	USB_OTG2_ID	USB_OTG_2
Power	DGND	41	42	USB_OTG1_CHD#	USB_OTG_!
CSI	CSI.CLK_P	43	44	DGND	Power
CSI	CSI.CLK_N	45	46	UART7.RTS#	UART7
Power	DGND	47	48	DGND	Power
ECSPI1	ECSPI1.SS3	49	50	WDOG1#	WDOG1
Power	DGND	51	52	DGND	Power
ADC1	ADC1_IN0	53	54	WDOG2#	WDOG2
ADC1	ADC1_IN1	55	56	WDOG2_RESET#	WDOG2
ADC1	ADC1_IN2	57	58	ADC1_IN3	ADC1
Power	DGND	59	60	DGND	Power

4.2.14 100 mil Headers (continued)

Table 64: Pinout Header 3 – X25

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
QSPI	QSPIA.SCLK	7	8	QSPIA.DATA0	QSPI
Power	DGND	9	10	QSPIA.DATA1	QSPI
QSPI	QSPIA.SS0#	11	12	QSPIA.DATA2	QSPI
QSPI	QSPIA.SS1#	13	14	QSPIA.DATA3	QSPI
QSPI	QSPIA.RESET#	15	16	DGND	Power
Power	DGND	17	18	I2C1.SDA	I2C1
I2C3	I2C3.SDA	19	20	I2C1.SCL	I2C1
I2C3	I2C3.SCL	21	22	DGND	Power
UART5	UART5.RX	23	24	SAI1.RX_BCLK	SAI
UART5	UART5.TX	25	26	SAI1.RX_SYNC	SAI
Power	DGND	27	28	DGND	Power
SD	PMIC_SD_VSELECT	29	30	ECSPI2_SCLK	ECSPI2
SD	SD1_RESET#	31	32	ECSPI2_MISO	ECSPI2
Power	DGND	33	34	ECSPI2_MOSI	ECSPI2
RFU	RFU	35	36	ECSPI2_SS0#	ECSPI2
Power	DGND	37	38	DGND	Power
UART3	UART3.RX	39	40	PE_GPIO3	GPIO
UART3	UART3.TX	41	42	PE_GPIO4	GPIO
UART3	UART3.CTS#	43	44	PE_GPIO5	GPIO
UART3	UART3.RTS#	45	46	PE_GPIO6	GPIO
Power	DGND	47	48	DGND	Power
Tamper	TAMPER8	49	50	TAMPER9	Tamper
Tamper	TAMPER6	51	52	TAMPER7	Tamper
Tamper	TAMPER4	53	54	TAMPER5	Tamper
Tamper	TAMPER2	55	56	TAMPER3	Tamper
Tamper	TAMPER0	57	58	TAMPER1	Tamper
Power	DGND	59	60	DGND	Power

4.3 Diagnostic- and user interfaces

4.3.1 Diagnostic LEDs

The MBa7x provides 22 diagnostic and status LEDs to indicate the system condition.

Table 65: Meaning of diagnostic LEDs

Function	Reference	Colour	Signal
USB	V1	Green	VBUS USB Host 1 (lights up when VBUS of USB Host 1 is active)
	V2	Green	VBUS USB Host 2 (lights up when VBUS of USB Host 2 is active)
	V3	Green	VBUS USB Host 3 (lights up when VBUS of USB Host 3 is active)
	V4	Green	VBUS USB Host 4 (lights up when VBUS of USB Host 4 is active)
	V5	Green	VBUS USB-OTG 1 (lights up when VBUS of USB-OTG 1 is active)
Mini PCIe	V6	Green	Mini PCIe WWAN
	V7	Green	Mini PCIe WLAN
	V8	Green	Mini PCIe WPAN
GPIO-LEDs	V9	Green	LED on Port expander Port IO1_0 (lit when port high)
	V10	Green	LED on Port-Expander Port IO1_1 (lit when port high)
Power	V11	Green	Status 24 V (lights up when supply 24 V active)
	V12	Green	Status 12 V (lights up when supply 12 V active)
	V13	Green	Status 5 V (lights up when supply 5 V active)
	V14	Green	Status 3.3 V (lights up when supply 3.3 V active)
	V15	Green	Status 3.3 V Mini-PCIe (lights up when supply 3.3 V for Mini-PCIe active)
USB-Debug	V16	Green	TX-LED (lights up when transmission is active)
	V17	Green	RX-LED (lights up when transmission active)
Ethernet	X8B	Yellow	Activity LED Ethernet 1 (lights up in case of error)
	X8C	Green	Error LED Ethernet 1 (lights up when link is active, flashes during data transfer)
	X9B	Yellow	Activity LED Ethernet 2 (lights up in case of error)
	X9C	Green	Error LED Ethernet 2 (lights up when link is active, flashes during data transfer)
Reset	V19	Red	Reset LED (lights up when module in reset)

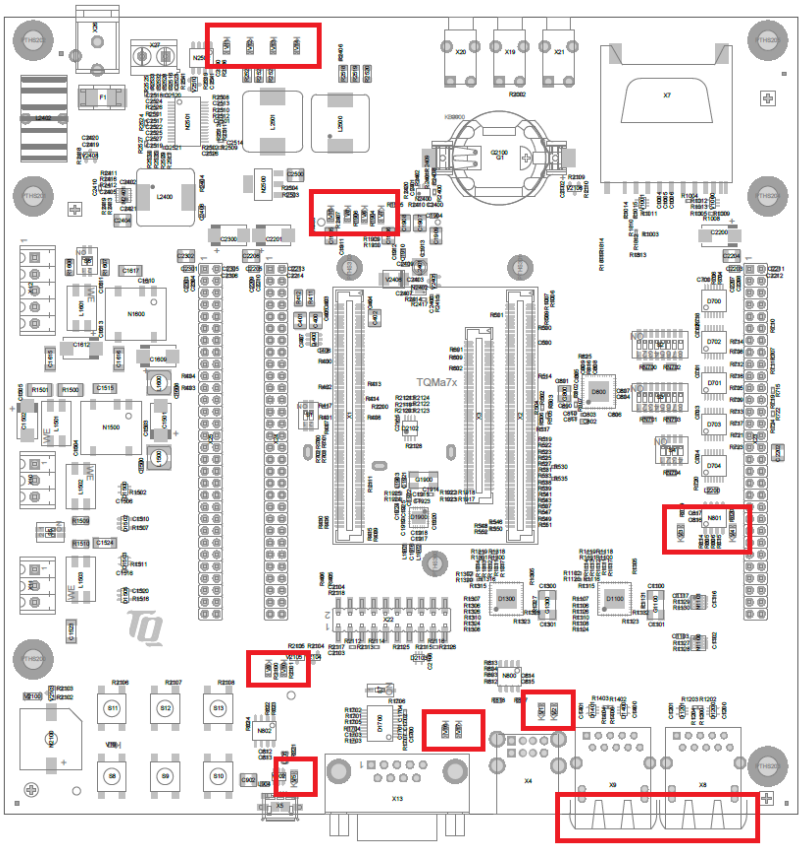

Figure 43: Position of diagnostic LEDs

4.3.2 Navigation buttons

On the MBa7x, three navigation buttons are connected to a port expander PCA9555.
The port expander is interrupt-capable by signal PE1_INT#.

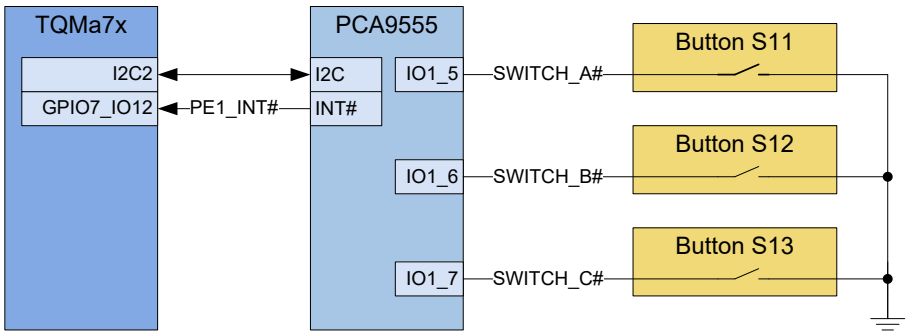

Figure 44: Block diagram navigations buttons

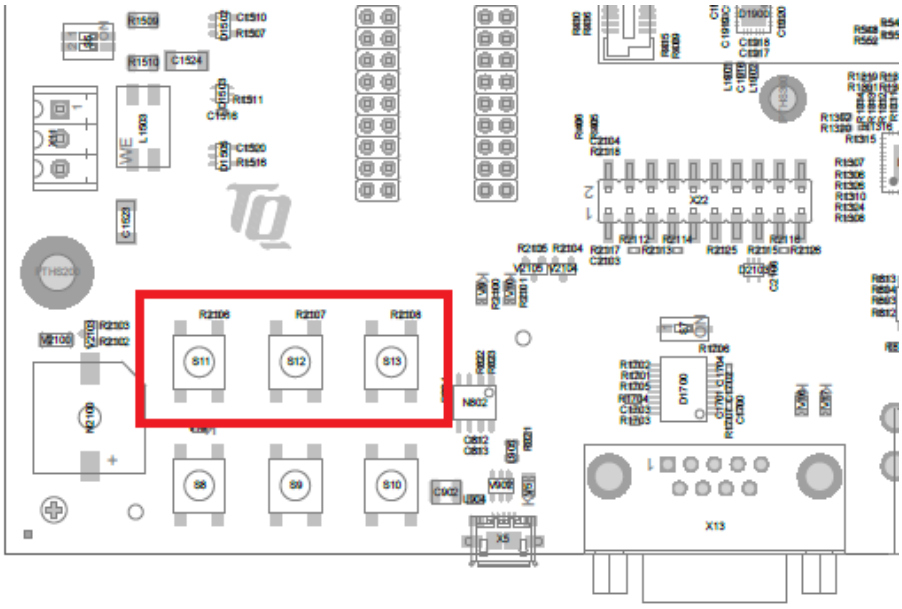

Figure 45: Position of navigations buttons – S11, S12, S13

4.3.3 Power-On (S10) and Reset (S8) button

For further information see chapter 4.1.6.

4.3.4 CAN (S5) and RS-485 (S6) termination

For further information see chapter 4.2.4 and 4.2.5.

4.3.5 Boot-Mode configuration

With the MBa7x all boot sources available for the TQMa7x can be used:

- eMMC
- QSPI Nor Flash
- SD card
- Serial Downloader via USB-OTG 1

Information about the boot configurations of the i.MX7 can be found in the TQMa7x User's Manual.

- ➢ A High level at BOOT_EN# decouples the DIP switches S[1:4] from the LCD interface.
- ➢ A Low level at BOOT_EN# connects the DIP switches S[1:4] to the LCD interface.

By default, BOOT_EN# is set to Low ⇨ the DIP switch circuit S[1:4] is connected to the LCD interface.

After the Boot Configuration is read out and the Boot Loader is started, the signals for the Boot Configuration BOOT_CFG[20:00] are used as parallel LCD signals, depending on the multiplexing.
To prevent the LCD signals from being affected by the DIP switch circuitry after the boot process, they can be separated from each other by IO buffers. The BOOT_EN# signal is available on a module GPIO for this purpose. After a reset, the buffers automatically connect the DIP switch circuit.

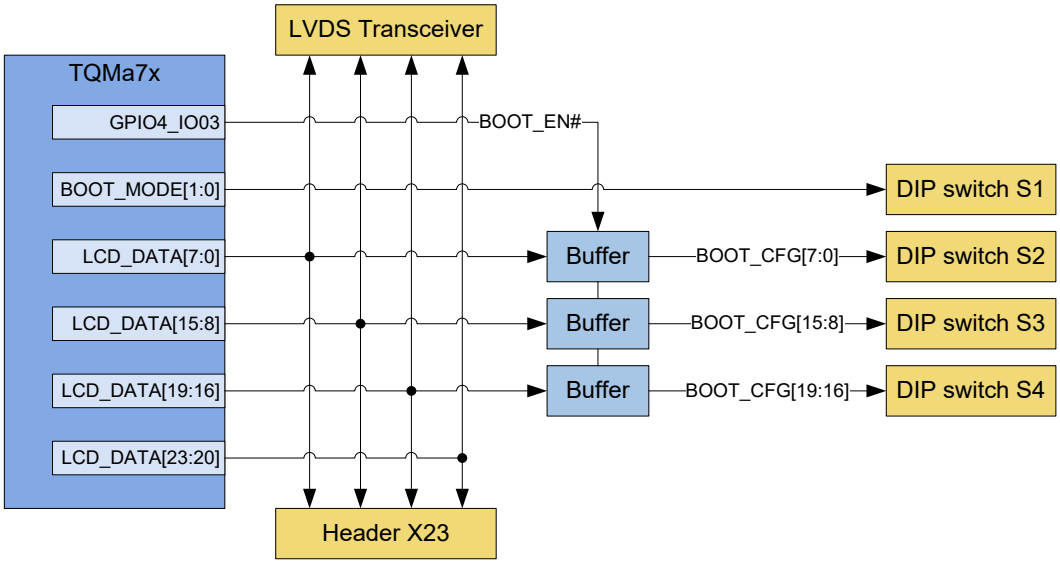

Figure 46: Block diagram Boot Mode DIP switches S1 to S4

Note:	LCD interface, stubs
	For EMC reasons and in order not to impair the signal quality, it is not recommended to connect the LCD interface to a pin header and an LVDS transceiver. On the MBa7x this was only implemented for functional Figure. In the final design, the LCD interface should be connected as short as possible and without stubs to only one type of display.

4.3.5 Boot-Mode configuration (continued)

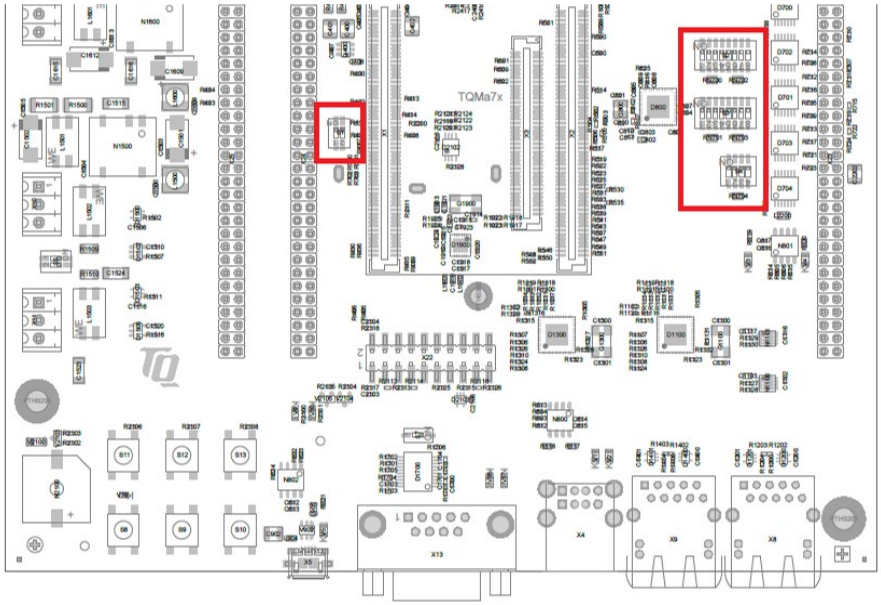

Figure 47: Position of Boot Mode DIP switches S1 to S4

The following tables describe the DIP switch settings for the different boot media.
Further settings like transfer modes and CPU clock can be found in the User's Manual of the TQMa7x (10).
Switch position 1 means ON, switch position 0 means OFF.

Table 66: Boot-Mode configuration – S1

Boot Mode	S1-1, BOOT_MODE1	S1-2, BOOT_MODE0
Boot from eFuses	0	0
Serial Downloader	0	1
Internal Boot	1	0
Reserved	1	1

4.3.5 Boot-Mode configuration (continued)

Table 67: Boot-Mode configuration DIP switches – S1, S2, S3, S4

DIP switch		Signal	eMMC	SD card	QSPI NOR	Serial Downloader
S1	1	BOOT_MODE1	1	1	1	0
	2	BOOT_MODE0	0	0	0	1
S2	1	BOOT_CFG0	X	X	X	X
	2	BOOT_CFG1	X	1	X	X
	3	BOOT_CFG2	0	0	X	X
	4	BOOT_CFG3	0	0	X	X
	5	BOOT_CFG4	0	1	0	X
	6	BOOT_CFG5	1	X	0	X
	7	BOOT_CFG6	0	X	0	X
	8	BOOT_CFG7	0	0	0	X
S3	1	BOOT_CFG8	X	0	0	X
	2	BOOT_CFG9	0	0	0	X
	3	BOOT_CFG10	0	0	0	X
	4	BOOT_CFG11	1	0	0	X
	5	BOOT_CFG12	0	1	0	X
	6	BOOT_CFG13	1	0	0	X
	7	BOOT_CFG14	0	0	1	X
	8	BOOT_CFG15	0	0	0	X
S4	1	BOOT_CFG16	0	0	0	X
	2	BOOT_CFG17	0	0	0	X
	3	BOOT_CFG18	0	0	0	X
	4	BOOT_CFG19	0	0	0	X

4.3.6 Buzzer

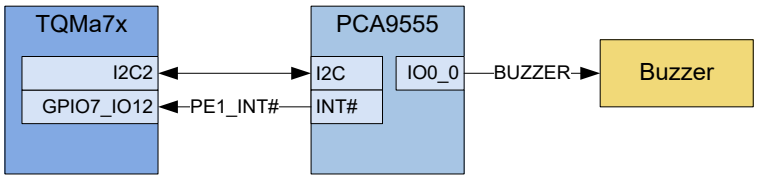

Figure 48: Block diagram buzzer

The MBa7x provides a buzzer. The buzzer is controlled via the PCA9555 port expander.
A high level of the BUZZER signal activates the buzzer.

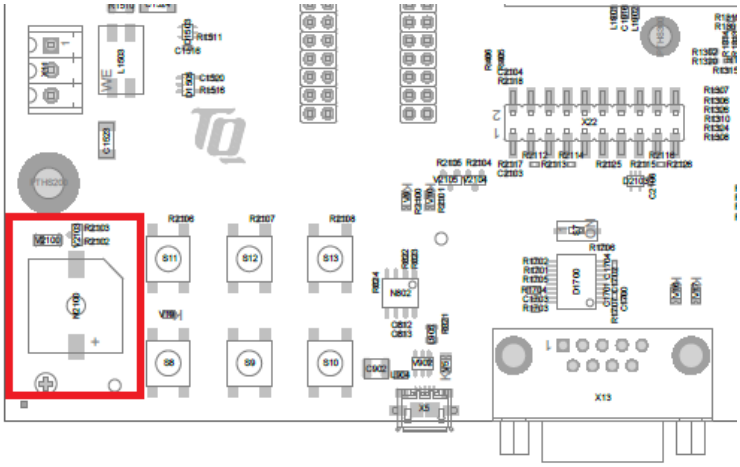

Figure 49: Position of buzzer – N2000

Table 68: Type of buzzer

Manufacturer / Number	Description
PUI Audio / SMI-1324-TW-5V-2-R	Buzzer, 5 V (typ.), 30 mA (max.)

4.3.7 JTAG

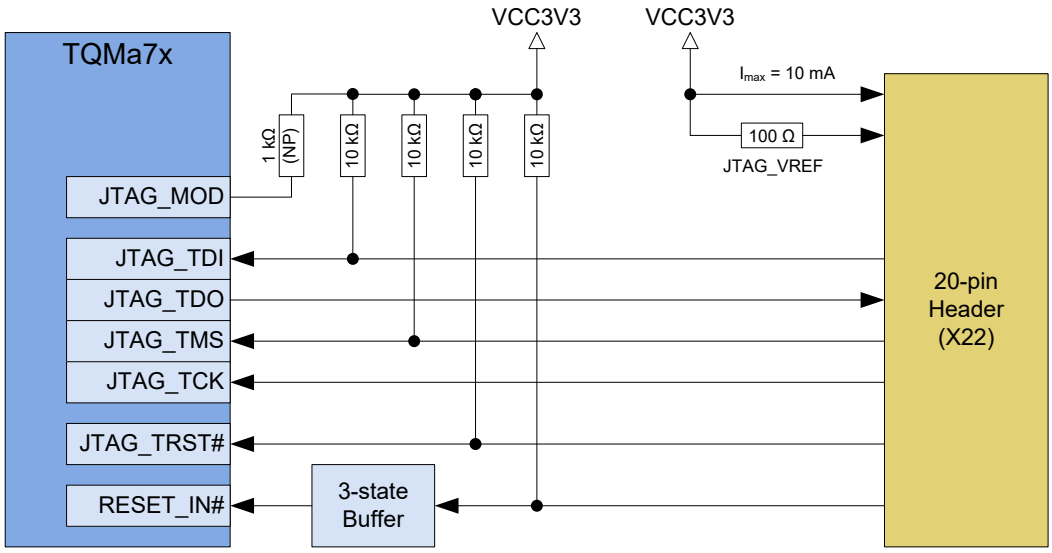

Figure 50: Block diagram JTAG

The JTAG interface is routed to a 20-pin header (X22). The pull-ups for the lines TDI, TMS, TRST# and SRST# are assembled on the MBa7x. All signal lines use 3.3 V as a reference. The JTAG interface has no ESD protection.
The JTAG mode can be configured by an assembly option. Information on this can be found in the current circuit diagram.

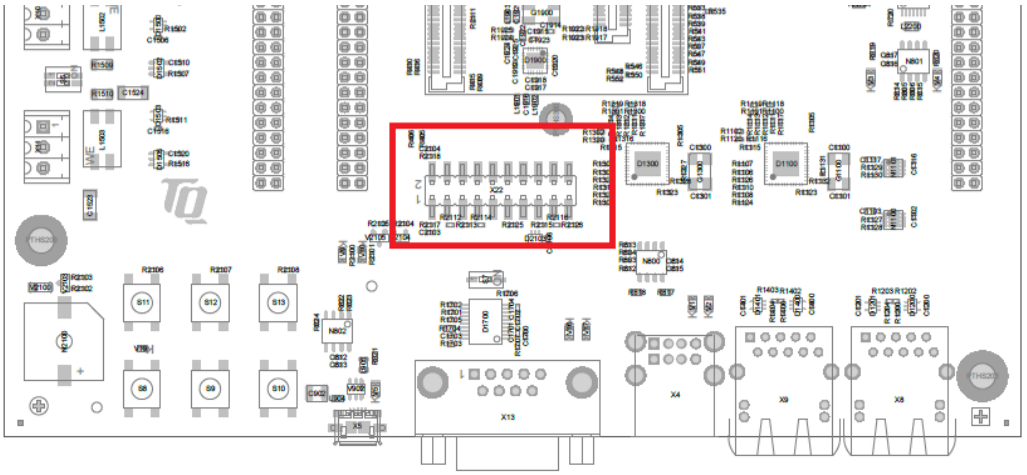

Figure 51: Position of JTAG – X22

Table 69: Type of JTAG connector

Manufacturer / Number	Description
Fischer Elektronik / SL-11-SMD-052-20-G-BTR	Header, 100 mil pitch, 2 × 10 pins

4.3.7 JTAG (continued)

The following table shows the pin assignment of the JTAG connector.

Table 70: Pinout JTAG – X22

Pin	Signal	Dir.	Remark
1	JTAG.VREF	P	100 Ω in series to VCC3V3, use only as reference
2	VCC3V3	P	0 Ω in series to VCC3V3, Imax = 10 mA
3	JTAG.TRST#	I	10 kΩ Pull-Up to VCC3V3
4	DGND	P	–
5	JTAG.TDI	I	10 kΩ Pull-Up to VCC3V3
6	DGND	P	–
7	JTAG.TMS	I	10 kΩ Pull-Up to VCC3V3
8	DGND	P	–
9	JTAG.TCK	I	–
10	DGND	P	–
11	DGND	P	10 kΩ to DGND
12	DGND	P	–
13	JTAG.TDO	O	–
14	DGND	P	–
15	JTAG.SRST#	I	10 kΩ Pull-Up to VCC3V3; open drain buffer at RESET_IN#
16	DGND	P	–
17	VCC3V3	P	10 kΩ Pull-Up to VCC3V3
18	DGND	P	–
19	DGND	P	10 kΩ to DGND
20	DGND	P	–

5. SOFTWARE

The software required for the HSIC hub can, depending on the configuration, be loaded by the TQMa7x software, see 4.2.1. Further software is not required for the MBa7x.

6. MECHANICS

6.1 Dimensions

The MBa7x has overall dimensions (length × width) of 170 × 170 mm².
The MBa7x has a maximum height of approximately 26.4 mm.
The MBa7x has six 4.3 mm holes for mounting in a housing and three 3.2 mm holes for mounting a heat sink.
The MBa7x weighs approximately 240 grams without TQMa7x.

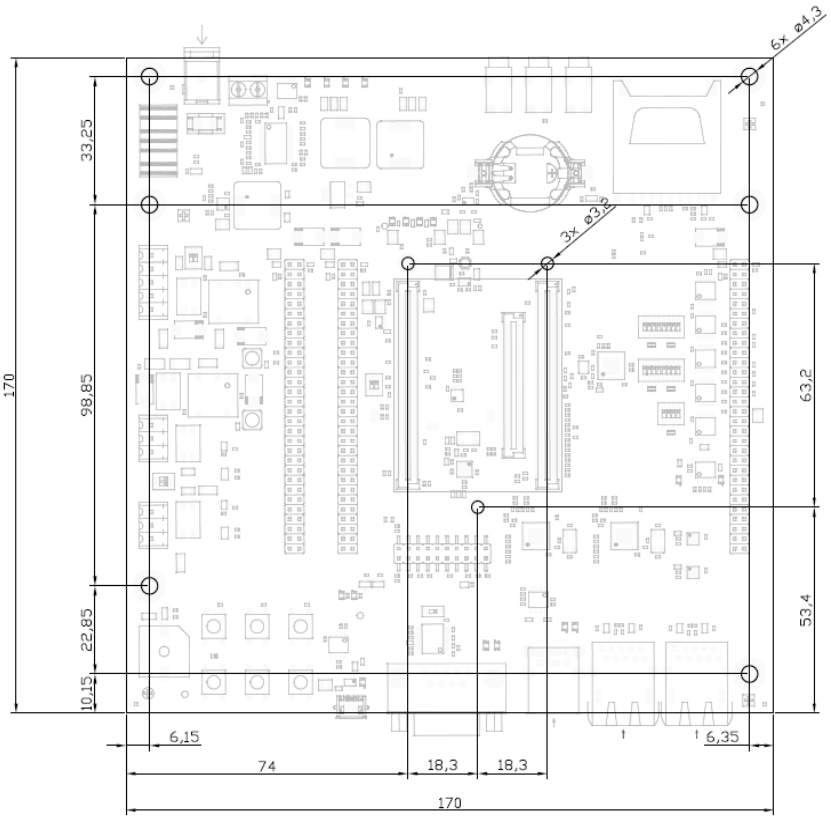

Figure 52: MBa7x dimensions

Note:	Component placement on carrier board
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa7x for the extraction tool MOZIa7x.

6.2 Thermal management

No special precautions were taken concerning the thermal management of the MBa7x.
At 100 % CPU load MBa7x and TQMa7x consume approx. 6.5 W.

Attention:	Destruction or malfunction, TQMa7x heat dissipation
	The i.MX7 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX7 must be taken into consideration when connecting the heat sink, see (1), and (2). The i.MX7 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa7x and thus malfunction, deterioration or destruction.

6.3 Assembly

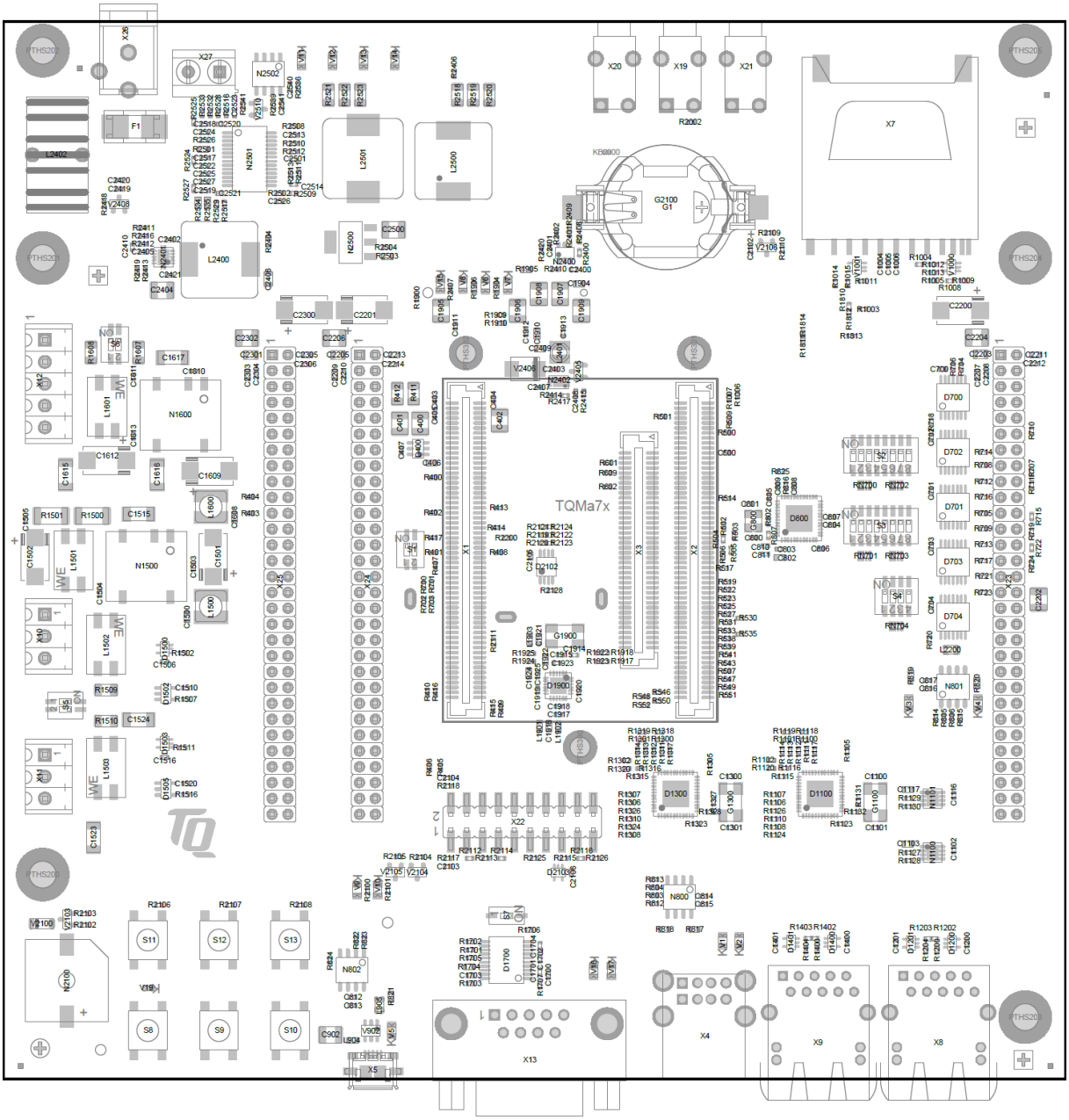

Figure 53: Component placement top

6.3 Assembly (continued)

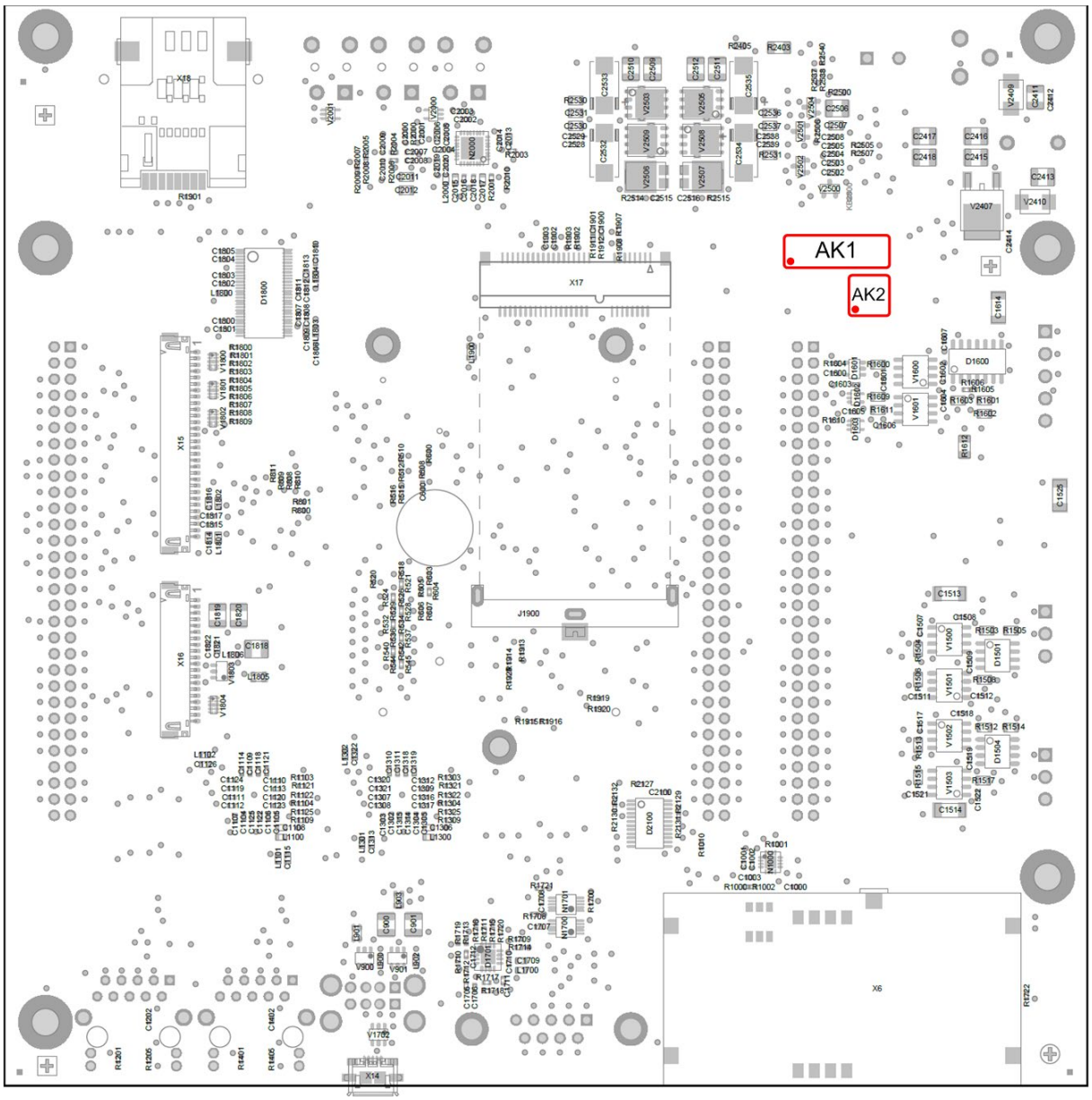

Figure 54: Component placement bottom

The labels on the MBa7x show the following information:

Table 71: Labels on MBa7x

Label	Text
AK1	MBa7x version, revision, tests performed
AK2	Serial number

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Because the MBa7x is a development platform, no EMC specific tests have been carried out.

Nevertheless DIN EN 55022:2010 class A was taken into account during development:

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.2 ESD

Most of the interfaces on the MBa7x are protected against electrostatic discharge. [12]
Interfaces providing an ESD protection are to be taken from the circuit diagram.

7.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety have not been carried out.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 72: Climatic and operational conditions MBa7x (without TQMa7x)

Parameter	Range	Remark
Ambient temperature	0 °C to +70 °C	Without Lithium battery CR2032
Ambient temperature	0 °C to +60 °C	With Lithium battery CR2032
Storage temperature	–10 °C to +60 °C	–
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

8.1 Protection against external effects

Protection class IP00 was defined for the MBa7x. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation was performed for the MBa7x.

The MBa7x is designed to be insensitive to vibration and impact.

High quality industrial grade connectors are assembled on the MBa7x.

12: The JTAG and PMIC interfaces do not provide ESD protection.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBa7x is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa7x was designed to be recyclable and easy to repair.

9.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

9.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000.
The MBa7x must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBa7x enable compliance with EuP requirements for the MBa7x.

9.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa7x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa7x is minimised by suitable measures. The MBa7x is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for the MBa7x. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa7x, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of the MBa7x is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 73: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ADR	Accord européen relatif au transport international des marchandises Dangereuses par Route
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CMC	Common Mode Choke
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrienorm)
DIP	Dual In-line Package
DSI	Display Serial Interface
ECSPI	Enhanced Capability Serial Peripheral Interface
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multi-Media Card
EN	European Norm
ENET	Ethernet
ESD	Electro-Static Discharge
EuP	Energy using Products
FFC	Flat Flex Cable
FIT	Failure In Time
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
HSIC	High-Speed Inter-Chip
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signal

10.1 Acronyms and definitions (continued)

Table 74: Further applicable documents (continued)

Acronym	Meaning
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MOZI	Module extractor (Modulzieher)
MTBF	Mean (operating) Time Between Failures
NA	Not Applicable
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SAI	Serial Audio Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
UART	Universal Asynchronous Receiver and Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UN	United Nations
USB	Universal Serial Bus
USDHC	Ultra-Secured Digital Host Controller
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

10.2 References

Table 74: Further applicable documents

No.	Document	Rev., Date	Company
(1)	i.MX 7Dual Family of Applications Processors Data Sheet, IMX7DCEC	2.0, 06/2016	NXP
(2)	i.MX 7Solo Family of Applications Processors Data Sheet, IMX7SCEC	2.0, 06/2016	NXP
(3)	i.MX7 Dual/Solo Product Lifetime Usage, AN5334	0, 09/2016	NXP
(4)	PF3000 PMIC	7.0, 09/2016	NXP
(5)	i.MX 7Dual Applications Processor Reference Manual, IMX7DRM	0.1, 08/2016	NXP
(6)	i.MX 7Solo Applications Processor Reference Manual, IMX7SRM	0.1, 08/2016	NXP
(7)	i.MX7S & i.MX7D, IMX7D_2N09P Mask Set Errata	0, 05/2016	NXP
(8)	i.MX 7DS Power Consumption Measurements, AN5383	0, 11/2016	NXP
(9)	Data Sheet USB4604, USB4604	1.1, 06.03.2014	Microchip
(10)	TQMa7x User's Manual	– current –	TQ-Systems
(11)	TQMa7x Support-Wiki	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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