MBa6x
User's Manual

MBa6x UM 0203
04.03.2024

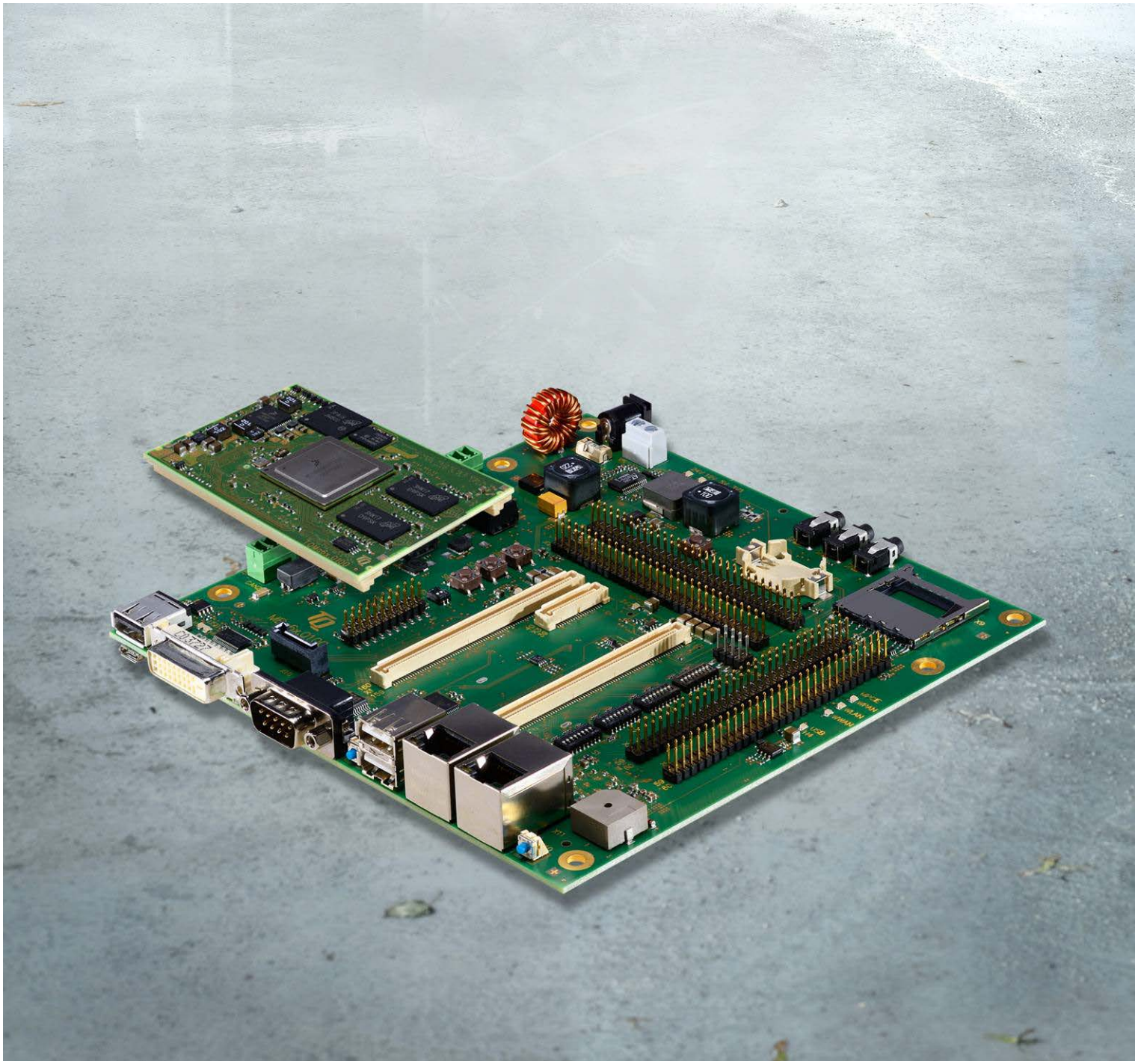

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	04.03.2015	Petz		First issue
0200	13.07.2016	Petz	All 1.4 2 4.1.1.2 Table 4 Table 10 8.3, 8.4 8.5, 8.7 Table 97	Freescale replaced with NXP, superfluous headlines removed FAX number updated “DualLite”-CPU added Typo in headline corrected Footnotes added Address of D2002 corrected Added Updated Updated and extended
0201	10.02.2018	Petz	All All 1.9, 2 Table 5 Table 4, Table 5, Table 6 4.1.4 4.1.7.2 Table 58 5.1, 7.2, 8.2	Typo, format and expression “VCC3V3_REFOUT” corrected to “VCC3V3_REF_OUT” Updated Function of signal al X2-26 corrected, “#” added at signal X2-67 Signal names corrected Table 12 and Table 13 added Added Signal names corrected Updated
0202	26.10.2018	Petz	All 7, 8	Links updated, formatting Updated
0203	03.04.2024	Petz	All Table 8 Tables 17, 21, 22, 23, 24, 25, 28, 34, 37, 40, 44, 50, 52, 53, 55, 57, 60, 67, 72, 75, 78, 81, 87, 88, 91, 92, 93, 95 1.9 3.1.7.1 Table 19 Table 24 4.1.7.3 Figure 59 Figure 60 Table 67	Non-functional changes, formatting, structure, links updated Tables 8, 9, 10 merged Removed Link to Yocto added “5 A slow blow” added Note on current supply Note on current supply Removed Updated Labels added Added

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa6x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa6x circuit diagram
- TQMa6x User's Manual
- IMX6DQRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa6x

2. BRIEF DESCRIPTION

This User's Manual describes the MBa6x revision ≥02xx. The MBa6x is designed as a carrier board for the TQMa6x.

All interfaces of the TQMa6x are available on the MBa6x. The characteristics of the i.MX6 CPU can be evaluated, and therefore the software development for a TQMa6x project can be started immediately.

The MBa6x supports all TQMa6x modules with Solo, DualLite, Dual or Quad i.MX6 CPU.

2.1 System architecture and functionality

2.1.1 MBa6x block diagram

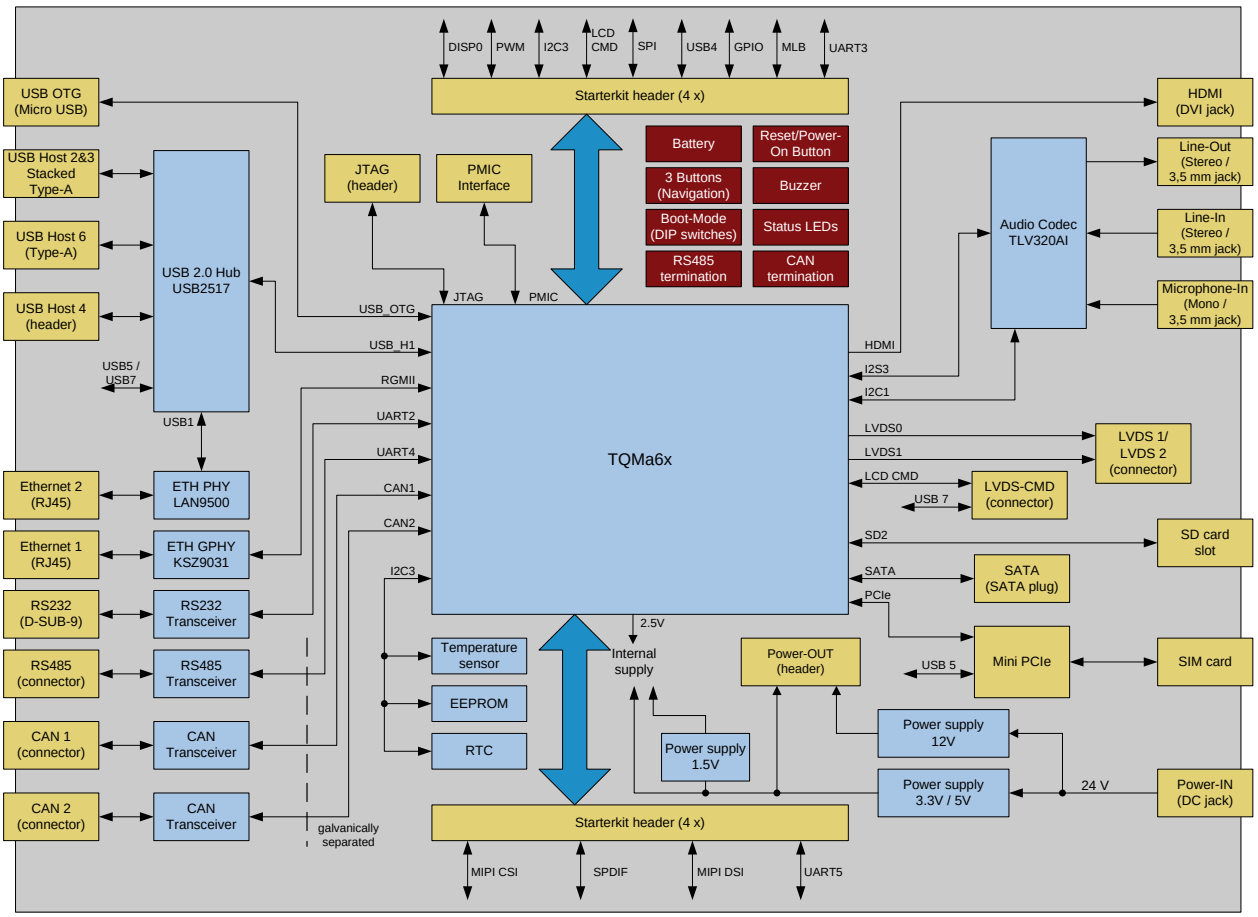


Figure 1: Block diagram MBa6x

2.1.2 Functionality

Core of the system is the TQMa6x with an NXP i.MX6 CPU. The TQMa6x connects all peripheral components to each other.
In addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, LVDS etc. all other available signals of the TQMa6x are routed to 100 mil standard headers.
The MBa6x provides the following interfaces and functions:

Table 2: Overview interfaces

Interface	Type of connector	Remark
USB 2.0 Hi-Speed host	USB receptacle Type A	Dual port receptacle, right angle
USB 2.0 Hi-Speed host	USB receptacle Type A	Single port receptacle, right angle
USB 2.0 Hi-Speed host	Header	–
USB 2.0 Hi-Speed OTG	USB receptacle type Micro AB	–
Ethernet 100BASE-T	RJ45 receptacle	Receptacle with integrated magnetics
Ethernet 1000BASE-T	RJ45 receptacle	Receptacle with integrated magnetics
CAN	Phoenix basic housing	Straight version, gal. separated
RS-485	Phoenix basic housing	Straight version, gal. separated
RS-232	D-Sub 9-pin connector	Right angle, Debug-UART
HDMI	DVI receptacle	–
LVDS	DF19 receptacle	LVDS data
LVDS-CMD	DF19 receptacle	LVDS control lines
Audio Out	Jack 3.5 mm	1 × Line-out (stereo) 1 × Line-in (stereo) 1 × Microphone (mono)
SD card	Push-Pull-Type	–
SATA	SATA connector	Straight version
PCIe	Mini PCIe	–
	SIM card holder	–
Headers	Header, 100 mil pitch	• DISP0 • PWM • I2C1, I2C3 • LCD-CMD • SPI1, SPI5 • USB4 • GPIOs • MLB • UART3, UART5 • SPDIF • MIPI CSI, MIPI DSI • 3.3 V / 2 A • 5 V / 2 A • 12 V / 3 A
Power In (V_{IN} = 24 V DC ±5 %)	DC jack (2.5 mm / 5.5 mm)	–
	DC jack 2-pin (screw terminals)	–
Battery holder	CR2032 holder	Backup battery RTC

Table 3: Overview diagnostic and user's interfaces

Interface	Component	Remark
Status-LEDs	16 × Chip LED	Power-LEDs, LEDs at GPIOs, …
Temperature sensor	1 × Temperature sensor	LM75A
Power / Reset buttons	3 × Push button	–
GP buttons	3 × Push button	General purpose push buttons
Boot-Mode configuration	32 + 2 DIP switch	–
CAN - and RS-485 termination	4 × DIP switch	–
Signal generator	1 × Buzzer	–
PMIC Diagnostic interface	1 × 8-pin	100 mil header
JTAG	1 × 20-pin	100 mil header

3. ELECTRONICS

3.1 MBa6x functional groups

3.1.1 TQMa6x

3.1.1.1 TQMa6x block diagram

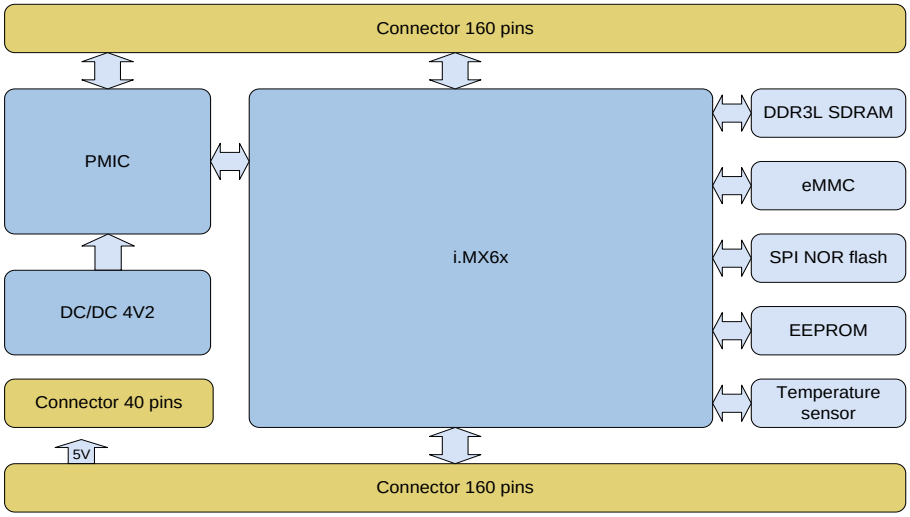


Figure 2: Block diagram TQMa6x

The TQMa6x with the i.MX6 CPU is the central system component. It provides DDR3-SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMa6x are derived from the supply voltage of 5 V. More information is to be taken from the accompanying User's Manual of the TQMa6x.

The boot behaviour of the TQMa6x can be customised. The required boot-mode configuration can be set with DIP switches, see chapter 3.3.5.

3.1.1.2 TQMa6x pinout

The available signals are routed via three connectors onto the MBa6x.

The pins assignment in Table 4 to Table 6 refers to the corresponding BSP provided by TQ-Systems.

3.1.1.2 TQMa6x pinout (continued)

Table 4: TQMa6x connector X1

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	5 V	POWER	VCC5V	1	2	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	3	4	VCC5V	POWER	5 V	P	–
–	P	5 V	POWER	VCC5V	5	6	VCC5V	POWER	5 V	P	–
–	P	0 V	POWER	DGND	7	8	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	9	10	DGND	POWER	0 V	P	–
–	P	0 V	POWER	DGND	11	12	DGND	POWER	0 V	P	–
A18	I/O	3.3 V	GPIO	GPIO2_IO00	13	14	PCIE_TX_N	PCIE	– [1]	O	A03
C17	I/O	3.3 V	GPIO	GPIO2_IO01	15	16	PCIE_TX_P	PCIE	– 1	O	B03
F16	I/O	3.3 V	GPIO	GPIO2_IO02	17	18	DGND	POWER	0 V	P	–
D17	I/O	3.3 V	GPIO	GPIO2_IO03	19	20	PCIE_RX_N	PCIE	– 1	I	B01
D18	I/O	3.3 V	GPIO	GPIO2_IO08	21	22	PCIE_RX_P	PCIE	– 1	I	B02
A20	I/O	3.3 V	GPIO	GPIO2_IO11	23	24	DGND	POWER	0 V	P	–
C15	I/O	3.3 V	GPIO	GPIO6_IO07	25	26	CLK1_N	XTAL	2.5 V	O	C07
A16	I/O	3.3 V	GPIO	GPIO6_IO08	27	28	CLK1_P	XTAL	2.5 V	O	D07
F15	I/O	3.3 V	GPIO	GPIO6_IO11	29	30	DGND	POWER	0 V	P	–
C16	I/O	3.3 V	GPIO	GPIO6_IO14	31	32	USB_H1_DP	USB	– [2]	I/O	E10
B19	O	3.3 V	PWM	PWM3	33	34	USB_H1_DN	USB	– 2	I/O	F10
–	P	0 V	POWER	DGND	35	36	DGND	POWER	0 V	P	–
D10	P	5 V	POWER	USB_H1_VBUS	37	38	HDMI_CLK_N	HDMI	– [3]	O	J05
T05	O	3.3 V	USB	USB_H1_PWR	39	40	HDMI_CLK_P	HDMI	– 3	O	J06
R07	I	3.3 V	USB	USB_H1_OC	41	42	DGND	POWER	0 V	P	–
E09	P	5 V	POWER	USB_OTG_VBUS	43	44	HDMI_D0_N	HDMI	– 3	O	K05
T04	I	3.3 V	USB	USB_OTG_ID	45	46	HDMI_D0_P	HDMI	– 3	O	K06
–	P	0 V	POWER	DGND	47	48	DGND	POWER	0 V	P	–
A06	I/O	– 2	USB	USB_OTG_DP	49	50	HDMI_D1_N	HDMI	– 3	O	J03
B06	I/O	– 2	USB	USB_OTG_DN	51	52	HDMI_D1_P	HDMI	– 3	O	J04
–	P	0 V	POWER	DGND	53	54	DGND	POWER	0 V	P	–
A14	I	– [4]	SATA	SATA_RX_N	55	56	HDMI_D2_N	HDMI	– 3	O	K03
B14	I	– 4	SATA	SATA_RX_P	57	58	HDMI_D2_P	HDMI	– 3	O	K04
–	P	0 V	POWER	DGND	59	60	DGND	POWER	0 V	P	–
B12	O	– 4	SATA	SATA_TX_N	61	62	HDMI_DDC_SCL	HDMI	– 3	O	U05
A12	O	– 4	SATA	SATA_TX_P	63	64	HDMI_DDC_SDA	HDMI	– 3	I/O	T07
–	P	0 V	POWER	DGND	65	66	HDMI_HPD	HDMI	– 3	I	K01
C02	I	3.3 V	JTAG	JTAG_TRST#	67	68	BOOT.MODE0	CONFIG	3.0 V [5]	I	C12
C03	I	3.3 V	JTAG	JTAG_TMS	69	70	BOOT.MODE1	CONFIG	3.0 V 5	I	F12
G05	I	3.3 V	JTAG	JTAG_TDI	71	72	GPIO7_IO12	GPIO	3.3 V	I/O	R01
G06	O	3.3 V	JTAG	JTAG_TDO	73	74	GPIO4_IO06	GPIO	3.3 V	I/O	W05
H06	I_{PD}	3.3 V	JTAG	JTAG_MOD	75	76	VSNVS_REF_OUT	POWER	3.0 V	P	–
H05	I	3.3 V	JTAG	JTAG_TCK	77	78	CCM_CLKO1	CLKO	3.3 V	O	P04
–	P	0 V	POWER	DGND	79	80	DGND	POWER	0 V	P	–

1: See PCIe 1.1/2.0 Specification.
2: See USB 2.0 Specification.
3: See HDMI 1.4 Specification.
4: See Serial ATA 3.0 Specification.
5: Use VSNVS_REF_OUT only as reference voltage.

3.1.1.2 TQMa6x pinout (continued)

Table 4: TQMa6x connector X1 (continued)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
L01	I	3.3 V	UART	UART4_RX	81	82	GPIO5_IO18	GPIO	3.3 V	I/O	P01
M02	O	3.3 V	UART	UART4_TX	83	84	GPIO5_IO21	GPIO	3.3 V	I/O	N02
L04	I	3.3 V	UART	UART4_RTS#	85	86	I2C3_SCL	I2C	3.3 V	O_{PU}	R04
L03	O	3.3 V	UART	UART4_CTS#	87	88	I2C3_SDA	I2C	3.3 V	I/O_{PU}	T03
M05	I	3.3 V	UART	UART5_RX	89	90	CAN2_RX	CAN	3.3 V	I	V05
M04	O	3.3 V	UART	UART5_TX	91	92	CAN2_TX	CAN	3.3 V	O	T06
M06	I	3.3 V	UART	UART5_RTS#	93	94	CAN1_RX	CAN	3.3 V	I	W04
L06	O	3.3 V	UART	UART5_CTS#	95	96	CAN1_TX	CAN	3.3 V	O	W06
–	P	0 V	POWER	DGND	97	98	DGND	POWER	0 V	P	–
M01	I	3.3 V	AUDIO	AUD3_RXC	99	100	AUD3_TXC	AUDIO	3.3 V	O	N01
M03	I	3.3 V	AUDIO	AUD3_RXFS	101	102	AUD3_TXFS	AUDIO	3.3 V	O	N04
N03	I	3.3 V	AUDIO	AUD3_RXD	103	104	AUD3_TXD	AUDIO	3.3 V	O	P02
F17	O	3.3 V	PWM	PWM4	105	106	GPIO1_IO21	GPIO	3.3 V	I/O	F18
N05	O	3.3 V	I2C	I2C1_SCL	107	108	SPI5_MISO	SPI	3.3 V	I	A21
N06	I/O	3.3 V	I2C	I2C1_SDA	109	110	SPI5_MOSI	SPI	3.3 V	O	B21
P03	I/O	3.3 V	GPIO	GPIO5_IO20	111	112	SPI5_SS0#	SPI	3.3 V	O	C20
P05	I/O	3.3 V	GPIO	GPIO4_IO05	113	114	SPI5_SCK	SPI	3.3 V	O	D20
–	P	0 V	POWER	DGND	115	116	DGND	POWER	0 V	P	–
Y01	O	– [6]	LVDS	LVDS1_TX0_N	117	118	LVDS0_TX0_N	LVDS	– 6	O	U02
Y02	O	– 6	LVDS	LVDS1_TX0_P	119	120	LVDS0_TX0_P	LVDS	– 6	O	U01
–	P	0 V	POWER	DGND	121	122	DGND	POWER	0 V	P	–
AA02	O	– 6	LVDS	LVDS1_TX1_N	123	124	LVDS0_TX1_N	LVDS	– 6	O	U04
AA01	O	– 6	LVDS	LVDS1_TX1_P	125	126	LVDS0_TX1_P	LVDS	– 6	O	U03
–	P	0 V	POWER	DGND	127	128	DGND	POWER	0 V	P	–
AB01	O	– 6	LVDS	LVDS1_TX2_N	129	130	LVDS0_TX2_N	LVDS	– 6	O	V02
AB02	O	– 6	LVDS	LVDS1_TX2_P	131	132	LVDS0_TX2_P	LVDS	– 6	O	V01
–	P	0 V	POWER	DGND	133	134	DGND	POWER	0 V	P	–
Y03	O	– 6	LVDS	LVDS1_CLK_N	135	136	LVDS0_CLK_N	LVDS	– 6	O	V04
Y04	O	– 6	LVDS	LVDS1_CLK_P	137	138	LVDS0_CLK_P	LVDS	– 6	O	V03
–	P	0 V	POWER	DGND	139	140	DGND	POWER	0 V	P	–
AA03	O	– 6	LVDS	LVDS1_TX3_N	141	142	LVDS0_TX3_N	LVDS	– 6	O	W02
AA04	O	– 6	LVDS	LVDS1_TX3_P	143	144	LVDS0_TX3_P	LVDS	– 6	O	W01
–	P	0 V	POWER	DGND	145	146	DGND	POWER	0 V	P	–
T02	O	3.3 V	PWM	PWM1	147	148	GPIO7_IO13	GPIO	3.3 V	I/O	P06
U20	I/O	ENET [7]	GPIO	GPIO1_IO30	149	150	GPIO7_IO11	GPIO	3.3 V	I/O	R02
W20	I/O	ENET 7	GPIO	GPIO1_IO29	151	152	GPIO1_IO07	GPIO	3.3 V	I/O	R03
V21	I/O	ENET 7	GPIO	GPIO1_IO28	153	154	GPIO1_IO26	GPIO	ENET 7	I/O	W22
U21	I/O	ENET 7	GPIO	GPIO1_IO25	155	156	SPDIF_OUT	AUDIO	ENET 7	O	W21
R05	I/O	3.3 V	GPIO	GPIO1_IO08	157	158	SPDIF_IN	AUDIO	ENET 7	I	W23
–	P	0 V	POWER	DGND	159	160	DGND	POWER	0 V	P	–

6: See LVDS Specification (ANSI EIA-644-A).
7: 2.5 V if NVCC_ENET_IN is connected to VCC2V5_RGMII_OUT. 3.3 V if NVCC_ENET_IN is connected to VCC3V3_REF_OUT.

3.1.1.2 TQMa6x pinout (continued)

Table 5: TQMa6x connector X2

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	POWER	DGND	1	2	DGND	POWER	0 V	P	–
A22	I/O	3.3 V	SD	SD2_DAT0	3	4	SD2_DAT1	SD	3.3 V	I/O	E20
A23	I/O	3.3 V	SD	SD2_DAT2	5	6	SD2_DAT3	SD	3.3 V	I/O	B22
A19	I/O	3.3 V	SD	SD2_DAT4	7	8	SD2_DAT5	SD	3.3 V	I/O	B18
E17	I/O	3.3 V	SD	SD2_DAT6	9	10	SD2_DAT7	SD	3.3 V	I/O	C18
T01	I	3.3 V	SD	SD2_WP	11	12	SD2_CMD	SD	3.3 V	I/O	F19
C21	O	3.3 V	SD	SD2_CLK	13	14	SD2_CD#	SD	3.3 V	I	R06
–	P	0 V	POWER	DGND	15	16	DGND	POWER	0 V	P	–
–	P	3.3 V	POWER	LICELL	17	18	VCC8V25_OTP	CONFIG	8.25 V	P	–
–	I_{PU}	3.3 V	CONFIG	PMIC_PWRON	19	20	VCC3V3_OTP	CONFIG	3.3 V	P	–
D12	I_{PU}	3.3 V	CONFIG	MX6_ONOFF	21	22	OTP_SCL	CONFIG	3.3 V	I	–
C11	I_{PU}	3.3 V	CONFIG	MX6_POR#	23	24	OTP_SDA	CONFIG	3.3 V	I/O	–
–	O_{OD}	3.3 V	CONFIG	RESET_OUT#	25	26	VCC3V3MB_EN	POWER	3.3 V	P	–
E18	I	3.3 V	UART	UART2_RX	27	28	UART2_RTS#	UART	3.3 V	I	C19
D19	O	3.3 V	UART	UART2_TX	29	30	UART2_CTS#	UART	3.3 V	O	B20
–	P	0 V	POWER	DGND	31	32	DGND	POWER	0 V	P	–
B25	I	2.5 V	RGMII	RGMII_RXC	33	34	RGMII_TXC	RGMII	2.5 V	O	D21
–	P	0 V	POWER	DGND	35	36	DGND	POWER	0 V	P	–
C24	I	2.5 V	RGMII	RGMII_RD0	37	38	RGMII_TD0	RGMII	2.5 V	O	C22
B23	I	2.5 V	RGMII	RGMII_RD1	39	40	RGMII_TD1	RGMII	2.5 V	O	F20
B24	I	2.5 V	RGMII	RGMII_RD2	41	42	RGMII_TD2	RGMII	2.5 V	O	E21
D23	I	2.5 V	RGMII	RGMII_RD3	43	44	RGMII_TD3	RGMII	2.5 V	O	A24
D22	I	2.5 V	RGMII	RGMII_RX_CTL	45	46	RGMII_TX_CTL	RGMII	2.5 V	O	C23
–	P	0 V	POWER	DGND	47	48	DGND	POWER	0 V	P	–
V20	O	ENET [8]	MII	ENET_MDC	49	50	ENET_REFCLK	RGMII	ENET 8	I	V22
V23	I/O	ENET 8	MII	ENET_MDIO	51	52	DGND	POWER	0 V	P	–
R19	P	ENET 8	POWER	NVCC_ENET_IN	53	54	VCC2V5_RGMII_OUT	POWER	2.5 V	P	–
V06	I/O	3.3 V	GPIO	GPIO4_IO07	55	56	VCC3V3_REF_OUT	POWER	3.3 V	P	–
U07	I/O	3.3 V	GPIO	GPIO4_IO08	57	58	GPIO4_IO09	GPIO	3.3 V	I/O	U06
E16	I	3.3 V	UART	UART3_RX	59	60	WDOG1#	WDOG	3.3 V	O	E19
B17	O	3.3 V	UART	UART3_TX	61	62	DGND	POWER	0 V	P	–
F21	I	3.3 V	SPI	SPI1_MISO	63	64	SPI1_SCK	SPI	3.3 V	O	C25
G21	O	3.3 V	SPI	(SPI1_SS1#)/DNC	65	66	SPI1_MOSI	SPI	3.3 V	O	D24
H20	I	3.3 V	USB	USB_OTG_OC#	67	68	GPIO3_IO20	GPIO	3.3 V	I/O	G20
D25	I/O	3.3 V	GPIO	GPIO3_IO23	69	70	USB_OTG_PWR	USB	3.3 V	O	E23
G22	O	3.3 V	SPI	SPI1_SS3#	71	72	SPI1_SS2#	SPI	3.3 V	O	F22
–	P	0 V	POWER	DGND	73	74	DGND	POWER	0 V	P	–
E25	I/O	3.3 V	GPIO	GPIO3_IO27	75	76	GPIO3_IO26	GPIO	3.3 V	I/O	E24
J19	I/O	3.3 V	GPIO	GPIO3_IO29	77	78	GPIO3_IO28	GPIO	3.3 V	I/O	G23
H21	I	3.3 V	UART	UART3_RTS#	79	80	UART3_CTS#	UART	3.3 V	O	J20

8: 2.5 V, if NVCC_ENET_IN is connected to VCC2V5_RGMII_OUT. 3.3 V, if NVCC_ENET_IN is connected to VCC3V3_REF_OUT.

3.1.1.2 TQMa6x pinout (continued)

Table 5: TQMa6x connector X2 (continued)

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
J24	I/O	3.3 V	GPIO	GPIO2_IO25	81	82	CCM_CLKO2	CCM	3.3 V	O	A17
J23	I/O	3.3 V	GPIO	GPIO2_IO24	83	84	GPIO2_IO23	GPIO	3.3 V	I/O	H24
F23	I	3.3 V	BOOT	BOOT_CFG4_7	85	86	BOOT_CFG4_6	BOOT	3.3 V	I	E22
–	P	0 V	POWER	DGND	87	88	DGND	POWER	0 V	P	–
K20	I	3.3 V	BOOT	BOOT_CFG4_5	89	90	BOOT_CFG4_4	BOOT	3.3 V	I	K23
K21	I	3.3 V	BOOT	BOOT_CFG4_3	91	92	BOOT_CFG4_2	BOOT	3.3 V	I	K22
M25	I	3.3 V	BOOT	BOOT_CFG4_1	93	94	GPIO6_IO16	GPIO	3.3 V	I/O	D16
H19	I/O	3.3 V	HDMI	HDMI_CEC_LINE	95	96	BOOT_CFG4_0	BOOT	3.3 V	I	F25
J21	I	3.3 V	BOOT	BOOT_CFG3_7	97	98	BOOT_CFG3_6	BOOT	3.3 V	I	F24
H23	I	3.3 V	BOOT	BOOT_CFG3_5	99	100	BOOT_CFG3_4	BOOT	3.3 V	I	H22
G25	I	3.3 V	BOOT	BOOT_CFG3_3	101	102	BOOT_CFG3_2	BOOT	3.3 V	I	J22
G24	I	3.3 V	BOOT	BOOT_CFG3_1	103	104	BOOT_CFG3_0	BOOT	3.3 V	I	H25
–	P	0 V	POWER	DGND	105	106	DGND	POWER	0 V	P	–
N24	I	3.3 V	BOOT	BOOT_CFG2_7	107	108	BOOT_CFG2_6	BOOT	3.3 V	I	N23
M23	I	3.3 V	BOOT	BOOT_CFG2_5	109	110	BOOT_CFG2_4	BOOT	3.3 V	I	M24
M20	I	3.3 V	BOOT	BOOT_CFG2_3	111	112	BOOT_CFG2_2	BOOT	3.3 V	I	M22
M21	I	3.3 V	BOOT	BOOT_CFG2_1	113	114	BOOT_CFG2_0	BOOT	3.3 V	I	L24
L25	I	3.3 V	BOOT	BOOT_CFG1_7	115	116	BOOT_CFG1_6	BOOT	3.3 V	I	K25
L23	I	3.3 V	BOOT	BOOT_CFG1_5	117	118	BOOT_CFG1_4	BOOT	3.3 V	I	L22
K24	I	3.3 V	BOOT	BOOT_CFG1_3	119	120	BOOT_CFG1_2	BOOT	3.3 V	I	L21
J25	I	3.3 V	BOOT	BOOT_CFG1_1	121	122	BOOT_CFG1_0	BOOT	3.3 V	I	L20
–	P	0 V	POWER	DGND	123	124	DGND	POWER	0 V	P	–
N19	O	3.3 V	DISP	DISP0_CLK	125	126	GPIO6_IO31	GPIO	3.3 V	I/O	N22
N21	O	3.3 V	DISP	DISP0_DRDY	127	128	DISP0_HSYNC	DISP	3.3 V	O	N25
P25	O	3.3 V	DISP	DISP0_CONTRAST	129	130	DISP0_VSYNC	DISP	3.3 V	O	N20
–	P	0 V	POWER	DGND	131	132	DGND	POWER	0 V	P	–
P24	O	3.3 V	DISP	DISP0_DAT0	133	134	DISP0_DAT1	DISP	3.3 V	O	P22
P23	O	3.3 V	DISP	DISP0_DAT2	135	136	DISP0_DAT3	DISP	3.3 V	O	P21
P20	O	3.3 V	DISP	DISP0_DAT4	137	138	DISP0_DAT5	DISP	3.3 V	O	R25
R23	O	3.3 V	DISP	DISP0_DAT6	139	140	DISP0_DAT7	DISP	3.3 V	O	R24
R22	O	3.3 V	DISP	DISP0_DAT8	141	142	DISP0_DAT9	DISP	3.3 V	O	T25
R21	O	3.3 V	DISP	DISP0_DAT10	143	144	DISP0_DAT11	DISP	3.3 V	O	T23
–	P	0 V	POWER	DGND	145	146	DGND	POWER	0 V	P	–
T24	O	3.3 V	DISP	DISP0_DAT12	147	148	DISP0_DAT13	DISP	3.3 V	O	R20
U25	O	3.3 V	DISP	DISP0_DAT14	149	150	DISP0_DAT15	DISP	3.3 V	O	T22
T21	O	3.3 V	DISP	DISP0_DAT16	151	152	DISP0_DAT17	DISP	3.3 V	O	U24
V25	O	3.3 V	DISP	DISP0_DAT18	153	154	DISP0_DAT19	DISP	3.3 V	O	U23
U22	O	3.3 V	DISP	DISP0_DAT20	155	156	DISP0_DAT21	DISP	3.3 V	O	T20
V24	O	3.3 V	DISP	DISP0_DAT22	157	158	DISP0_DAT23	DISP	3.3 V	O	W24
–	P	0 V	POWER	DGND	159	160	DGND	POWER	0 V	P	–

3.1.1.2 TQMa6x pinout (continued)

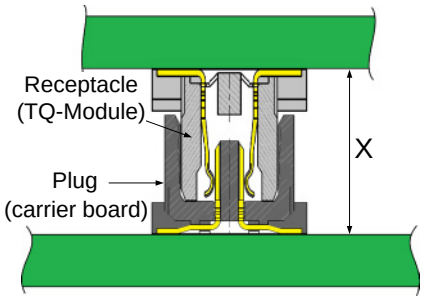
Table 6: TQMa6x connector X3

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	0 V	POWER	DGND	1	2	DGND	POWER	0 V	P	–
F04	I	– [9]	MIPI-CSI	CSI_CLK0_N	3	4	MLB_CLK_N	MLB	– 9	O	A11
F03	I	– 9	MIPI-CSI	CSI_CLK0_P	5	6	MLB_CLK_P	MLB	– 9	O	B11
–	P	0 V	POWER	DGND	7	8	DGND	POWER	0 V	P	–
E04	I	– 9	MIPI-CSI	CSI_D0_N	9	10	MLB_D_N	MLB	– 9	I/O	B10
E03	I	– 9	MIPI-CSI	CSI_D0_P	11	12	MLB_D_P	MLB	– 9	I/O	A10
–	P	0 V	POWER	DGND	13	14	DGND	POWER	0 V	P	–
D01	I	– 9	MIPI-CSI	CSI_D1_N	15	16	MLB_S_N	MLB	– 9	I/O	A09
D02	I	– 9	MIPI-CSI	CSI_D1_P	17	18	MLB_S_P	MLB	– 9	I/O	B09
–	P	0 V	POWER	DGND	19	20	DGND	POWER	0 V	P	–
E01	I	– 9	MIPI-CSI	CSI_D2_N	21	22	DSI_CLK0_N	MIPI-DSI	– 9	O	H03
E02	I	– 9	MIPI-CSI	CSI_D2_P	23	24	DSI_CLK0_P	MIPI-DSI	– 9	O	H04
–	P	0 V	POWER	DGND	25	26	DGND	POWER	0 V	P	–
F02	I	– 9	MIPI-CSI	CSI_D3_N	27	28	DSI_D0_N	MIPI-DSI	– 9	O	G02
F01	I	– 9	MIPI-CSI	CSI_D3_P	29	30	DSI_D0_P	MIPI-DSI	– 9	O	G01
–	P	0 V	POWER	DGND	31	32	DGND	POWER	0 V	P	–
C05	O	2.5 V	XTAL	CLK2_N	33	34	DSI_D1_N	MIPI-DSI	– 9	I	H02
D05	O	2.5 V	XTAL	CLK2_P	35	36	DSI_D1_P	MIPI-DSI	– 9	I	H01
–	P	0 V	POWER	DGND	37	38	DGND	POWER	0 V	P	–
E11	I	3.0 V [10]	CONFIG	TAMPER	39	40	SPI-NOR_WP#	CONFIG	3.3 V	I	–

3.1.1.3 TQMa6x mating connectors

The connectors used on the MBa6x are listed in Table 7.
If a different board-to-board distance is required, higher connectors can be used. Suitable types are to be taken from Table 7.

Table 7: Carrier board mating connectors

Manufacturer	Pin count / Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 160-pin: 5177986-8	On MBa6x	5 mm	
	40-pin: 1-5177986-1 160-pin: 2-5179230-8	–	6 mm	
	40-pin: 2-5177986-1 160-pin: 5179030-8	–	7 mm	
	40-pin: 3-5177986-1 160-pin: 3-5177986-8	–	8 mm	

Attention:	TQMa6x interfaces
	Depending on the selected TQMa6x, not all interfaces are available. Available interfaces are to be taken from the pinout table in the TQMa6x User's Manual.

9: See i.MX6 Reference Manuals (1), (2).
10: Use VSNVS_REF_OUT only as reference voltage.

3.1.2 I²C address mapping

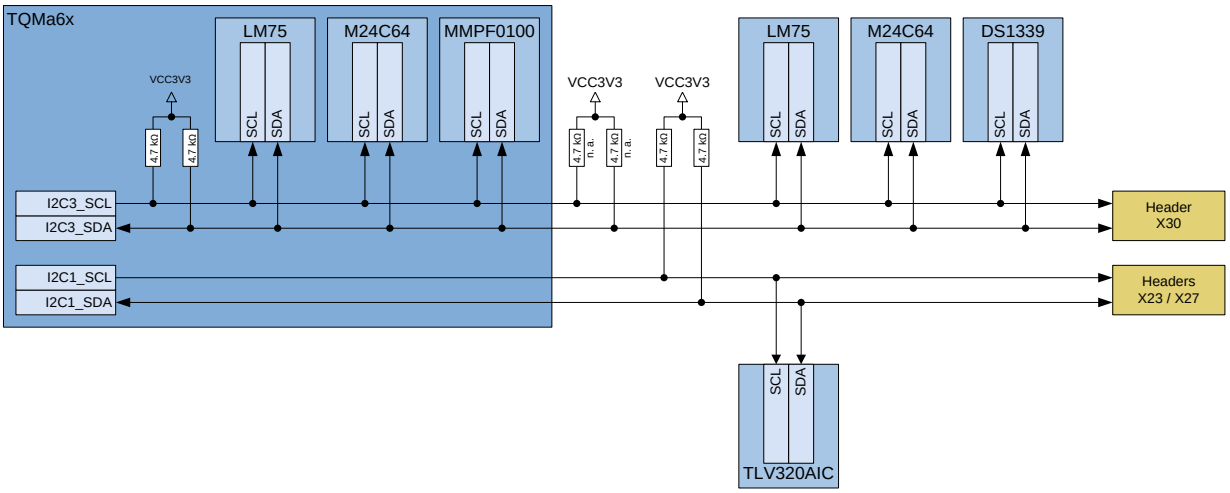


Figure 3: Block diagram I²C bus

I2C1 and I2C3 are used on the Starterkit.
A temperature sensor, an EEPROM and an RTC can be addressed using I2C3.
The audio-codec is connected to I2C1. Table 8 shows the device addresses used.
Both interfaces are also available on headers.

Table 8: I²C address mapping

I²C bus	Device	Ref. ID	Location	7-bit address
I2C1	Audio Codec (TLV320AIC)	N1800	MBa6x	0x18 / 001 1000b
I2C3	Temperature sensor (LM75A)	D2000		0x49 / 100 1001b
	EEPROM (M24C64)	D2002		0x57 / 101 0111b
	RTC (DS1339)	D2003		0x68 / 110 1000b
	Temperature sensor (LM75A)	–	TQMa6x	0x48 / 100 1000b
	EEPROM (M24C64)	–		0x50 / 101 0000b
	PMIC (MMPF0100)	–		0x08 / 000 1000b

Attention:	I2C3 bus
	Attention when using I2C3. Since the PMIC can be addressed on I2C3, errors on the bus can lead to instabilities of the TQMa6x!

3.1.3 Temperature sensor

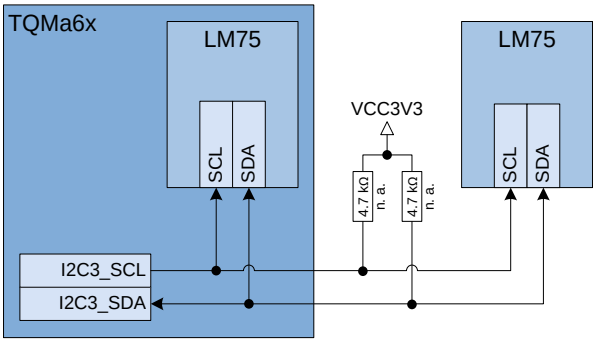


Figure 4: Block diagram temperature sensor

An LM75A sensor is available on the TQMa6x and on the MBa6x, to monitor the temperature.
Both sensors are connected via I2C3 and have an individual device address.
The address of the sensor on the MBa6x can be changed by reassembling some resistors.
If the address is changed, attention has to be paid that no address conflicts with already existing I²C device occur.

Table 9: Electrical characteristics LM75A

Manufacturer	Resolution	Accuracy	Temperature range	Error
NXP	0.125 °C	11 bit	–25 °C to +100 °C –55 °C to +125 °C	±2 °C ±3 °C

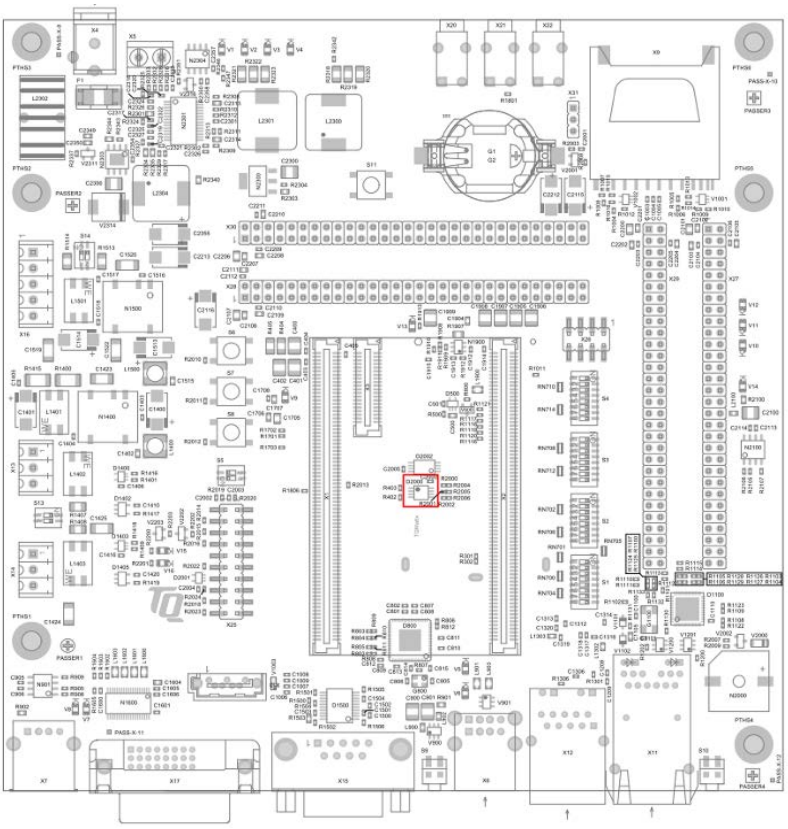


Figure 5: Position of LM75A (D2000)

The LM75A is on the top side of the MBa6x, in the middle of the plug-in position for the TQMa6x.

3.1.4 EEPROM

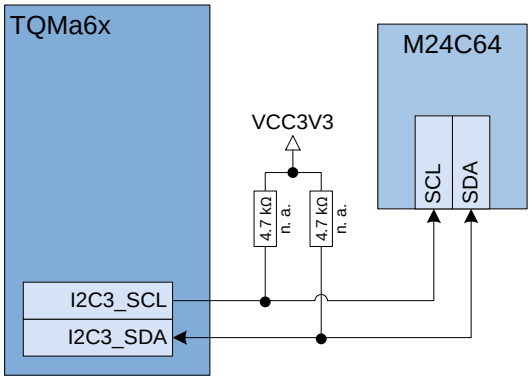


Figure 6: Block diagram EEPROM

The MBa6x provides a 64 Kbit EEPROM to save data (e.g., MAC address and serial number of the MBa6x).

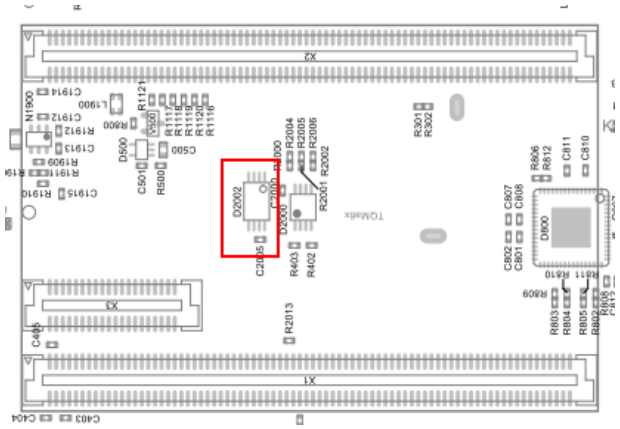


Figure 7: Position of EEPROM (D2002)

The EEPROM is on the top side of the MBa6x, in the middle of the plug-in position for the TQMa6x.
The following table shows the EEPROM used.

Table 10: Device EEPROM

Manufacturer	Part number	Size	Temperature range
STM	M24C64-WDW6TP	64 kbit	–45 °C to +85 °C

➢ The I²C address of the EEPROM is `0x57 / 101 0111b`

The data in the EEPROM is not essential for the correct operation of the MBa6x. The user can delete or alter the data.
In the following table, the parameters stored in the EEPROM are shown.

Table 11: EEPROM, MBa6x-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
`0x00`	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
`0x20`	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
`0x30`	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
`0x40`	Variable	Variable	$64_{(10)}$	ASCII	Order code
`0x80`	–	–	$8064_{(10)}$	–	(Unused)

3.1.5 RTC

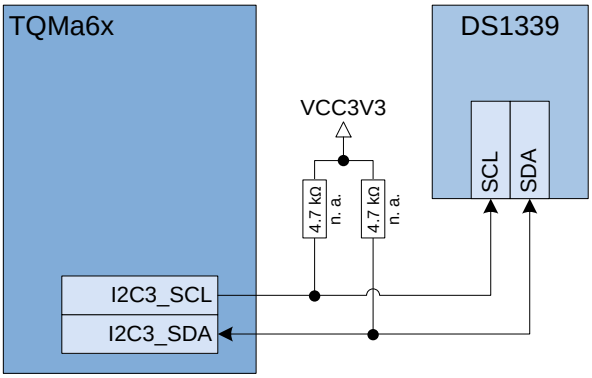


Figure 8: Block diagram RTC

The MBa6x provides an RTC. Another RTC is provided by the i.MX6 on the TQMa6x.
A lithium battery with very low self-discharge is provided as a backup supply for both RTCs.
A jumper connects the battery with the desired RTC.

Table 12: RTC supply, jumper settings

Component	Jumper X31	Remark
CPU RTC	1 – 2	PMIC connects the RTC of the CPU to battery.
MBa6x RTC	2 – 3	RTC on MBa6x is connected to battery.

The increased current consumption must be considered, if the RTC in the i.MX6 is used. This leads to a fast discharge of the battery. More information can be found in the TQMa6x User's Manual.
For the RTCs installed on the MBa6x the following applies:

Table 13: Electrical characteristics DS1339 RTC

Parameter	Min.	Typ.	Max.	Unit
Backup voltage at DS1339-VBACKUP (V_{RTC})	1.3	–	3.7	V
Current consumption DS1339	–	0.4	0.7	µA

The RTC on the MBa6x is on the bottom side, near the audio codec.

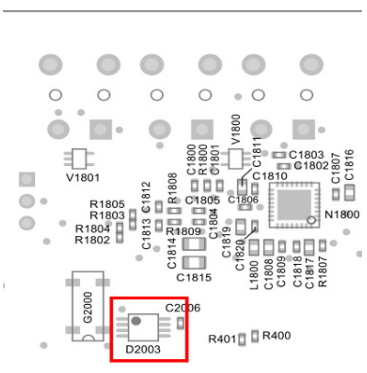


Figure 9: Position of RTC (D2003)

3.1.5 RTC (continued)

The header for the battery supply is on the top side, next to the SD card holder.

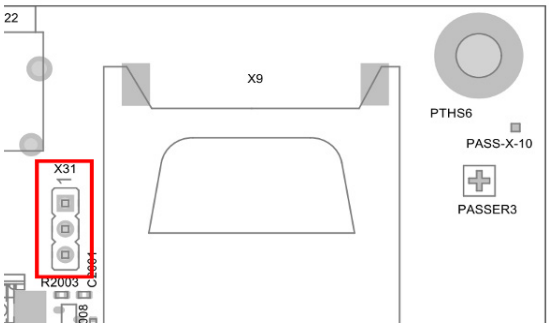


Figure 10: Header for selection of battery supply (X31)

Table 14: Pinout X31

Pin	Signal
1	LICELL
2	VBATT
3	VRTC

3.1.6 Power and Reset

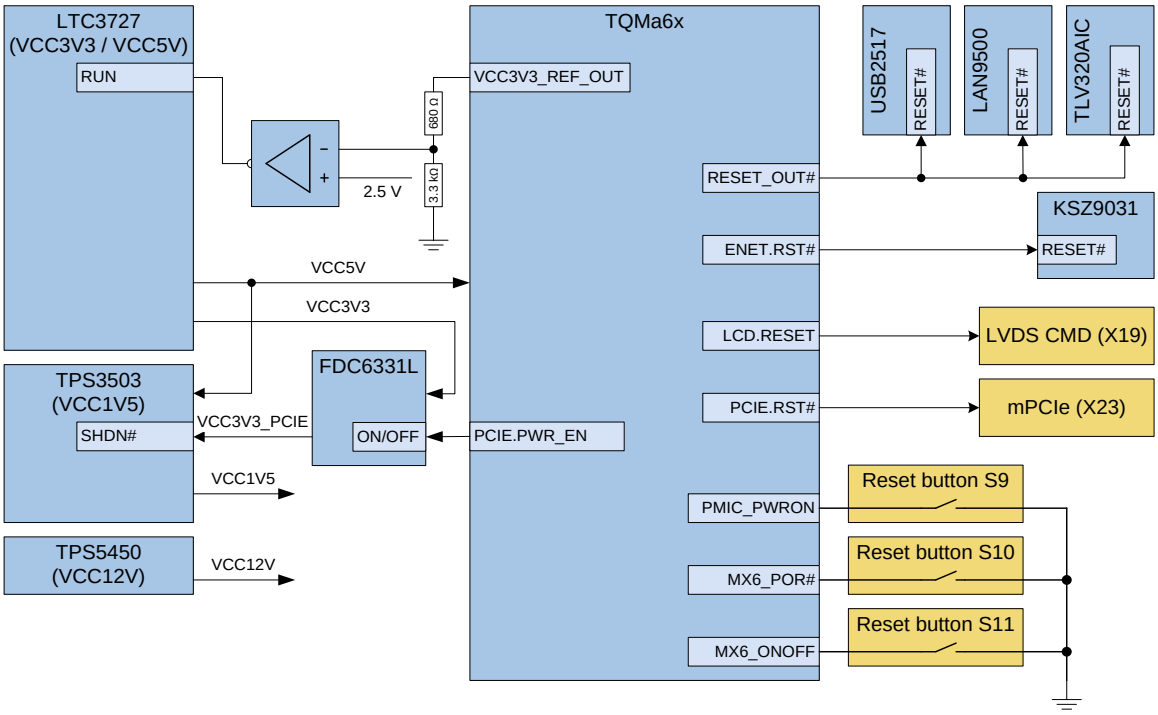


Figure 11: Block diagram Power and Reset

The MBa6x provides several options to trigger a complete or partial reset of the assembly.
The MBa6x provides four signals to reset sections of the circuit.

Table 15: MBa6x Reset signals

MBa6x Reset-Signal	Description
RESET_OUT	Signal resets USB hub (USB2517), USB Ethernet PHY (LAN9500) and audio-codec (TLV320AIC)
ENET.RST#	Signal resets the Gbit Ethernet PHYs (KSZ9031)
LCD.RESET	Signal resets a connected display
PCIE.RST#	Signal resets the PCIe device

3.1.6 Power and Reset (continued)

Two signals are provided for selective reset of the TQMa6x. [11]

Table 16: TQMa6x Reset signals

TQMa6x Reset-Signal	Description
PMIC_PWRON	Signal triggers a restart of the PMIC, Restarting the PMIC automatically triggers a reset of the CPU
MX6_POR#	Signal restarts the i.MX6, the PMIC is not affected

Two signals are provided to control the buck regulators.

Table 17: Buck regulator control

Signal	Description
PCIE.PWR_EN	This signal activates the power-switch in the supply of the PCIe interface. As soon as it is activated, N2302 begins to generate the 1.5 V.
VCC3V3_REF_OUT	This signal indicates, whether the TQMa6x is in the Power-Down mode. In the Power-Down mode the 3.3 V generated by the TQMa6x are switched off. As soon as this voltage drops below 3 V, the 3.3 V generated by the MBa6x are also switched off, to prevent a cross supply.

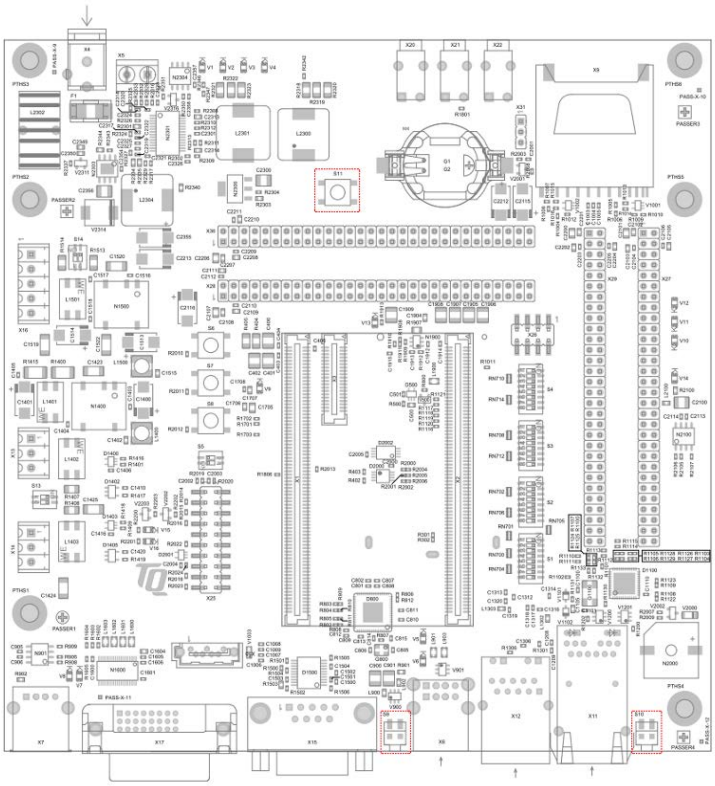


Figure 12: Position of Reset-Button / Power-Button (S9, S10, S11)

11: The exact functions and characteristics of the signals is to be taken from the TQMa6x User's Manual (7), the PMIC (5), and the CPU (1), (2).

3.1.7 Power supply

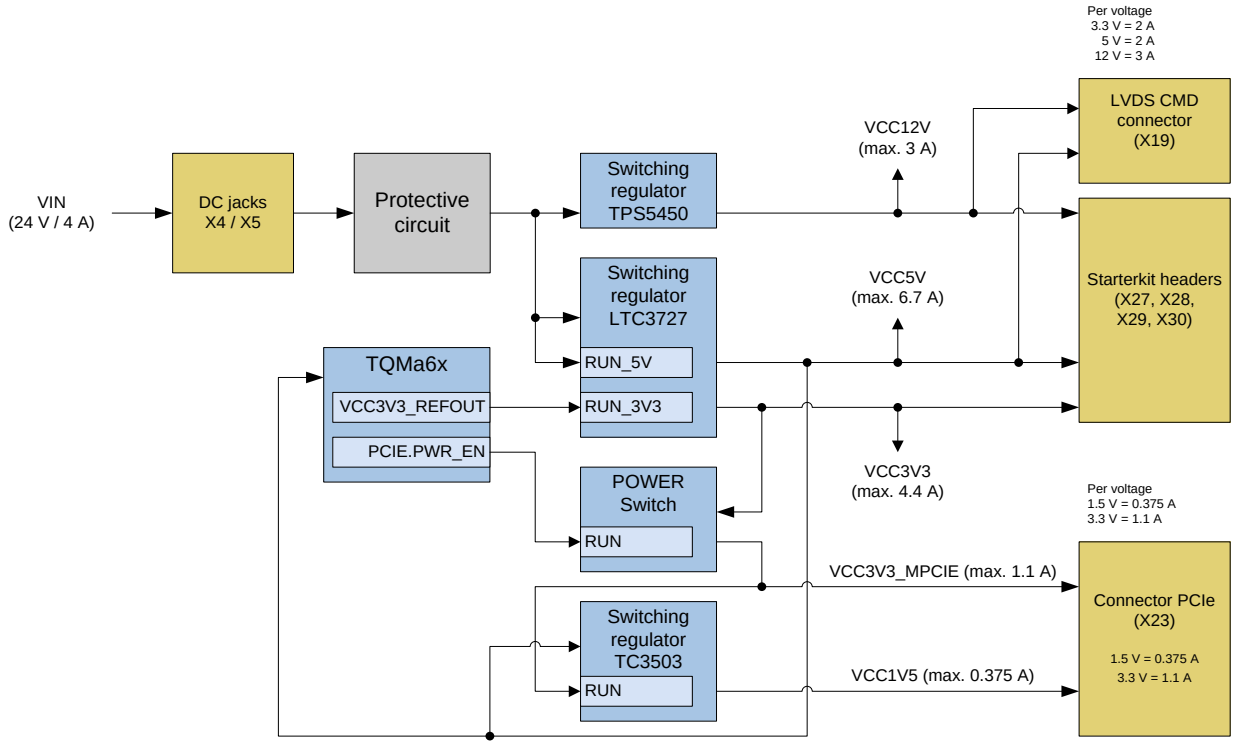


Figure 13: Block diagram power supply

The MBa6x is supplied with 24 V via X4 or X5. From this voltage 1.5 V, 3.3 V, 5 V and 12 V are generated on the MBa6x. These voltages are used to supply the components on the MBa6x.

Additionally, 3.3 V, 5 V and 12 V are available at each of the four headers (X27, X28, X29 and X30). 5 V and 12 V are available at the LVDS-CMD connector (X19). All five connectors share the available power (2 A @ 3.3 V, 2 A @ 5 V, 3 A @ 12 V).

The PCIe connector is supplied with 1.5 V and 3.3 V. 1.5 V is generated from 3.3 V and is only available at the PCIe connector. The 1.5 V rail can supply 0.375 A, the 3.3 V rail can supply 1.1 A.

Attention:	Usage of VCC3V3_REF_OUT
	In the own design, the buck regulator for VCC3V3 should be switched on or off with the signal VCC3V3_REF_OUT from the TQMa6x, to avoid cross supply and errors in the power-up/down sequence. [12]

12: Attention: When the PMIC is switched off, the voltage VCC3V3_REF_OUT (from the TQMa6x) drops to approx. 2.7 V due to cross-supply effects of the still activated 3.3 V (on the MBa6x). It must be ensured that the circuitry can respond to this level.

3.1.7.1 Protective circuitry

The 3.3 V / 5 V and the 12 V buck regulators are supplied with V_{IN}.
The protective circuit (Figure 14) has the following characteristics:

- Fuse 5 A slow blow
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

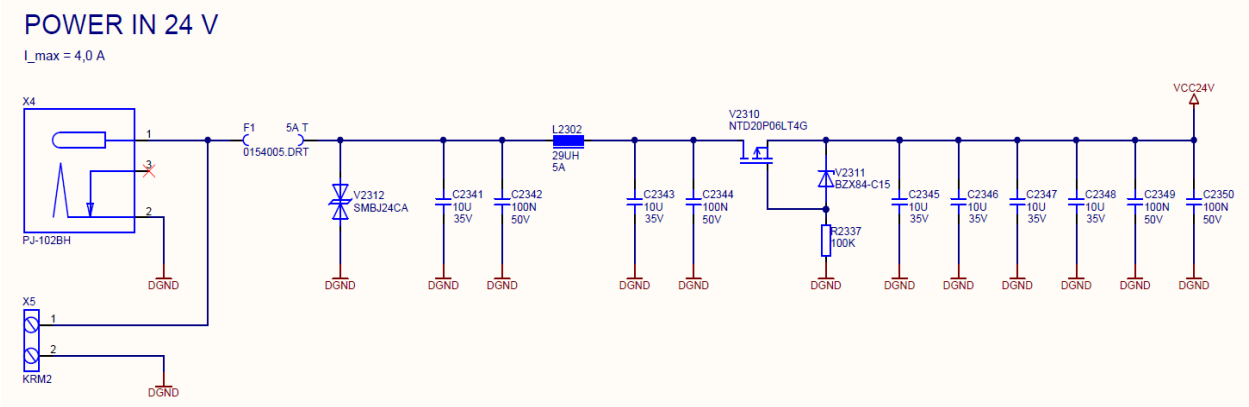


Figure 14: Protective circuit for V_{IN}

3.1.7.2 Power consumption

To measure the power consumption of the TQMa6x, two 50 mΩ resistors connected in parallel are assembled on the MBa6x.

The following figures show circuitry and position of the two 50 mΩ resistors on the MBa6x.

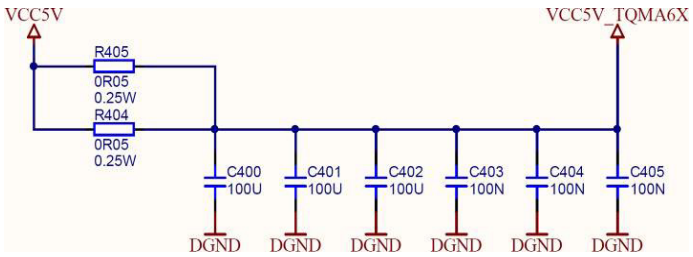


Figure 15: Schematics of shunts on MBa6x

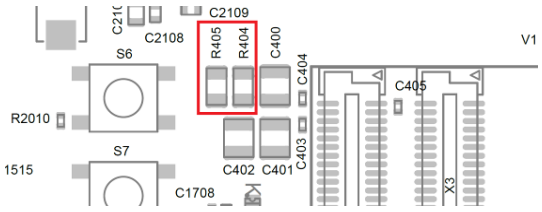


Figure 16: Position of shunts in 5 V line

3.1.7.3 Connectors X4, X5

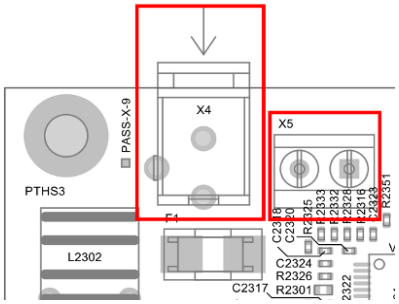


Figure 17: Position of connectors X4, X5

Table 18: Power supply, connectors

Manufacturer / Number	Description
Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V
Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A

3.2 Communication interfaces

3.2.1 USB 2.0 Hi-Speed Host

A USB hub provides five USB 2.0 Hi-Speed host interfaces. The hub provides an upstream port and seven downstream ports.

The USB connectors are supplied with 5 V by power distribution switches. The components used provide current monitoring and can switch off the bus voltage with overload and/or overheating. USB host 2 and 3 are routed to a stacked USB Type A connector (X6). USB host 6 is routed to a single Type A connector (X7). USB host 4 is available at Starterkit header X27 and USB host 7 at the LVDS-CMD connector (X19).

On the MBa6x, USB host 1 is connected to the USB-Ethernet-PHY (LAN9500) and USB host 5 to the Mini PCIe interface (X23).

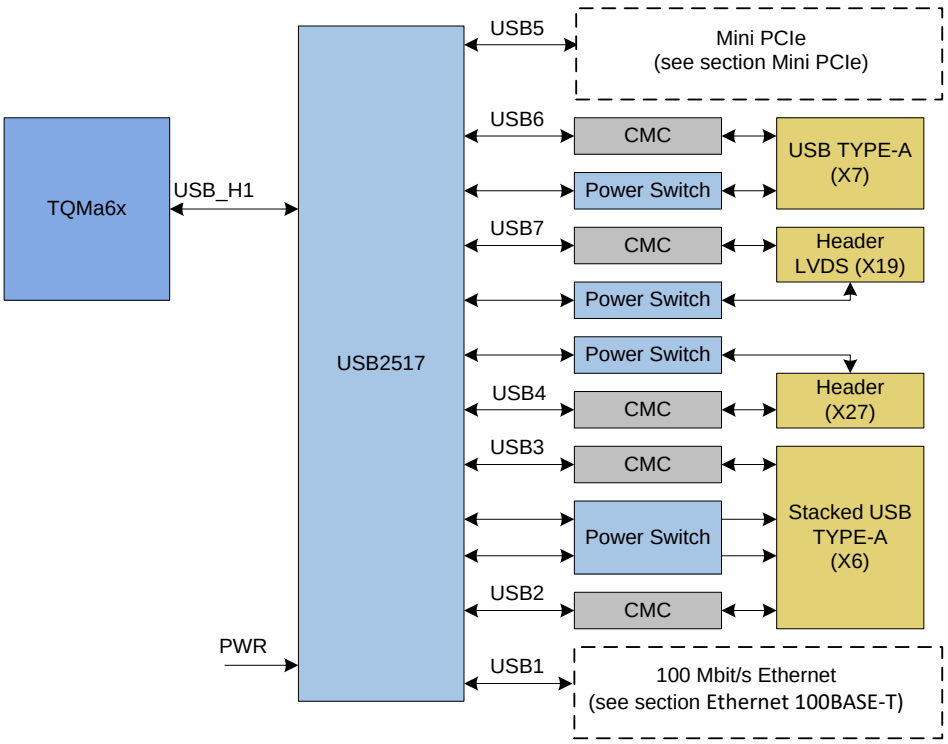


Figure 18: Block diagram USB-Hub

The USB host port of the TQMa6x provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

3.2.1 USB 2.0 Hi-Speed Host (continued)

Table 19: USB characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	–
Current	–	500	900	mA	500 mA continuous, 900 mA short circuit
Load step change	–	–90	–	mV	Host 2 – when adding a load of 500 mA
Read rate	–	23.7	–	Mbyte/s	Host 2 – USB-HDD an Port 3: 1.2 Gbyte file, 16 Mbyte block size
Write rate	–	18.3	–	Mbyte/s	Host 2 – USB-HDD an Port 3: 1.2 Gbyte file, 16 Mbyte block size

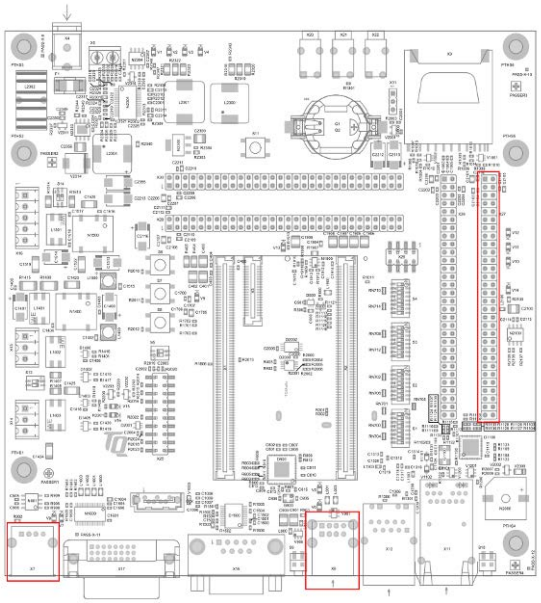


Figure 19: Position of USB connectors X6, X7, X27

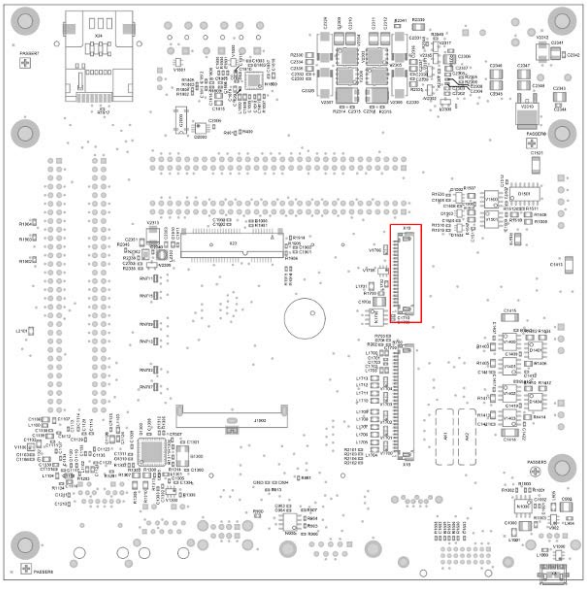


Figure 20: Position of LVDS-CMD connector X19

3.2.1 USB 2.0 Hi-Speed Host (continued)

Table 20: Pinout USB-Host 2/3 (X6)

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H2_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H2_D_N	I/O	Common mode choke in series
3A	D+	USB_H2_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	–
1B	VBUS	USB_H3_VBUS	P	100 µF to DGND; EMI filter
2B	D–	USB_H3_D_N	I/O	Common mode choke in series
3B	D+	USB_H3_D_P	I/O	Common mode choke in series
4B	DGND	DGND	P	–
M1 – M4	DGND	DGND	P	–

Table 21: Pinout USB-Host 6 (X7)

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H6_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H6_D_N	I/O	Common mode choke in series
3A	D+	USB_H6_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	–
M1, M2	DGND	DGND	P	–

Table 22: Pinout USB-Host 7 (X19)

Pin	Pin name	Signal	Dir.	Remark
11	VBUS	USB_H7_VBUS	P	100 µF to DGND; EMI filter
13	D–	USB_H7_D_N	I/O	Common mode choke in series
14	D+	USB_H7_D_P	I/O	Common mode choke in series

Table 23: Pinout USB-Host 4 (X27)

Pin	Pin name	Signal	Dir.	Remark
34	VBUS	USB_H4_VBUS	P	100 µF to DGND; EMI filter
36	D–	USB_H4_D_N	I/O	Common mode choke in series
38	D+	USB_H4_D_P	I/O	Common mode choke in series

3.2.2 USB 2.0 Hi-Speed OTG

The USB OTG interface of the TQMa6x is provided on the MBa6x. The OTG compatibility is maintained by a 5-pin Micro AB connector. The ID signal is directly routed to the CPU.

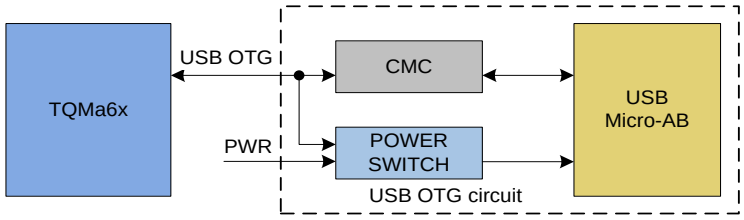


Figure 21: Block diagram USB 2.0 Hi-Speed OTG

The interface can be a client or a host. To use this feature the appropriate software support is necessary, however.

The OTG port provides a theoretical data rate of 480 Mbit/s. The data rate can significantly deviate depending on the hardware and software used.

Table 24: USB 2.0 Hi-Speed OTG characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	–
Current	–	500	900	mA	500 mA continuous, 900 mA short circuit
Load step change	–	–85	–	mV	When adding a load of 500 mA
Read rate	–	23.7	–	Mbyte/s	USB-HDD at USB OTG: 1.2 Gbyte file, 16 Mbyte block size
Write rate	–	18.3	–	Mbyte/s	USB-HDD at USB OTG: 1.2 Gbyte file, 16 Mbyte block size

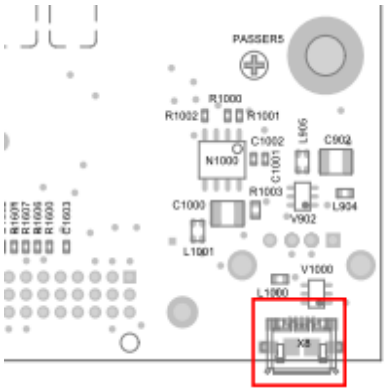


Figure 22: Position of USB 2.0 Hi-Speed OTG connector X8

Table 25: Pinout USB-Host OTG (X8)

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB_OTG_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
2	D–	USB_OTG_D_N	I/O	Common mode choke in series
3	D+	USB_OTG_D_P	I/O	Common mode choke in series
4	ID	USB_OTG.ID	I	–
5	DGND	DGND	P	–
M1 – M6	DGND	DGND	P	–

3.2.3 Ethernet 100BASE-T

The 100 Mbit/s Ethernet interface is provided by a USB to Ethernet controller. The LAN9500 is connected to USB host 1. The following Figure shows the connection.

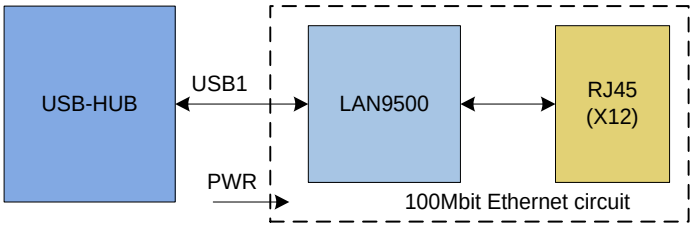


Figure 23: Block diagram Ethernet 100 BASE-T

Jack X12 contains integrated magnetics and two status LEDs.

This Ethernet interface corresponds to the IEEE 802.3 standard and offers an Auto-MDI-X detection.

Table 26: Ethernet 100BASE-T characteristics

Parameter	Min.	Typ.	Max.	Remark
Transfer rate UDP	–	85.2 Mbit/s	–	Upstream: tested with 100 m CAT6 cable
Transfer rate TCP	–	75.4 Mbit/s	–	Upstream: tested with 100 m CAT6 cable
Transfer rate UDP	–	82.0 Mbit/s	–	Downstream: tested with 100 m CAT6 cable
Transfer rate TCP	–	59.4 Mbit/s	–	Downstream: tested with 100 m CAT6 cable
Cable length	100 m	–	–	Tested with 100 m CAT6 cable

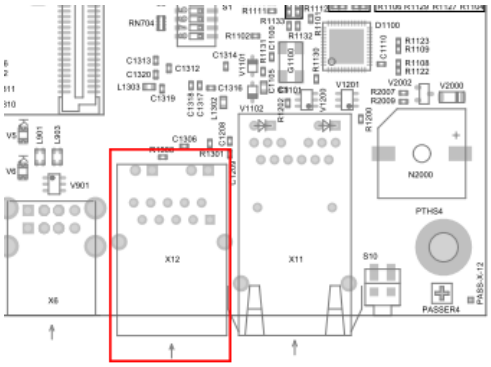


Figure 24: Position of Ethernet 100BASE-T connector X12

Table 27: Pinout Ethernet 100BASE-T (X12)

Pin	Pin name	Signal	Dir.
1	TX+	ETH100_TX_P	I/O
2	TX–	ETH100_TX_N	I/O
3	RX+	ETH100_RX_P	I/O
4	–	–	–
5	–	–	–
6	RX–	ETH100_RX_N	I/O
7	–	–	–
8	–	–	–

3.2.4 Ethernet 1000BASE-T

The MBa6x provides a Gigabit Ethernet interface.
This is implemented by the Micrel PHY KSZ9031.

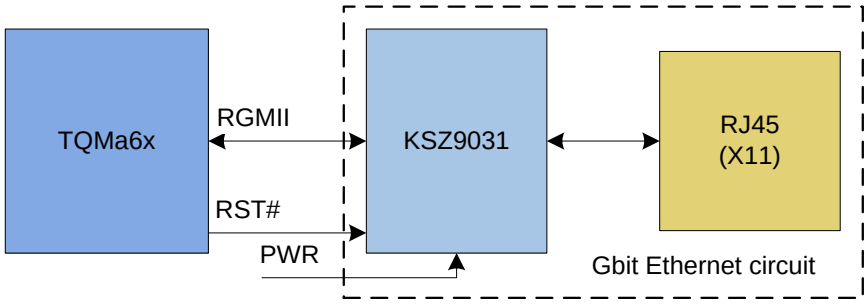


Figure 25: Block diagram Ethernet 1000BASE-T

The RJ45 jack (X11) contains integrated magnetics and two status LEDs.

The PHY has the following characteristics:

- Auto-negotiation capable
- Different speeds (10/100/1000 Mbps)
- Duplex-Modi (full/half)
- IEEE 802.3 compatible
- Wake-on-LAN
- Jumbo Frame Support

Table 28: Ethernet 1000BASE-T characteristics

Parameter	Min.	Typ.	Max.	Remark
Transfer rate TCP	–	–	286 Mbit/s	Upstream, 5 m cable
Transfer rate TCP	–	–	510 Mbit/s	Downstream, 5 m cable
Transfer rate TCP	–	–	130 Mbit/s 273 Mbit/s	Upstream, 5 m cable Downstream, 5 m cable

Attention:	Micrel PHY KSZ9031 works in Master-Mode
	The interface operates in Master-Mode on account of an erratum in the PHY (6). For this reason it is not possible to connect the MBa6x to other devices whose Ethernet interface also works in Master-Mode.

3.2.4 Ethernet 1000BASE-T (continued)

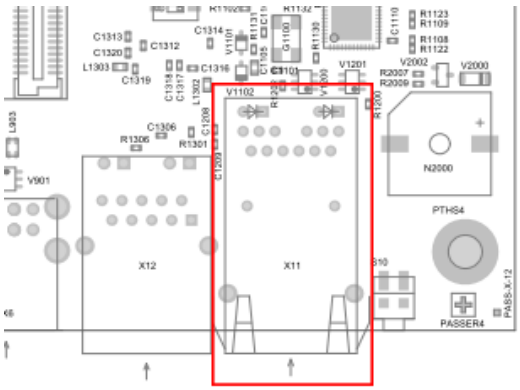


Figure 26: Position of Ethernet 1000BASE-T connector X11

Table 29: Pinout Ethernet 1000BASE-T (X11)

Pin	Pin name	Signal	Dir.
1	D1+	ETH1G_D1_P	I/O
2	D1–	ETH1G_D1_N	I/O
3	D2+	ETH1G_D2_P	I/O
4	D3+	ETH1G_D3_P	I/O
5	D3–	ETH1G_D3_N	I/O
6	D2–	ETH1G_D2_N	I/O
7	D4+	ETH1G_D4_P	I/O
8	D4–	ETH1G_D4_N	I/O

3.2.5 CAN

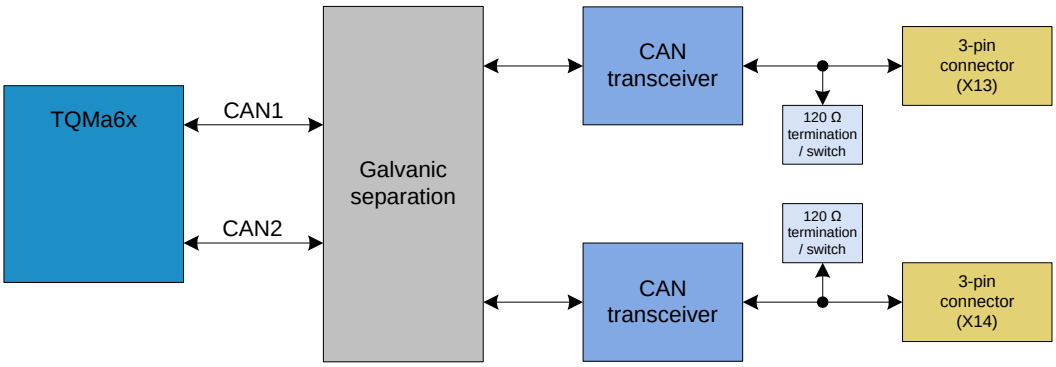


Figure 27: Block diagram CAN

Both CAN interfaces of the MBa6x are directly connected to the CAN ports of the TQMa6x and are made available at the 3-pin connectors X13 and X14. Both interfaces are galvanically separated.
The CAN interfaces are galvanically not separated among themselves.

The high speed mode is configured by default using a configuration resistor at the input RS of the CAN transceiver MCP2551 (390 Ω to Ground è maximum slew rate).

The high speed mode supports data rates up to 1 Mbit/s or maximum cable length. When required, the resistor at the RS input can be increased (10 kΩ to 120 kΩ) to reduce the slew rate. [13]

The CAN signals can be terminated with 120 Ω using DIP switches S13-1 and S13-2.

Table 30: CAN DIP switch settings

Switch	Interface	ON	OFF
S13-1	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated
S13-2	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated

The following characteristics apply to the interfaces:

Table 31: CAN characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	2.0	Mbaud	Tested up to 2.5 Mbaud
Line length	–	–	100	m	CAT.6 cable at 0.6 Mbaud
Line length	–	–	0.1	m	CAT.5 cable at 2 Mbaud
Electric strength	–	–	1.0	kV	–
Output voltage CANL	0.5	1.6	2.25	V	Dominant
Output voltage CANL	2.0	2.58	3.0	V	Recessive
Output voltage CANH	2.75	3.7	4.5	V	Dominant
Output voltage CANH	2.0	2.58	3.0	V	Recessive
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

13: See data sheet MCP2551.

3.2.5 CAN (continued)

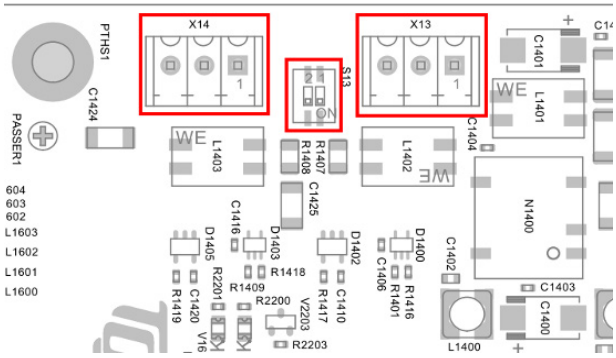


Figure 28: Position of CAN connectors X13, X14, and termination DIP switch S13

Table 32: Pinout CAN1 (X13)

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN1_H	I/O	Galvanically separated
2	CAN_L	CAN1_L	I/O	Galvanically separated
3	DGND	DGND_CAN	P	Galvanically separated

Table 33: Pinout CAN2 (X14)

Pin	Pin name	Signal	Dir.	Remark
1	CAN_H	CAN2_H	I/O	Galvanically separated
2	CAN_L	CAN2_L	I/O	Galvanically separated
3	DGND	DGND_CAN	P	Galvanically separated

3.2.6 RS-485

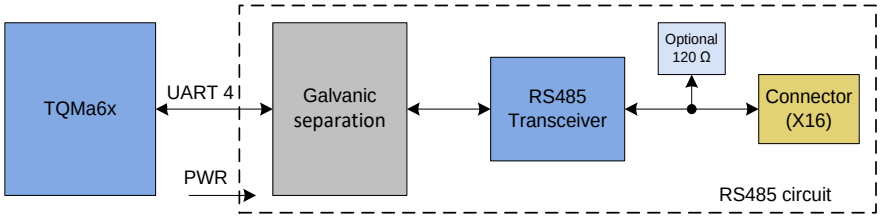


Figure 29: Block diagram RS-485

The UART4 interface of the TQMa6x is routed to an RS-485 transceiver (SP491), which provides the signals at the 9-pin D-Sub connector X16. The RS-485 interface is galvanically separated.

In full-duplex mode the interface can operate with a maximum data rate of 1 Mbit/s. With an assembly option half-duplex is also possible.

Table 34: RS-485 mode settings

Mode	R1511	R1512	Remark
Full-duplex	n.a.	0 Ω	Receiver always active (default)
Half-duplex	0 Ω	n.a.	Receiver controlled by CTS# (UART4.CTS#)

The RS-485 signals can be terminated with 120 Ω using DIP switches S14-1 and S14-2.

Table 35: RS-485 DIP switch settings

Switch	Interface	ON	OFF
S14-1	RS-485	Receive path terminated with 120 Ω	Receive path not terminated
S14-2	RS-485	Transmit path terminated with 120 Ω	Transmit path not terminated

The following characteristics apply to the interface:

Table 36: RS-485 characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	460.8	kbit/s	Tested up to 921.6 kbit/s with a maximum error rate of 3.3 %
Error rate	–	–	0.9	%	At 115.2 kbit/s with 1.8 m cable
Error rate	–	–	3.3	%	At 460.8 kbit/s with 1.8 m cable
Electric strength	–	–	1	kV	–
Output voltage RS-485_TXD	2	5.32	5.5	V	High-Level
Output voltage RS-485_TXD	0	0.24	0.8	V	Low-Level
Input voltage RS-485_RXD	2	5.2	5.5	V	High-Level
Input voltage RS-485_RXD	0	0.36	0.8	V	Low-Level
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

3.2.6 RS-485 (continued)

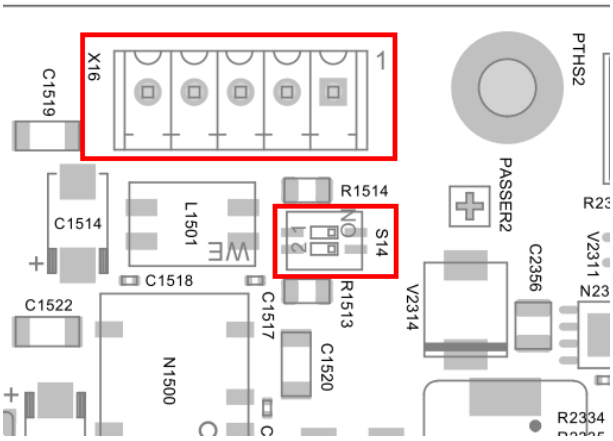


Figure 30: Position of RS-485 connector X16

Table 37: Pinout RS-485 (X16)

Pin	Pin name	Signal	Dir.	Remark
1	A	RS-485_A	I	Galvanically separated
2	B	RS-485_B	I	Galvanically separated
3	Y	RS-485_Y	O	Galvanically separated
4	Z	RS-485_Z	O	Galvanically separated
5	DGND	DGND_ RS-485	P	Galvanically separated

3.2.7 RS-232

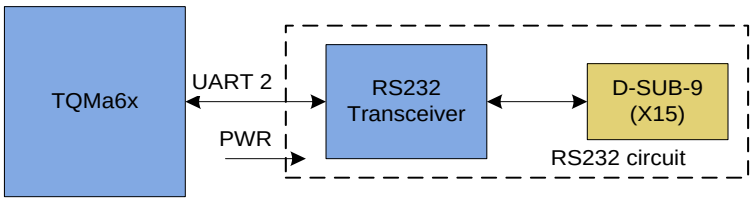


Figure 31: Block diagram RS-232

The UART2 interface of the TQMa6x is routed to transceiver SP3222E, which provides the signals at the 9-pin D-Sub connector X15. For UART2 the handshake signals RTS# and CTS# are available.

The interface is used to output debug information.

Additional information (e.g.: default baud rate) can be found in the TQMa6x Support-Wiki.

The following characteristics apply to the RS-232 interface:

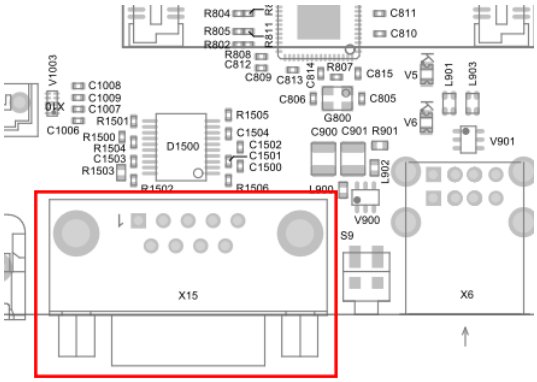


Figure 32: Position of RS-232 connector X15

Table 38: Pinout RS-485 (X15)

Pin	Pin name	Signal	Dir.	Remark
1	DCD	(NC)	–	Not used
2	RXD	RS-232_RXD	I	–
3	TXD	RS-232_TXD	O	–
4	DTR	(NC)	–	Not used
5	DGND	DGND	P	–
6	DSR	(NC)	–	Not used
7	RTS	RS-232_RTS#	O	–
8	CTS	RS-232_CTS#	I	–
9	RI	(NC)	–	Not used
M1, M2	DGND	DGND	P	–

3.2.8 HDMI

An external monitor can be connected at the HDMI interface.
For licence and stability reasons a DVI-D connector is used instead of an HDMI connector.

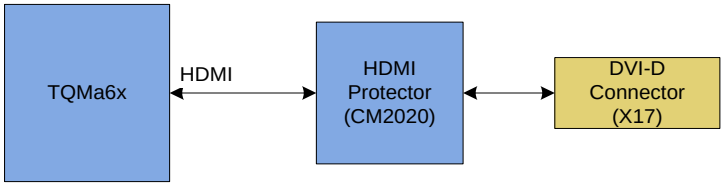


Figure 33: Block diagram HDMI

The interface is protected against ESD by an HDMI protector (CM2020). The characteristics of the interface are determined by the HDMI transmitter in the CPU. More information can be taken from the Reference Manual of the respective CPU. Analog signals are not supported by the interface.

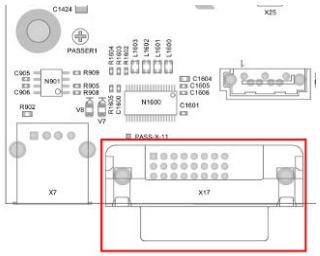


Figure 34: Position of HDMI connector X17

Table 39: Pinout HDMI (X17)

Pin	Pin name	Signal	Dir.	Remark
1	TMDS data 2–	HDMI_D2_N	O	Additional common mode choke in series
2	TMDS data 2+	HDMI_D2_P	O	Additional common mode choke in series
3	DGND	DGND	P	
4	–	(NC)	–	
5	–	(NC)	–	
6	DDC clock	HDMI_DDC_SCL_R	O	
7	DDC data	HDMI_DDC_SDA_R	I/O	
8	–	(NC)	–	
9	TMDS data 1–	HDMI_D1_N	O	Additional common mode choke in series
10	TMDS data 1+	HDMI_D1_P	O	Additional common mode choke in series
11	DGND	DGND	P	
12	–	(NC)	–	
13	–	(NC)	–	
14	+5 V	HDMI_5V_OUT	P	I_{max} = 75 mA
15	DGND	DGND	P	
16	Hot Plug Detect	HDMI_HPD	I	
17	TMDS data 0–	HDMI_D0_N	O	Additional common mode choke in series
18	TMDS data 0+	HDMI_D0_P	O	Additional common mode choke in series
19	DGND	DGND	P	
20	–	(NC)	–	
21	–	(NC)	–	
22	DGND	DGND	P	
23	TMDS clock +	HDMI_CLK_P	O	Additional common mode choke in series
24	TMDS clock –	HDMI_CLK_N	O	Additional common mode choke in series
M1, M2	DGND	DGND	P	

3.2.9 LVDS

Both LVDS interfaces of the TQMa6x (a clock pair and four data pairs) are directly routed to the 30-pin FFC (X18).
In addition to the LVDS signals 3.3 V and 5 V are provided at the connector.

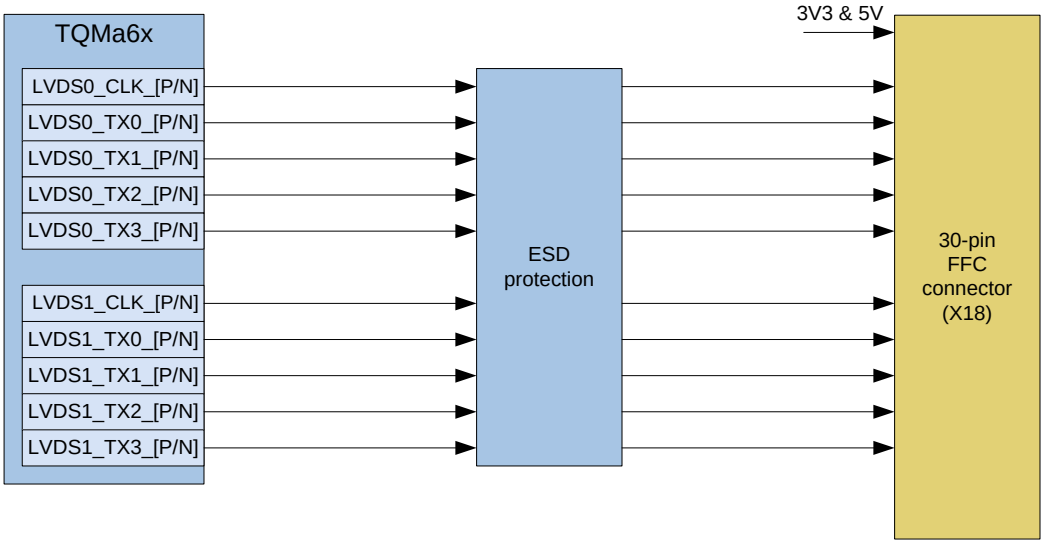


Figure 35: Block diagram LVDS

The characteristics of the interface are determined by the LVDS transmitter in the CPU.
More information can be taken from the Reference Manual of the respective CPU.

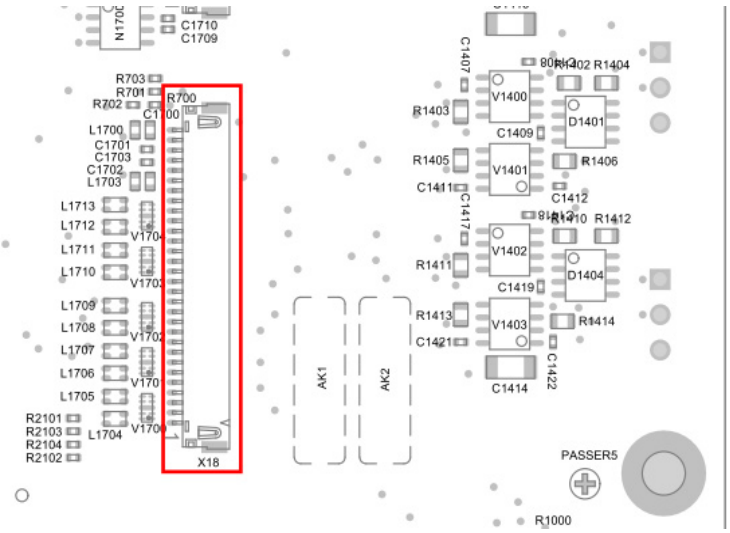


Figure 36: Position of LVDS connector X18

3.2.9 LVDS (continued)

Table 40: Pinout LVDS (X18)

Pin	Pin name	Signal	Dir.	Remark
1	LVDS0_TX0–	LVDS0_TX0_N	O	Additional common mode choke in series
2	LVDS0_TX0+	LVDS0_TX0_P	O	Additional common mode choke in series
3	LVDS0_TX1–	LVDS0_TX1_N	O	Additional common mode choke in series
4	LVDS0_TX1+	LVDS0_TX1_P	O	Additional common mode choke in series
5	LVDS0_TX2–	LVDS0_TX2_N	O	Additional common mode choke in series
6	LVDS0_TX2+	LVDS0_TX2_P	O	Additional common mode choke in series
7	DGND	DGND	P	
8	LVDS0_CLK–	LVDS0_CLK_N	O	Additional common mode choke in series
9	LVDS0_CLK+	LVDS0_CLK_P	O	Additional common mode choke in series
10	LVDS0_TX3–	LVDS0_TX3_N	O	Additional common mode choke in series
11	LVDS0_TX3+	LVDS0_TX3_P	O	Additional common mode choke in series
12	LVDS1_TX0–	LVDS1_TX0_N	O	Additional common mode choke in series
13	LVDS1_TX0+	LVDS1_TX0_P	O	Additional common mode choke in series
14	DGND	DGND	P	
15	LVDS1_TX1–	LVDS1_TX1_N	O	Additional common mode choke in series
16	LVDS1_TX1+	LVDS1_TX1_P	O	Additional common mode choke in series
17	DGND	DGND	P	
18	LVDS1_TX2–	LVDS1_TX2_N	O	Additional common mode choke in series
19	LVDS1_TX2+	LVDS1_TX2_P	O	Additional common mode choke in series
20	LVDS1_CLK–	LVDS1_CLK_N	O	Additional common mode choke in series
21	LVDS1_CLK+	LVDS1_CLK_P	O	Additional common mode choke in series
22	LVDS1_TX3–	LVDS1_TX3_N	O	Additional common mode choke in series
23	LVDS1_TX3+	LVDS1_TX3_P	O	Additional common mode choke in series
24	DGND	DGND	P	
25	VCC5V	VCC5V_LVDS	P	I_{max} = 1 A [14] [15] 10 µF + 1 µF to Ground; ferrite in series
26	VCC5V	VCC5V_LVDS	P	
27	VCC5V	VCC5V_LVDS	P	
28	VCC3V3	VCC3V3_LVDS	P	I_{max} = 1 A [14] [15] 10 µF + 1 µF to Ground; ferrite in series
29	VCC3V3	VCC3V3_LVDS	P	
30	VCC3V3	VCC3V3_LVDS	P	
M1, M2	DGND	DGND	P	

14: Due to maximum load of FFC contacts.
15: Excluding the current drawn from the headers.

3.2.10 LVDS-CMD

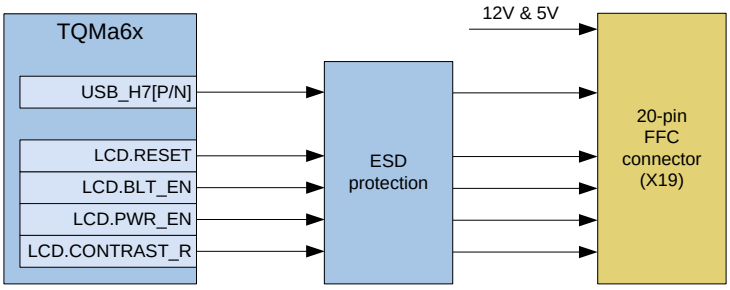


Figure 37: Block diagram LVDS-CMD

To connect an LVDS display, the LVDS-CMD connector (X19) is placed near the LVDS connector (X18).
The FFC connector X19 provides a USB interface and control signals for display and backlight.
In addition to the data signals 5 V and 12 V are available as supply voltages.

Table 41: LVDS-CMD characteristics

Parameter	Min.	Typ.	Max.	Remark
Current at 12 V	–	–	1 A	–
Current at 5 V	–	–	1 A	–
USB signals	–	–	–	Characteristics see section 3.2.1
Level for display / backlight signals	0 V	–	3.3 V	–

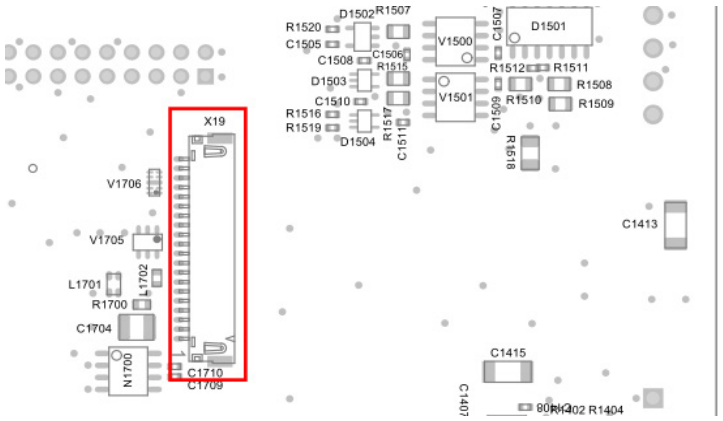


Figure 38: Position of LVDS-CMD connector X19

3.2.10 LVDS-CMD (continued)

Table 42: Pinout LVDS CMD (X19)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	I_{max} = 1 A [16] [17] 10 µF + 1 µF to Ground
2	VCC12V	VCC12V	P	
3	VCC12V	VCC12V	P	
4	DGND	DGND	P	
5	DGND	DGND	P	
6	DGND	DGND	P	
7	VCC5V	VCC5V	P	I_{max} = 1 A [16] [17] 10 µF + 1 µF to Ground
8	VCC5V	VCC5V	P	
9	DGND	DGND	P	
10	DGND	DGND	P	
11	VBUS	USB_H7_VBUS	P	100 µF to DGND; EMI filter
12	DGND	DGND	P	
13	D+	USB_H7_D_N	I/O	Common mode choke in series
14	D–	USB_H7_D_P	I/O	Common mode choke in series
15	DGND	DGND	P	
16	LCD_RESET	LCD.RESET	O	
17	LCD_BLT_EN	LCD.BLT_EN	O	
18	LCD_PWR_EN	LCD.PWR_EN	O	
19	LCD_CONTRAST	LCD.CONTRAST_R	O	
20	DGND	DGND	P	
M1, M2	DGND	DGND	P	

16: Due to maximum load of FFC contacts.
17: Excluding the current drawn from the headers.

3.2.11 Audio

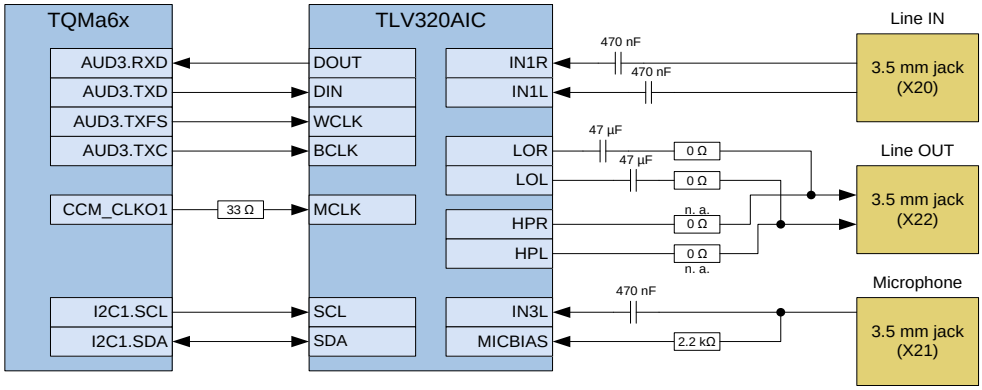


Figure 39: Block diagram audio

Audio input and output is possible with the audio codec TLV320AIC. The codec is routed to the AUD3 interface of the i.MX6. The MBa6x provides a stereo line-in, a stereo line-out and a microphone input.

An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 43: Configuration line-out or headphone

Mode	R1802	R1803	R1804	R1805	Remark
Headphone	n.a.	n.a.	0 Ω	0 Ω	Default
Line-out	0 Ω	0 Ω	n.a.	n.a.	–

The following tables show the characteristics of the audio codec.

Table 44: Audio headphone characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Load resistor	14.4	16	–	Ω	Single-ended configuration
Load resistor	24.4	32	–	Ω	Differential configuration
Output power	–	64	–	mW	–40 dB THD @ 16 Ω input impedance
Output power	–	40	–	mW	–40 dB THD @ 32 Ω input impedance
Signal-noise ratio	87	100	–	dB	

Table 45: Audio line-out characteristics

Parameter	Min.	Typ.	Max.	Unit
Load resistor	0.6	106	–	kΩ
Signal-noise ratio	87	100	–	dB

Table 46: Audio line-in characteristics

Parameter	Min.	Typ.	Max.	Unit
Signal-noise ratio	80	93	–	dB

Table 47: Microphone characteristics

Parameter	Min.	Typ.	Max.	Unit
Output Noise	–	10	–	μV_{RMS}
Current	–	3	–	mA

3.2.11 Audio (continued)

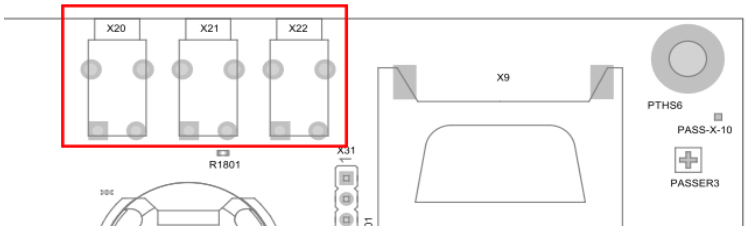


Figure 40: Position of audio connectors X20, X21, X22

Table 48: Pinout line-in (X20)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	–
2A,2B	Left	LINE_IN_L	I	470 nF in series; ESD protection
3	Right	LINE_IN_R	I	470 nF in series; ESD protection

Table 49: Pinout Microphone (X21)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	–
2A,2B	Left	MIC_IN	I	2.2 kΩ in series to MIC_BIAS; ESD protection
3	Right	AGND_AUDIO	I	10 kΩ in series, right channel unused (mono)

Table 50: Pinout line-out (X22)

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	–
2A,2B	Left	AUDIO_OUT_L	O	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; optional connection to HP_L; ESD protection is possible
3	Right	AUDIO_OUT_R	O	1 µF and 100 Ω in series; 47 nF to AGND_AUDIO; optional connection to HP_R; ESD protection is possible

3.2.12 SD card

The SD card slot is directly connected with the SDHC controller of the TQMa6x.
Serial resistors are integrated in the data lines or control lines to adjust the line attenuation.

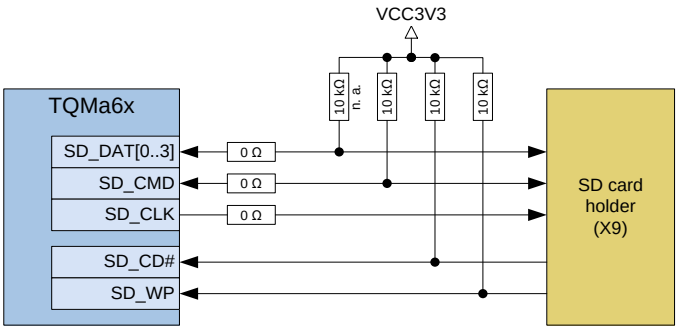


Figure 41: Block diagram SD card

It is possible to boot from SD card (see section 3.3.5). The read and write speeds of the SD card interface depend on the SD card used. The following table shows values measured with Class 4 and Class 10 SD cards. The maximum available data rate is to be taken from the respective CPU Reference Manual.

Table 51: SD card characteristics

Parameter	Min.	Typ.	Max.	Remark
Read	–	17.7 Mbyte/s	–	SanDisk Class 10 SD card, 200 Mbyte file with 25 Mbyte block size
Write	–	15.6 Mbyte/s	–	
Read	–	17.1 Mbyte/s	–	SanDisk Class 4 SD card, 200 Mbyte file with 25 Mbyte block size
Write	–	3.5 Mbyte/s	–	

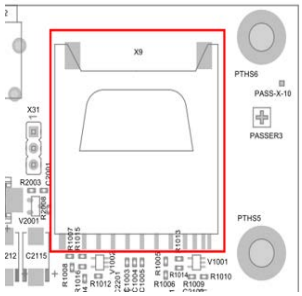


Figure 42: Position of SD card connector X9

Table 52: Pinout SD card (X9)

Pin	Pin name	Signal	Dir.	Remark
1	CD/DAT3/CS	SD2.DAT3_R	I/O	0 Ω in series
2	CMD/DI	SD2.CMD_R	I/O	0 Ω in series; 10 kΩ to VCC3V3
3	VSS1	DGND	P	–
4	VDD	VCC3V3	P	1 µF + 100 nF + 10 nF to Ground
5	CLK	SD2.CLK_R	O	0 Ω in series
6	VSS2	DGND	P	–
7	DAT0/DO	SD2.DAT0_R	I/O	0 Ω in series
8	DAT1	SD2.DAT1_R	I/O	0 Ω in series
9	DAT2	SD2.DAT2_R	I/O	0 Ω in series
CDS	CARD_DETECT	SD2.CD#	I	10 kΩ to VCC3V3
COM	COMMON	DGND	P	–
WP	WRITE_PROTECT	SD2.WP	I	10 kΩ to VCC3V3
M1, M2	DGND	DGND	P	–

3.2.13 SATA

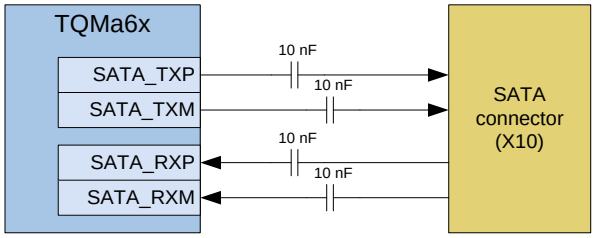


Figure 43: Block diagram SATA interface

The SATA interface of the TQMa6x is directly connected to a 7-pin SATA connector via capacitive coupling (10 nF).
A SATA device must be supplied separately, e.g., via the power OUT header. All four data lines provide ESD protection.
It is possible to boot from SATA (see section 3.3.5).
The SATA interface has the following characteristics:

- Serial ATA 3.0
- AHCI Revision 1.3
- AMBA 2.0 from ARM
- 1.5 Gbit/s and 3.0 Gbit/s SATA data rate

Table 53: SATA characteristics [18]

Parameter	Min.	Typ.	Max.	Remark
Read	–	57.0 Mbyte/s	–	1 Gbyte with block size 512 Kbyte
Write	–	9.0 Mbyte/s	–	1 Gbyte with block size 512 Kbyte
Read	–	56.9 Mbyte/s	–	1 Gbyte with block size 10 Mbyte
Write	–	24.8 Mbyte/s	–	1 Gbyte with block size 10 Mbyte

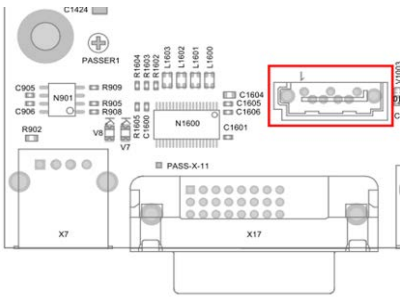


Figure 44: Position of SATA connector X10

Table 54: Pinout SATA (X10)

Pin	Pin name	Signal	Dir.	Remark
1	DGND	DGND	P	–
2	TX+	SATA_TX_P	I	10 nF in series; ESD protection
3	TX–	SATA_TX_N	I	10 nF in series; ESD protection
4	DGND	DGND	P	–
5	RX–	SATA_RX_N	O	10 nF in series; ESD protection
6	RX+	SATA_RX_P	O	10 nF in series; ESD protection
7	DGND	DGND	P	–
M1, M2	DGND	DGND	P	–

18: Tested with hard disk WD1200JS.

3.2.14 Mini PCIe

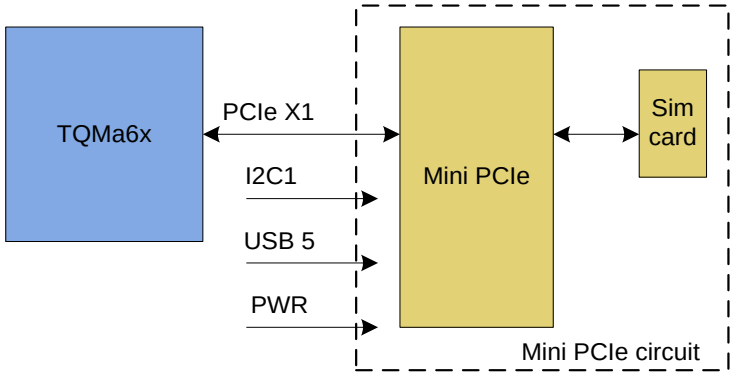


Figure 45: Block diagram Mini PCIe

The MBa6x provides a Mini PCIe interface. It is fully connected (PCIe lane, I²C, USB) and thereby permits the use of various Mini PCIe devices. A SIM card holder is also available to connect an UMTS / GSM modem.

Table 55: Mini PCIe characteristics

Parameter	Min.	Typ.	Max.	Remark
Current @ 3.3 V	–	–	1.1 A	–
Current @ 1.5 V	–	–	0.375 A	–
USB signals	–	–	–	Characteristics see section 3.2.1

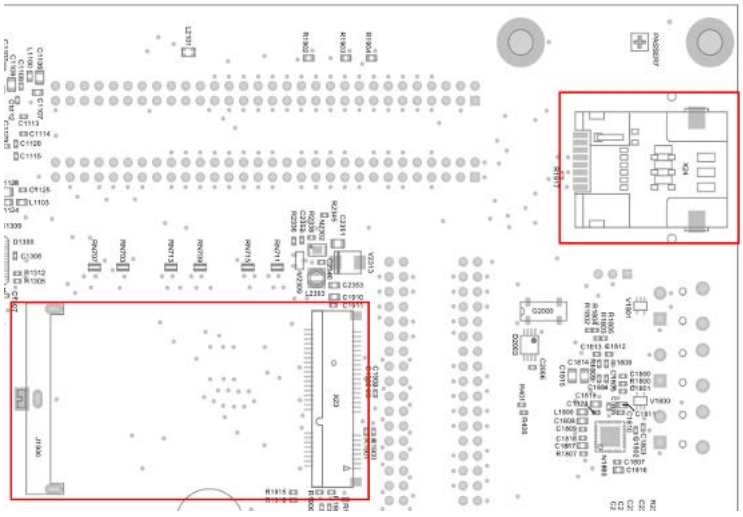


Figure 46: Position of Mini PCIe connectors X23, X24, J1900

3.2.14 Mini PCIe (continued)

Table 56: Pinout Mini PCIe (X23)

Pin	Pin name	Signal	Dir.	Remark
1	WAKE	PCIE.WAKE#	O	
2	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
3	–	(NC)	–	
4	DGND	DGND	P	
5	–	(NC)	–	
6	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
7	–	(NC)	–	
8	UIM_PWR	UIM_PWR	P	
9	DGND	DGND	P	
10	UIM_DATA	UIM_DATA	I/O	
11	CLK–	PCIE_REFCLK_N	O	100 nF in series; 49.9 Ω to Ground
12	UIM_CLK	UIM_CLK	I	
13	CLK+	PCIE_REFCLK_P	O	100 nF in series; 49.9 Ω to Ground
14	UIM_RST	UIM_RST	I	
15	DGND	DGND	P	
16	UIM_VPP	UIM_VPP	P	
17	–	(NC)	–	
18	DGND	DGND	P	
19	–	(NC)	–	
20	DIS	PCIE.DIS#	O	
21	DGND	DGND	P	
22	RST	PCIE.RST#	O	
23	RX–	PCIE_RX_N	I	0 Ω in series
24	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
25	RX+	PCIE_RX_P	I	0 Ω in series
26	DGND	DGND	P	
27	DGND	DGND	P	
28	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
29	DGND	DGND	P	
30	SCL	I2C1.SCL	O	
31	TX–	PCIE_TX_N	O	100 nF in series
32	SDA	I2C1.SDA	I/O	
33	TX+	PCIE_TX_P	O	100 nF in series
34	DGND	DGND	P	
35	DGND	DGND	P	
36	USB_D–	USB_H5_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB_D+	USB_H5_D_P	I/O	Common mode choke in series
39	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
40	DGND	DGND	P	
41	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground
42	WWAN	LED_WWAN#	I	Connected to LED
43	DGND	DGND	P	
44	WLAN	LED_WLAN#	I	Connected to LED
45	–	(NC)	–	
46	WPAN	LED_WPAN#	I	Connected to LED
47	–	(NC)	–	
48	VCC1V5	VCC1V5	P	Can be switched off indirectly by N1900; 3 × 100 µF + 4.7 µF to Ground
49	–	(NC)	–	
50	DGND	DGND	P	
51	–	(NC)	–	
52	VCC3V3	VCC3V3_MPCIE	P	Can be switched off by N1900; 5 × 100 µF + 4.7 µF to Ground

Table 57: Pinout SIM card (X24)

Pin	Pin name	Signal	Dir.
C1	PWR	UIM_PWR	P
C2	RST	UIM_RST	O
C3	CLK	UIM_CLK	O
C5	DGND	DGND	P
C6	VPP	UIM_VPP	P
C7	DATA	UIM_DATA	I/O
SW1, SW2	–	–	–

3.2.15 Headers

All unused signals are routed to the headers X27, X28, X29, X30 on the MBa6x, to permit a comprehensive evaluation of the TQMa6x modules. All headers are 60-pin with 100 mil pitch.

The headers are positioned in such a way, that adaptor boards which additional electronics and connectors can be plugged in.

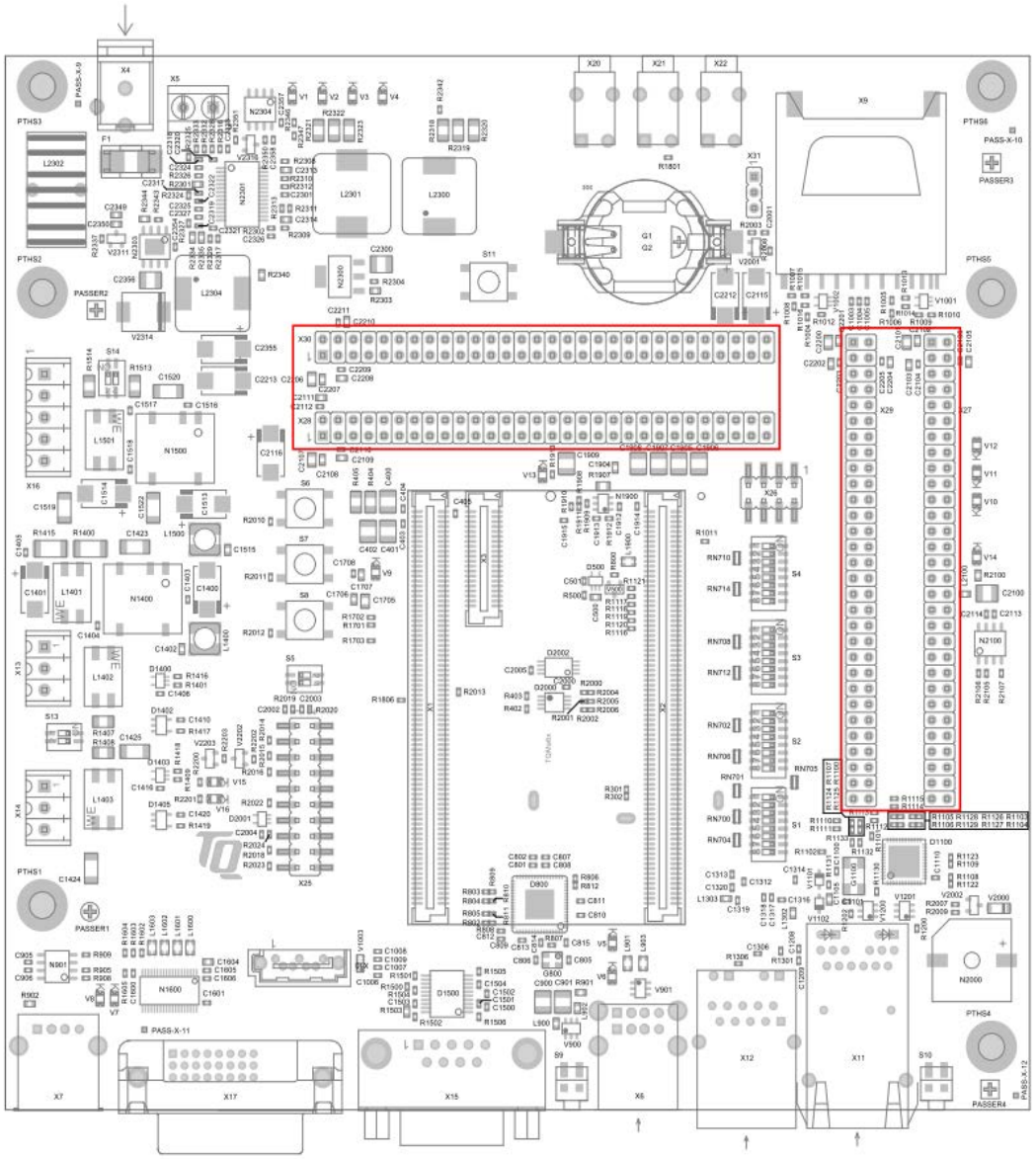


Figure 47: Position of pin headers X27, X28, X29, X30

3.2.15 Headers (continued)

Table 58: Pinout header 1 (X27)

Pin	Interface	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DISP0	DISP0.CLK	O	
8	DISP0	DISP0.DRDY	O	
9	DISP0	DISP0.HSYNC	O	
10	DISP0	DISP0.DAT1	O	
11	DISP0	DISP0.VSYNC	O	
12	DISP0	DISP0.DAT3	O	
13	DISP0	DISP0.DAT0	O	
14	DISP0	DISP0.DAT5	O	
15	DISP0	DISP0.DAT2	O	
16	DISP0	DISP0.DAT7	O	
17	DISP0	DISP0.DAT4	O	
18	DISP0	DISP0.DAT9	O	
19	DISP0	DISP0.DAT6	O	
20	DISP0	DISP0.DAT11	O	
21	DISP0	DISP0.DAT8	O	
22	DISP0	DISP0.DAT13	O	
23	DISP0	DISP0.DAT10	O	
24	DISP0	DISP0.DAT15	O	
25	DISP0	DISP0.DAT12	O	
26	DISP0	DISP0.DAT17	O	
27	DISP0	DISP0.DAT14	O	
28	DISP0	DISP0.DAT19	O	
29	DISP0	DISP0.DAT16	O	
30	DISP0	DISP0.DAT21	O	
31	DISP0	DISP0.DAT18	O	
32	DISP0	DISP0.DAT23	O	
33	DISP0	DISP0.DAT20	O	
34	USB	USB_H4_VBUS	P	100 µF to DGND; EMI filter
35	DISP0	DISP0.DAT22	O	
36	USB	USB_H4_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB	USB_H4_D_P	I/O	Common mode choke in series
39	I2C1	I2C1.SCL	O	
40	DGND	DGND	P	
41	I2C1	I2C1.SDA	I/O	
42	SPI1	SPI1.SS2#	O	
43	SPI1	SPI1.MOSI	O	
44	SPI1	SPI1.MISO	I	
45	SPI1	SPI1.SS3#	O	
46	SPI1	SPI1.SCLK	O	
47	–	–	–	
48	DGND	DGND	P	
49	LCD	LCD.PWR_EN	O	Pull-Down or Pull-Up can be assembled
50	LCD	LCD.BLT_EN	O	
51	LCD	LCD.RESET	O	Pull-Down or Pull-Up can be assembled
52	LCD	LCD.CONTRAST_R	O	
53	DGND	DGND	P	
54	DGND	DGND	P	
55	–	–	–	
56	–	–	–	
57	–	–	–	
58	–	–	–	
59	DGND	DGND	P	
60	DGND	DGND	P	

3.2.15 Headers (continued)

Table 59: Pinout header 2 (X28)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DGND	DGND	P	
8	DGND	DGND	P	
9	XTAL2	XTAL2.CLK2_P	O	
10	MIPI_DSI	MIPI_DSI.CLK0_N	O	
11	XTAL2	XTAL2.CLK2_N	O	
12	MIPI_DSI	MIPI_DSI.CLK0_P	O	
13	DGND	DGND	P	
14	DGND	DGND	P	
15	DGND	DGND	P	
16	DGND	DGND	P	
17	MIPI_CSI	MIPI_CSI.D3_P	I	
18	MIPI_DSI	MIPI_DSI.D0_N	O	
19	MIPI_CSI	MIPI_CSI.D3_N	I	
20	MIPI_DSI	MIPI_DSI.D0_P	O	
21	DGND	DGND	P	
22	DGND	DGND	P	
23	MIPI_CSI	MIPI_CSI.D2_P	I	
24	MIPI_DSI	MIPI_DSI.D1_N	O	
25	MIPI_CSI	MIPI_CSI.D2_N	I	
26	MIPI_DSI	MIPI_DSI.D1_P	O	
27	DGND	DGND	P	
28	DGND	DGND	P	
29	MIPI_CSI	MIPI_CSI.D1_P	I	
30	DGND	DGND	P	
31	MIPI_CSI	MIPI_CSI.D1_N	I	
32	MLB	MLB.C_N	O	
33	DGND	DGND	P	
34	MLB	MLB.C_P	O	
35	MIPI_CSI	MIPI_CSI.D0_P	I	
36	DGND	DGND	P	
37	MIPI_CSI	MIPI_CSI.D0_N	I	
38	MLB	MLB.D_N	I/O	
39	DGND	DGND	P	
40	MLB	MLB.D_P	I/O	
41	DGND	DGND	P	
42	DGND	DGND	P	
43	MIPI_CSI	MIPI_CSI.CLK0_P	I	
44	MLB	MLB.S_N	I/O	
45	MIPI_CSI	MIPI_CSI.CLK0_N	I	
46	MLB	MLB.S_P	I/O	
47	DGND	DGND	P	
48	DGND	DGND	P	
49	DGND	DGND	P	
50	USB_H.PWR	USB_H.PWR	O	Unused USB signal line for USB_H (used for upstream port USB-Hub)
51	ECSPI5	ECSPI5.MISO	I	
52	USB_H.OC	USB_H.OC	I	Unused USB signal line for USB_H (used for upstream port USB-Hub)
53	ECSPI5	ECSPI5.MOSI	O	
54	DGND	DGND	P	
55	ECSPI5	ECSPI5.SS0#	O	
56	DEBUG	SPI-NOR_WP#	I	
57	ECSPI5	ECSPI5.SCLK	O	
58	DEBUG	TAMPER	I	
59	DGND	DGND	P	
60	DGND	DGND	P	

3.2.15 Headers (continued)

Table 60: Pinout header 3 (X29)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	BOOT	BOOT.CFG4_6	I	Pin is not configured in default BSP
8	BOOT	BOOT.CFG4_7	I	Pin is not configured in default BSP
9	DGND	DGND	P	
10	DGND	DGND	P	
11	BOOT	BOOT.CFG4_4	I	Pin is not configured in default BSP
12	BOOT	BOOT.CFG4_5	I	Pin is not configured in default BSP
13	BOOT	BOOT.CFG4_2	I	Pin is not configured in default BSP
14	BOOT	BOOT.CFG4_3	I	Pin is not configured in default BSP
15	DGND	DGND	P	
16	BOOT	BOOT.CFG4_1	I	Pin is not configured in default BSP
17	BOOT	BOOT.CFG4_0	I	Pin is not configured in default BSP
18	DGND	DGND	P	
19	BOOT	BOOT.CFG3_6	I	Pin is not configured in default BSP
20	BOOT	BOOT.CFG3_7	I	Pin is not configured in default BSP
21	BOOT	BOOT.CFG3_4	I	Pin is not configured in default BSP
22	BOOT	BOOT.CFG3_5	I	Pin is not configured in default BSP
23	BOOT	BOOT.CFG3_2	I	Pin is not configured in default BSP
24	BOOT	BOOT.CFG3_3	I	Pin is not configured in default BSP
25	BOOT	BOOT.CFG3_0	I	Pin is not configured in default BSP
26	BOOT	BOOT.CFG3_1	I	Pin is not configured in default BSP
27	DGND	DGND	P	
28	DGND	DGND	P	
29	BOOT	BOOT.CFG2_6	I	Pin is not configured in default BSP
30	BOOT	BOOT.CFG2_7	I	Pin is not configured in default BSP
31	BOOT	BOOT.CFG2_4	I	Pin is not configured in default BSP
32	BOOT	BOOT.CFG2_5	I	Pin is not configured in default BSP
33	BOOT	BOOT.CFG2_2	I	Pin is not configured in default BSP
34	BOOT	BOOT.CFG2_3	I	Pin is not configured in default BSP
35	BOOT	BOOT.CFG2_0	I	Pin is not configured in default BSP
36	BOOT	BOOT.CFG2_1	I	Pin is not configured in default BSP
37	BOOT	BOOT.CFG1_6	I	Pin is not configured in default BSP
38	BOOT	BOOT.CFG1_7	I	Pin is not configured in default BSP
39	BOOT	BOOT.CFG1_4	I	Pin is not configured in default BSP
40	BOOT	BOOT.CFG1_5	I	Pin is not configured in default BSP
41	BOOT	BOOT.CFG1_2	I	Pin is not configured in default BSP
42	BOOT	BOOT.CFG1_3	I	Pin is not configured in default BSP
43	BOOT	BOOT.CFG1_0	I	Pin is not configured in default BSP
44	BOOT	BOOT.CFG1_1	I	Pin is not configured in default BSP
45	DGND	DGND	P	
46	DGND	DGND	P	
47	UART3	UART3.RX	I	
48	–	–	–	
49	UART3	UATR3.TX	O	
50	PWM	PWM3	O	
51	UART3	UART3.RTS#	O	
52	PWM	PWM4	O	
53	UART3	UART3.CTS#	I	
54	DGND	DGND	P	
55	DGND	DGND	P	
56	UART4	UART4.RTS#	O	Unused UART signal line of UART4 (used for RS-485)
57	CCM	CCM_CLKO2	O	
58	DEBUG	RFU	I	Reserved for future use
59	DGND	DGND	P	
60	DGND	DGND	P	

3.2.15 Headers (continued)

Table 61: Pinout header 4 (X30)

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	100 µF + 10 µF + 1 µF to DGND, I_{max} = 1 A
2	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
3	VCC5V	VCC5V	P	10 µF + 1 µF to DGND, I_{max} = 1 A
4	VCC3V3	VCC3V3	P	10 µF + 1 µF to DGND, I_{max} = 1 A
5	DGND	DGND	P	
6	DGND	DGND	P	
7	DGND	DGND	P	
8	DGND	DGND	P	
9	GPIO	GPIO1_IO26	I/O	
10	SPDIF	SPDIF.OUT	O	
11	GPIO	GPIO1_29	I/O	
12	SPDIF	SPDIF.IN	I	
13	GPIO	GPIO1_30	I/O	
14	DGND	DGND	P	
15	GPIO	GPIO2_IO01	I/O	
16	UART5	UART5.RX	I	
17	GPIO	GPIO2_IO02	I/O	
18	UART5	UART5.TX	O	
19	GPIO	GPIO2_IO03	I/O	
20	UART5	UART5.RTS#	O	
21	DGND	DGND	P	
22	UART5	UART5.CTS#	I	
23	GPIO	GPIO2_IO08	I/O	
24	DGND	DGND	P	
25	GPIO	GPIO2_IO23	I/O	
26	I2C3	I2C3.SCL	O	
27	GPIO	GPIO2_IO24	I/O	
28	I2C3	I2C3.SDA	I/O	
29	GPIO	GPIO2_IO25	I/O	
30	DGND	DGND	P	
31	GPIO	GPIO3_IO20	I/O	
32	GPIO	GPIO5_IO18	I/O	
33	GPIO	GPIO3_IO23	I/O	
34	GPIO	GPIO5_IO20	I/O	
35	DGND	DGND	P	
36	GPIO	GPIO5_IO21	I/O	
37	GPIO	GPIO3_IO26	I/O	
38	GPIO	GPIO6_IO08	I/O	
39	GPIO	GPIO3_IO27	I/O	
40	GPIO	GPIO6_IO14	I/O	
41	GPIO	GPIO3_IO28	I/O	
42	DGND	DGND	P	
43	GPIO	GPIO3_IO29	I/O	
44	GPIO	GPIO6_IO16	I/O	With LED
45	GPIO	GPIO4_IO06	I/O	
46	GPIO	GPIO6_IO31	I/O	With LED
47	GPIO	GPIO4_IO07	I/O	
48	GPIO	GPIO4_IO08	I/O	
49	DGND	DGND	P	
50	GPIO	GPIO4_IO09	I/O	
51	SD	SD2.DAT4	I/O	Unused SD signal line of SD2 (used for SD card)
52	DGND	DGND	P	
53	SD	SD2.DAT5	I/O	Unused SD signal line of SD2 (used for SD card)
54	AUD3	AUD3.RXC	I	Unused AUDIO signal line of AUD3 (used for Audio)
55	SD	SD2.DAT6	I/O	Unused SD signal line of SD2 (used for SD card)
56	AUD3	AUD3.RXFS	I	Unused AUDIO signal line of AUD3 (used for Audio)
57	SD	SD2.DAT7	I/O	Unused SD signal line of SD2 (used for SD card)
58	DEBUG	DNC	I	Do not connect
59	DGND	DGND	P	
60	DGND	DGND	P	

3.3 Diagnostic- and user interfaces

3.3.1 Diagnostic LEDs

The MBa6x provides 20 diagnostic LEDs to indicate the system condition.

Table 62: Meaning of diagnostic LEDs

Function	Reference	Colour	Signal
Power	V1	Green	24 V Power-LED (lights up when supply 24 V is active)
	V2	Green	12 V Power-LED (lights up when supply 12 V is active)
	V3	Green	5 V Power-LED (lights up when supply 5 V is active)
	V4	Green	3.3 V Power-LED (lights up when supply 3.3 V is active)
USB	V5	Green	VBUS USB Host 2 (lights up when VBUS of USB Host 2 is active)
	V6	Green	VBUS USB Host 3 (lights up when VBUS of USB Host 3 is active)
	V7	Green	VBUS USB Host 6 (lights up when VBUS of USB Host 6 is active)
	V8	Green	VBUS USB OTG (lights up when VBUS of USB OTG is active)
	V9	Green	VBUS USB Host 7 (LVDS-CMD, lights up when VBUS of USB Host 7 is active)
	V14	Green	VBUS USB Host 4 (header 1, lights up when VBUS of USB Host 4 is active)
Mini PCIe	V10	Green	Mini PCIe WWAN
	V11	Green	Mini PCIe WLAN
	V12	Green	Mini PCIe WPAN
	V13	Green	Mini PCIe 3.3 V Power-LED (lights up when PCIe supply 3.3 V is active)
Ethernet	X11B	Yellow	Activity-LED Ethernet 1000BASE-T (blinks at transfer)
	X11C	Green	Link-LED Ethernet 1000BASE-T (lights up when connected)
	X12B	Yellow	Speed-LED Ethernet 100BASE-T (lights up at 100 Mbit/s, is not lit at 10 Mbit/s)
	X12C	Green	Link-LED Ethernet 100BASE-T (lights up at valid link, blinks at transfer)
GPIOs	V15	Green	GPIO6_IO16 (high-active)
	V16	Green	GPIO6_IO31 (high-active)

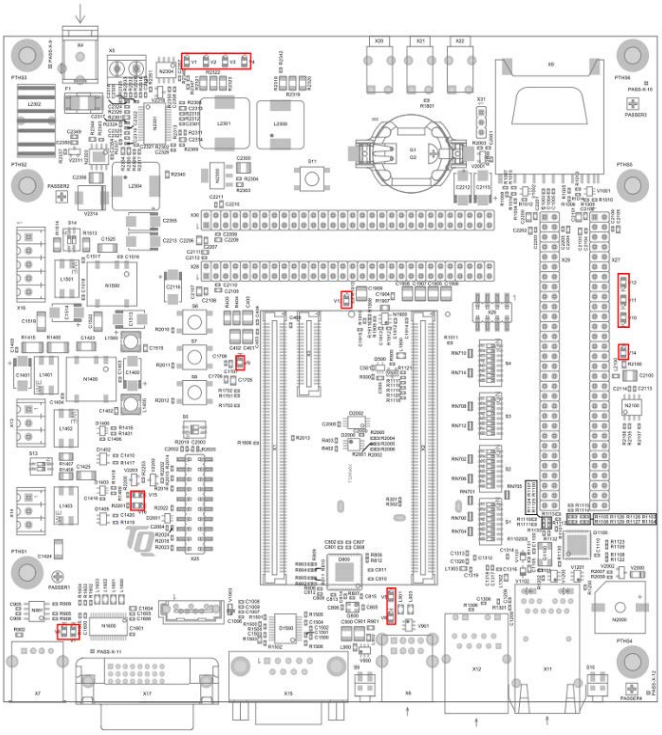


Figure 48: Position of LEDs V1 to V16

3.3.2 GP push buttons

Three general purpose push buttons are available on the MBa6x for development purposes.
The push buttons are not debounced in hardware. They have to be debounced in software, if necessary.

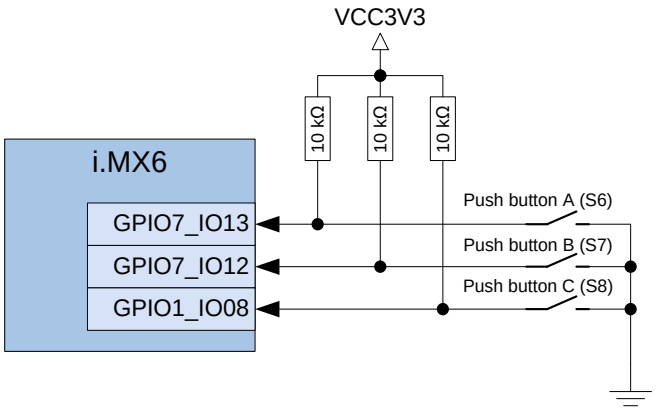


Figure 49: Block diagram GP push buttons

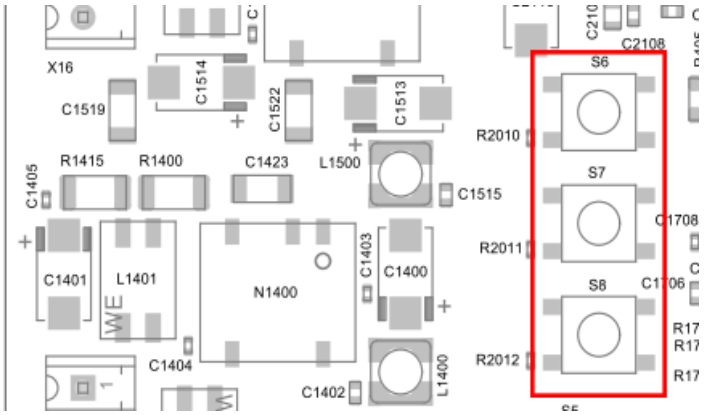


Figure 50: Position of GP push buttons S6, S7, S8

3.3.3 Power-On and Reset-button

For further information see section 3.1.6.

3.3.4 CAN and RS-485 termination

For further information see section 3.2.5 and 3.2.6.

3.3.5 Boot-Mode configuration

The i.MX6 can boot from different media:

- eMMC
- SD-/MMC card
- SATA HDD [19]
- Serial ROM

The setting of switches S1 to S5 determines which device is selected to boot from. [20]
Each signal and its meaning regarding the boot process is to be taken from the TQMa6x User's Manual.

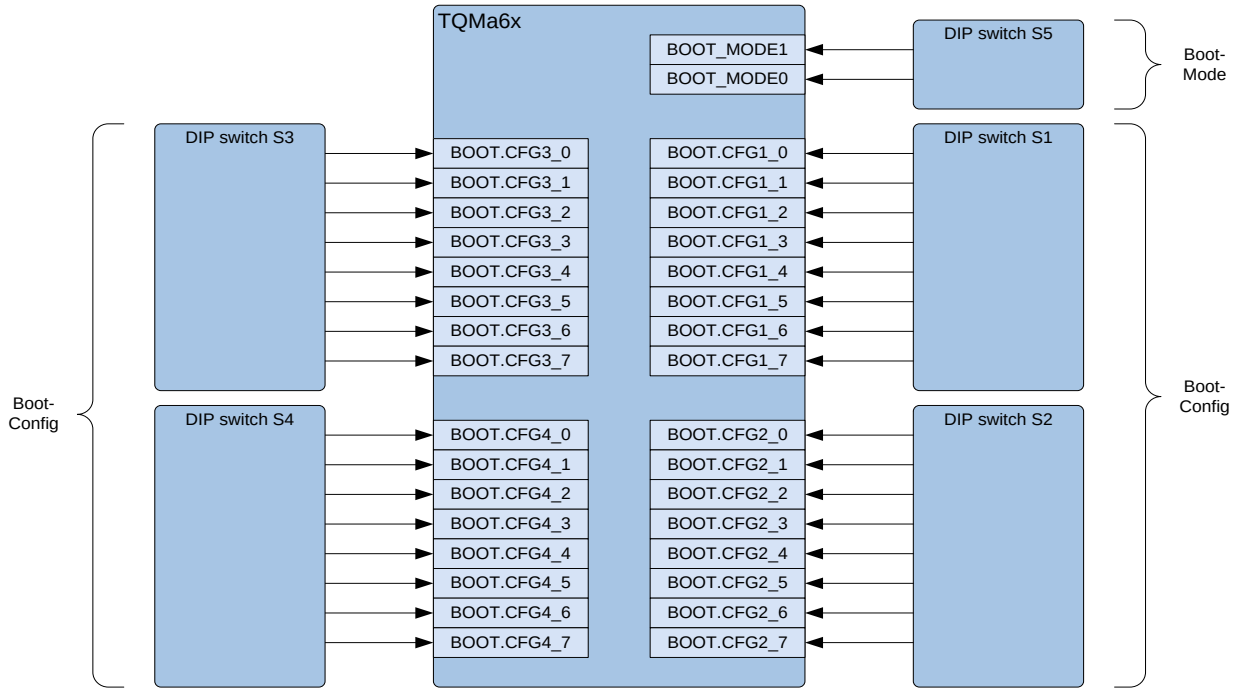


Figure 51: Configuration of boot loader with DIP switches S1 to S5

The following settings can be used as default.

Table 63: Boot-Mode configuration (S5)

Boot-Mode	S5-1 / BOOT.MODE1	S5-2 / BOOT.MODE0
Boot from eFuses	0	0
Serial Downloader	0	1
Internal Boot [21]	1	0
Reserved	1	1

19: Only available with Dual or Quad CPUs.
20: Only applies to modules with unburnt eFuses.
21: Boot configuration is set with DIP switches S2 to S4.

3.3.5 Boot-Mode configuration (continued)

Table 64: Standard boot-configurations (S1, S2, and S4) [22]

BOOT_CFG Group	Bit	DIP switch	eMMC	Serial ROM	SD card	SATA
BOOT_CFG1_[Bit]	7	S1-1	0	0	0	0
	6	S1-2	1	0	1	0
	5	S1-3	1	1	0	1
	4	S1-4	0	1	1	0
	3	S1-5	0	x	0	x
	2	S1-6	x	x	0	x
	1	S1-7	1	x	0	x
	0	S1-8	x	x	0	x
BOOT_CFG2_[Bit]	7	S2-1	0	x	0	x
	6	S2-2	1	x	0	x
	5	S2-3	0	x	1	x
	4	S2-4	1	x	0	0
	3	S2-5	0	x	1	0
	2	S2-6	0	x	x	0
	1	S2-7	0	x	0	0
	0	S2-8	0	x	0	0
BOOT_CFG4_[Bit]	7	S4-1	x	x	x	x
	6	S4-2	x	0	x	x
	5	S4-3	x	0	x	x
	4	S4-4	x	1	x	x
	3	S4-5	x	1	x	x
	2	S4-6	x	0	x	x
	1	S4-7	x	0	x	x
	0	S4-8	x	0	x	x

With S3 settings can be made, which are independent of the boot device.
More information is to be taken from the TQMa6x User's Manual.

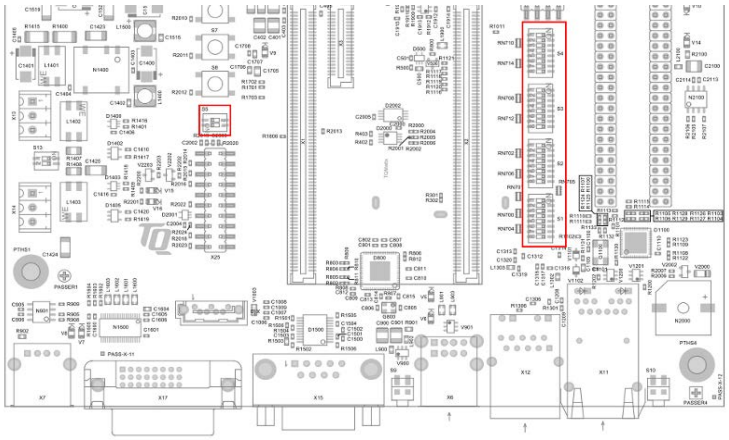


Figure 52: Position of Boot-Mode configuration switches S1, S2, S3, S4, S5

22: Switch setting: 0 = OFF / 1 = ON / x = DONT CARE.

3.3.6 Buzzer

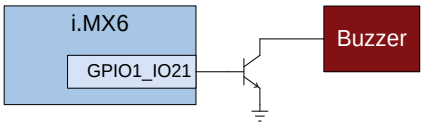


Figure 53: Block diagram buzzer

The MBa6x provides a buzzer to signal acoustic events. The buzzer is directly controlled with a GPIO from the TQMa6x.

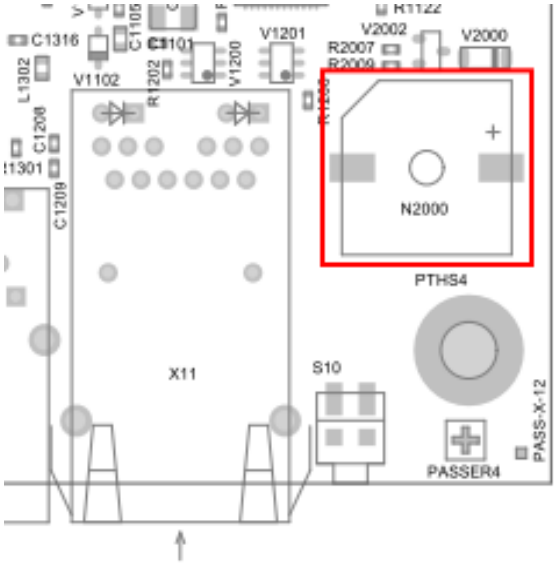


Figure 54: Position of buzzer N2000

3.3.7 PMIC diagnostic interface

The behaviour of the PMIC on the TQMa6x can be changed using the diagnostic interface (X26).
The switching frequency, the output voltages or the work mode can be changed, for example.
Further information is to be taken from the TQMa6x User's Manual (8), or the PMIC data sheet (5).

Attention:	PMIC settings
	The usability of the PMIC diagnostic interface depends on placement options of the TQMa6x. Update of PMIC settings may only be carried out with **extreme care**. Wrong settings can lead to system instabilities or irreparable damage the hardware.

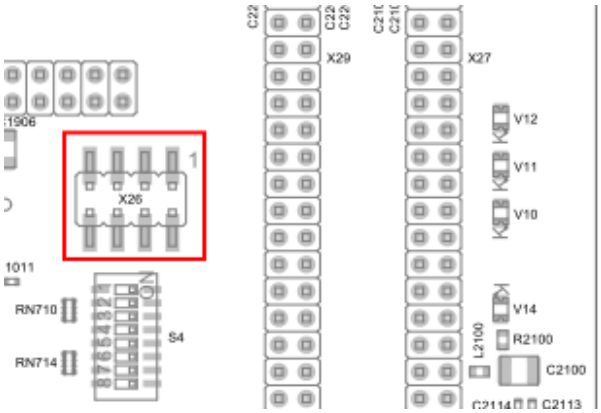


Figure 55: Position of PMIC diagnostic interface X25

Table 65: Pinout PMIC diagnostic interface (X25)

Pin	Pin name	Signal	Dir.	Remark
1	VDD8V25	VDD8V25_OTP	P	Programming voltage for OTP fuses
2	VDD3V3	VDD3V3_OTP	P	Auxiliary 3.3 V supply
3	GND	GND	P	–
4	SCL	SCL_OTP	I	I2C3 Master clock
5	SDA	SDA_OTP	I/O	I2C3 Master data
6	PWRON	PWRON	I	Logic output to turn-on / turn-off the PMIC
7	–	–	–	–
8	–	–	–	–

3.3.8 JTAG

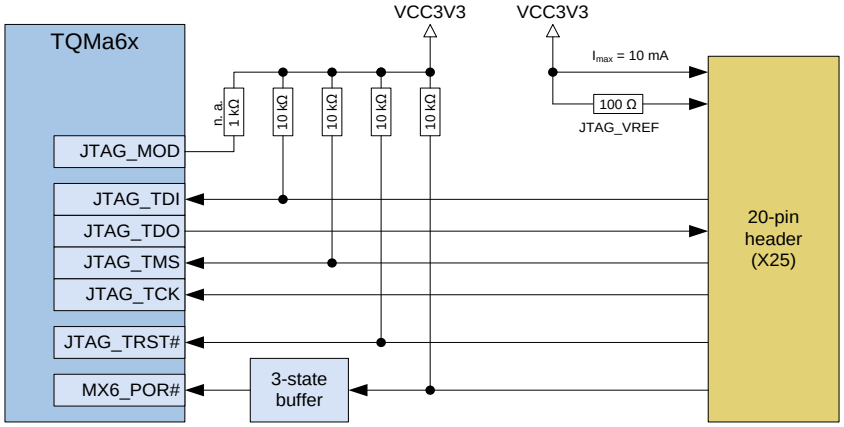


Figure 56: Block diagram JTAG

The JTAG interface is routed to a 20-pin header (X25). The pull-ups for the lines TDI, TMS, TRST# and SRST# are assembled on the MBa6x. All signal lines use 3.3 V as a reference. The JTAG interface has no ESD protection.

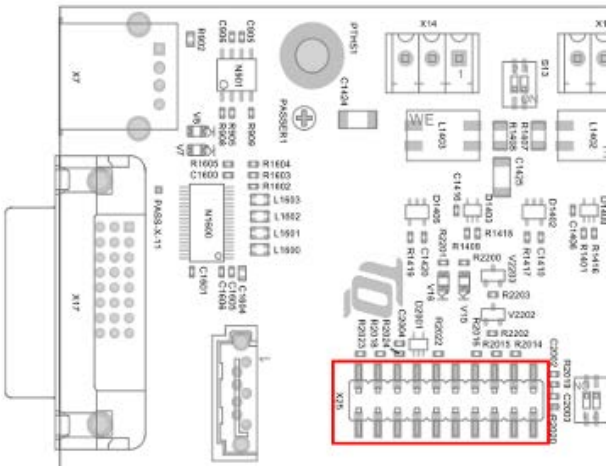


Figure 57: Position of JTAG connector X25

3.3.8 JTAG (continued)

Table 66: Pinout JTAG (X25)

Pin	Pin name	Signal	Dir.	Remark
1	VREF	JTAG.VREF	P	100 Ω in series to VCC3V3, use only as reference
2	VSUPPLY	VCC3V3	P	0 Ω in series to VCC3V3, I_{max} = 10 mA
3	TRST#	JTAG.TRST#	I	10 kΩ Pull-Up to VCC3V3
4	DGND	DGND	P	
5	TDI	JTAG.TDI	I	10 kΩ Pull-Up to VCC3V3
6	DGND	DGND	P	
7	TMS	JTAG.TMS	I	10 kΩ Pull-Up to VCC3V3
8	DGND	DGND	P	
9	TCK	JTAG.TCK	I	
10	DGND	DGND	P	
11	DGND	DGND	P	10 kΩ in series to DGND
12	DGND	DGND	P	
13	TDO	JTAG.DTO	O	
14	DGND	DGND	P	
15	SRST#	JTAG.SRST#	I	10 kΩ Pull-Up to VCC3V3; open drain buffer at MX6_POR#
16	DGND	DGND	P	
17	VCC3V3	VCC3V3	P	
18	DGND	DGND	P	
19	DBGACK	DGND	P	10 kΩ in series to DGND
20	DGND	DGND	P	

4. MECHANICS

4.1 Dimensions

The design of the MBa6x is based on the Mini-ITX form factor (170 × 170 mm²) and has a maximum height of approximately 24 mm. The MBa6x has six 4.3 mm holes for mounting in a housing and weighs approximately 260 grams without TQMa6x.

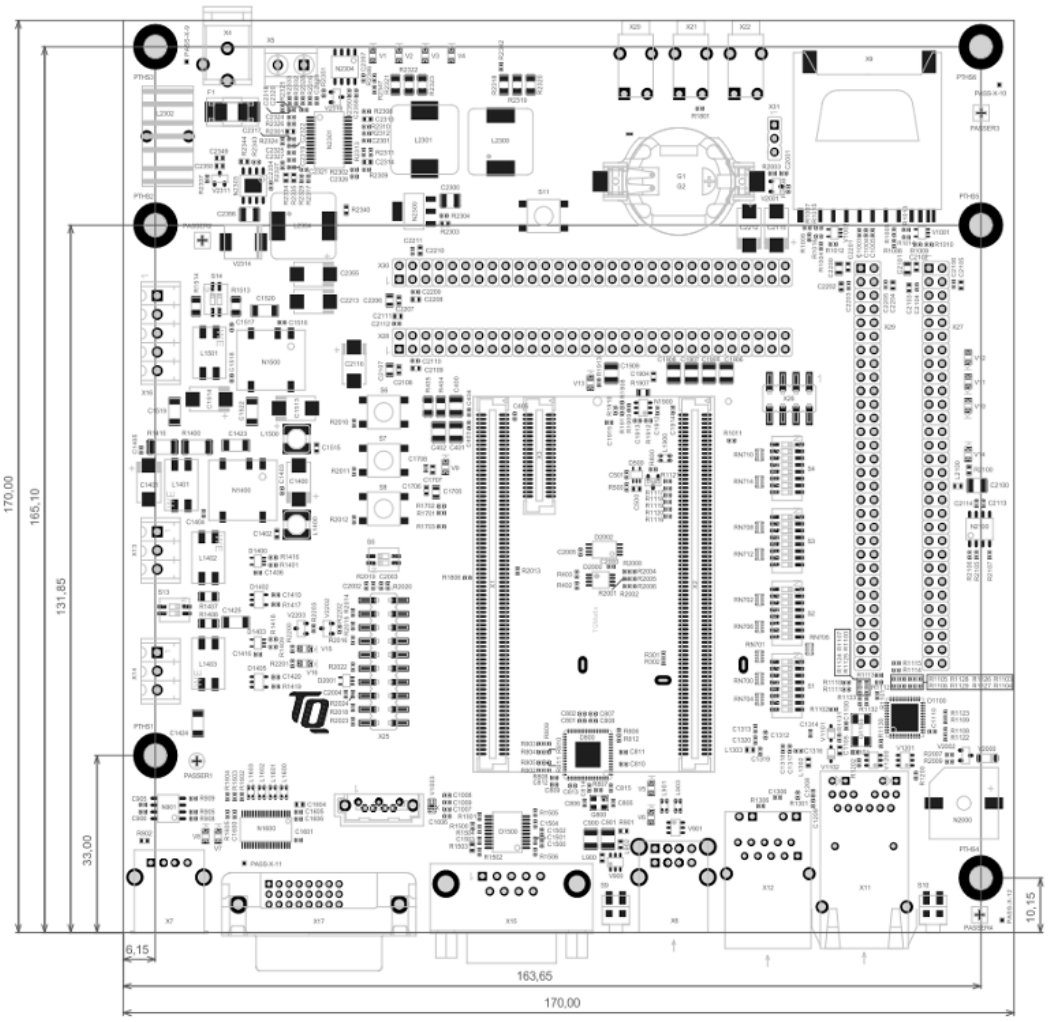


Figure 58: MBa6x dimensions

4.2 Thermal management

No special precautions were taken concerning the thermal management of the MBa6x.
Cooling the TQMa6x may be necessary depending on the software or the TQMa6x used (Solo/Dual/Quad).
More information is to be taken from the TQMa6x User's Manual.

4.3 Assembly

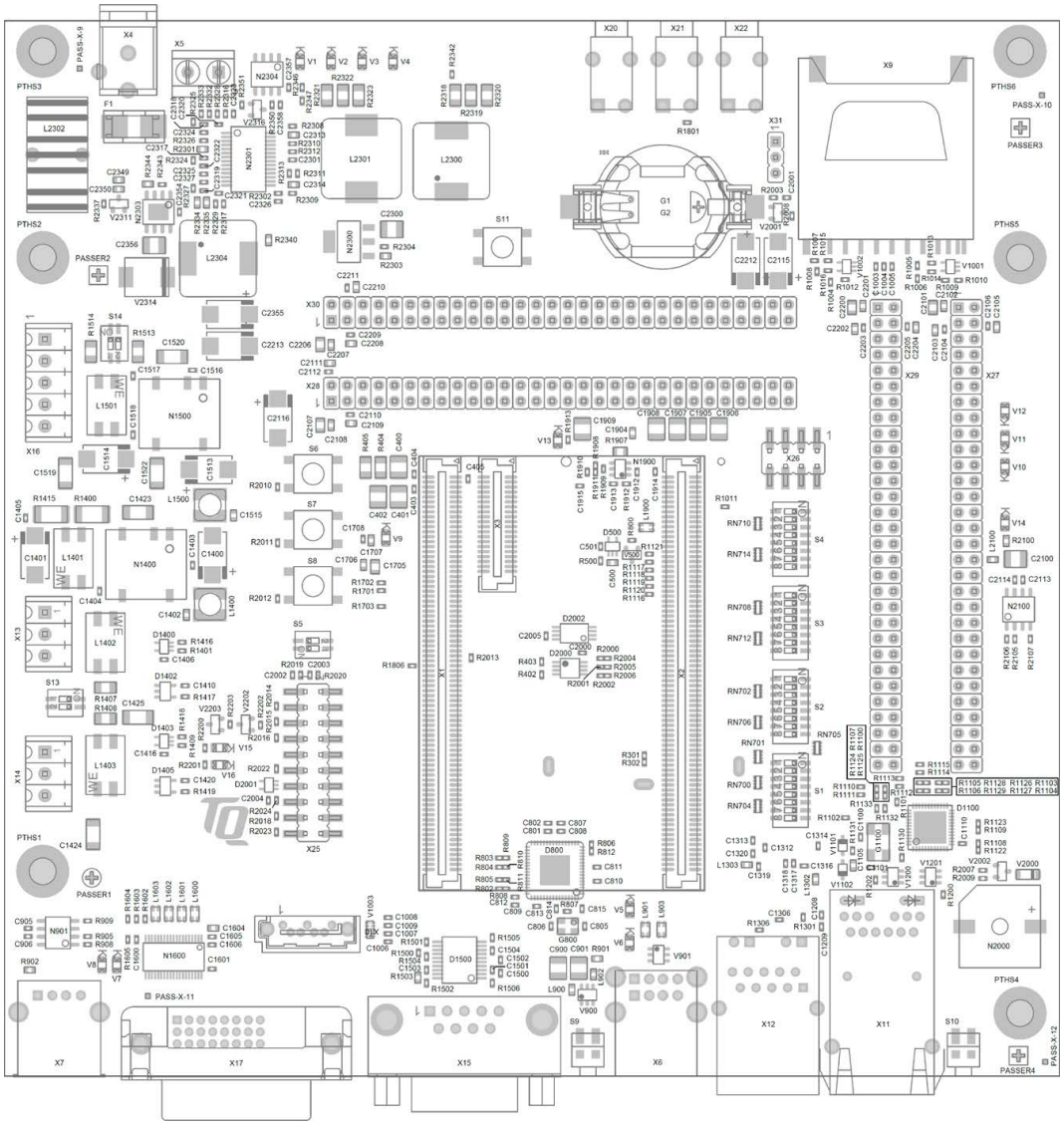


Figure 59: MBa6x, component placement top

4.3 Assembly (continued)

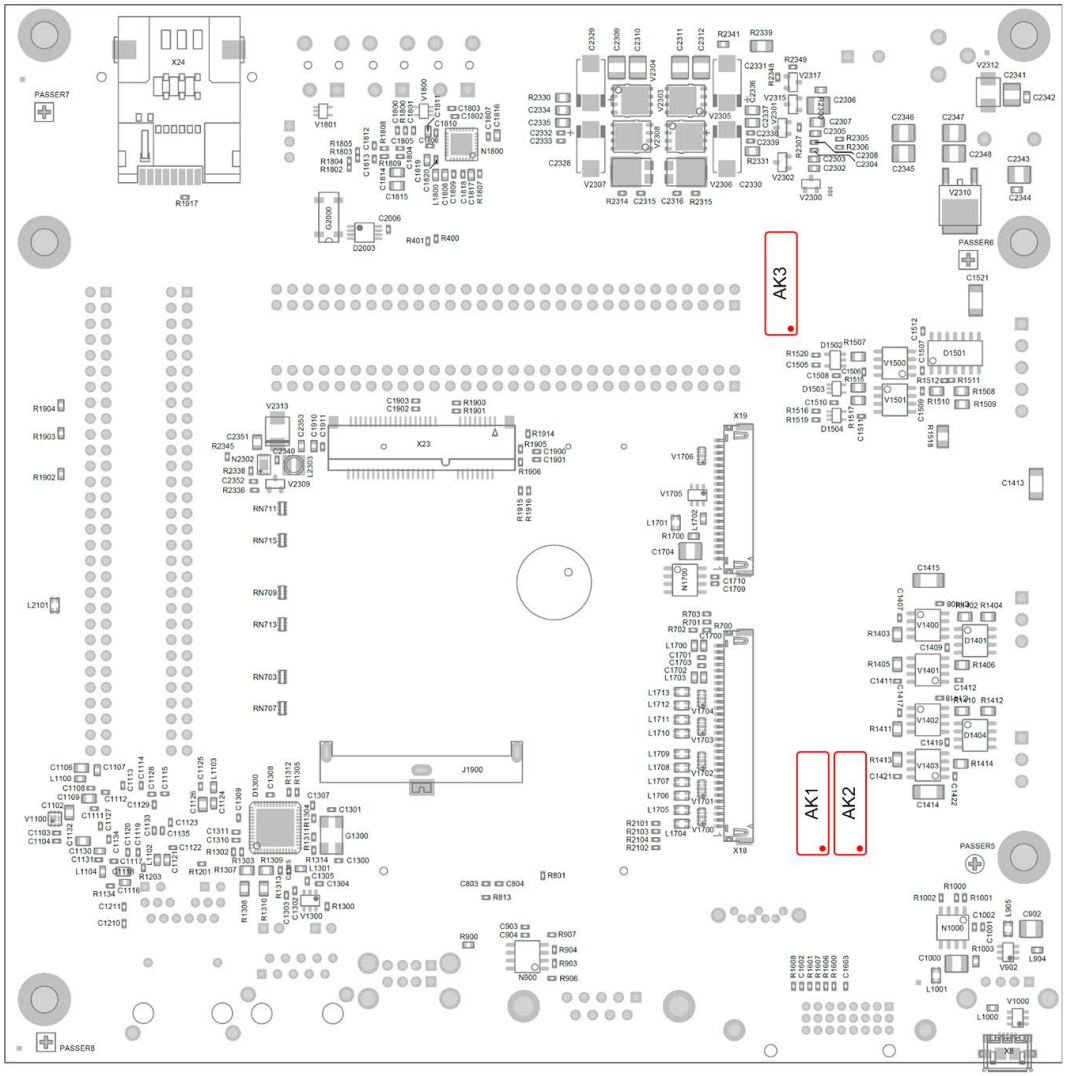


Figure 60: MBa6x, component placement bottom

The labels on the MBa6x revision 02xx show the following information:

Table 67: Labels on MBa6x

Label	Content
AK1	Serial number
AK2	MBa6x version and revision, tests performed
AK3	MAC address

5. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

5.1 EMC

Because the MBa6x is a development platform, no EMC specific tests have been carried out.
During the development of the MBa6x the following standard was taken into account:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 55022 A1:2007.

5.2 ESD

Most of the interfaces on the MBa6x are protected against electrostatic discharge. [23]
The interfaces, which provide an ESD protection is to be taken from the circuit diagram.

5.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety have not been carried out.

6. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 68: Climatic and operational conditions MBa6x (without TQMa6x)

Parameter	Range	Remark
Ambient temperature	0 °C to +70 °C	Without Lithium battery CR2032
Ambient temperature	0 °C to +60 °C	With Lithium battery CR2032
Storage temperature	–10 °C to +60 °C	With Lithium battery CR2032
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

6.1 Protection against external effects

Protection class IP00 was defined for the MBa6x. There is no protection against foreign objects, touch or humidity.

6.2 Reliability and service life

No detailed MTBF calculation was performed for the MBa6x.
The MBa6x is designed to be insensitive to vibration and impact.
High quality industrial grade connectors are assembled on the MBa6x.

23: The JTAG and PMIC interfaces do not provide ESD protection.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The MBa6x is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa6x was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa6x must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBa6x enable compliance with EuP requirements for the MBa6x.

7.5 Packaging

The MBa6x is delivered in reusable packaging.

7.6 Batteries

7.6.1 General notes

Due to technical reasons a battery is necessary for the MBa6x. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

7.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa6x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa6x is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 69: Acronyms

Acronym	Meaning
ADR	Accord européen relatif au transport international des marchandises Dangereuses par Route
AHCI	Advanced Host Controller Interface
AMBA	Advanced Microcontroller Bus Architecture
ARM®	Advanced RISC Machine
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDC	Display Data Channel
DDR3	Double Data Rate 3
DIN	Deutsche Industrie Norm
DIP	Dual In-line Package
DNC	Do Not Connect
DSI	Display Serial Interface
DVI	Digital Visual Interface
DVI-D	Digital Visual Interface-Digital
ECSPI	Enhanced Capability Serial Peripheral Interface
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
EuP	Energy using Products
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
HP_L / HP_R	Headphone Left / Right
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
IPD	Input with Pull-Down (resistor)
IPU	Input with Pull-Up (resistor)
JTAG®	Joint Test Action Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signalling
MAC	Media Access Control
MIC	Microphone
MII	Media-Independent Interface

8.1 Acronyms and definitions (continued)

Table 69: Acronyms (continued)

Acronym	Meaning
MIPI	Mobile Industry Processor Interface
MLB	Media Local-Bus
MMC	Multimedia Card
MSB	Most Significant Bit
MTBF	Mean (operating) Time Between Failures
n.a.	Not Assembled
NC	Not Connected
OPU	Output with Pull-Up
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SATA	Serial ATA
SD	Secure Digital
SD/MMC	Secure Digital Multimedia Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMD	Surface-Mounted Device
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TCP	Transmission Control Protocol
THD	Through-Hole Device
THT	Through-Hole Technology
TMDS	Transition-Minimized Differential Signalling
UART	Universal Asynchronous Receiver/Transmitter
U-Boot	Universal Bootloader
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

8.2 References

Table 70: Further applicable documents

No.	Name	Rev., Date	Company
(1)	IMX6SDLRM	Rev. 2, 04/2015	NXP
(2)	IMX6DQRM	Rev. 3, 07/2015	NXP
(3)	IMX6SDLCE	Rev. 5, 12/2014	NXP
(4)	IMX6DQCE	Rev. 5, 06/2015	NXP
(5)	MMPF0100	Rev. 11.0, 08/2015	NXP
(6)	KSZ9031 Errata Sheet	11/2012	Micrel
(7)	TQMa6x User's Manual	– current –	TQ-Systems
(8)	TQMa6x Support-Wiki	– current –	TQ-Systems
(9)	TQMa6x-MBa6x_Tech Note	– current –	TQ-Systems

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