MBa6ULx
User's Manual

MBa6ULx UM 0103
02.04.2019

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TABLE DIRECTORY

TABLE DIRECTORY (continued)

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	16.01.2018	Petz		Initial release
0101	10.02.2018	Petz	All Illustration 1, Table 3, Table 14 Table 2 Table 23, Table 45 Table 44 4.2.7, 5.1, 5.2, 7.2	Typo, formatting and expression Updated Updated, footnote 1 added Signal names corrected ON / OFF changed Updated
0102	26.10.2018	Petz	All	Formatting, links updated
0103	02.04.2019	Petz	Table 61 Table 62 Footnote 18	Signals at pins 17, 19 corrected Signals at pins 25, 44, 50 corrected Added

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa6ULx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa6ULx circuit diagram
- TQMa6ULx User's Manual
- IMX6ULRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma6ulx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa6ULx Rev. ≥0200.
The MBa6ULx is designed as a carrier board for the TQMa6ULx.
The LGA version (TQMa6ULxL) can also be used with an adapter on the MBa6ULx.
The illustrations in this User's Manual also refer to the TQMa6ULx.
All interfaces of the TQMa6ULx are available on the MBa6ULx. The characteristics of the i.MX6ULx can be evaluated, and therefore the software development for a TQMa6ULx / TQMa6ULxL project can start immediately.
The MBa6ULx supports all TQMa6ULx with i.MX6UL1, i.MX6UL2, and i.MX6UL3 CPU.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 MBa6ULx Block diagram

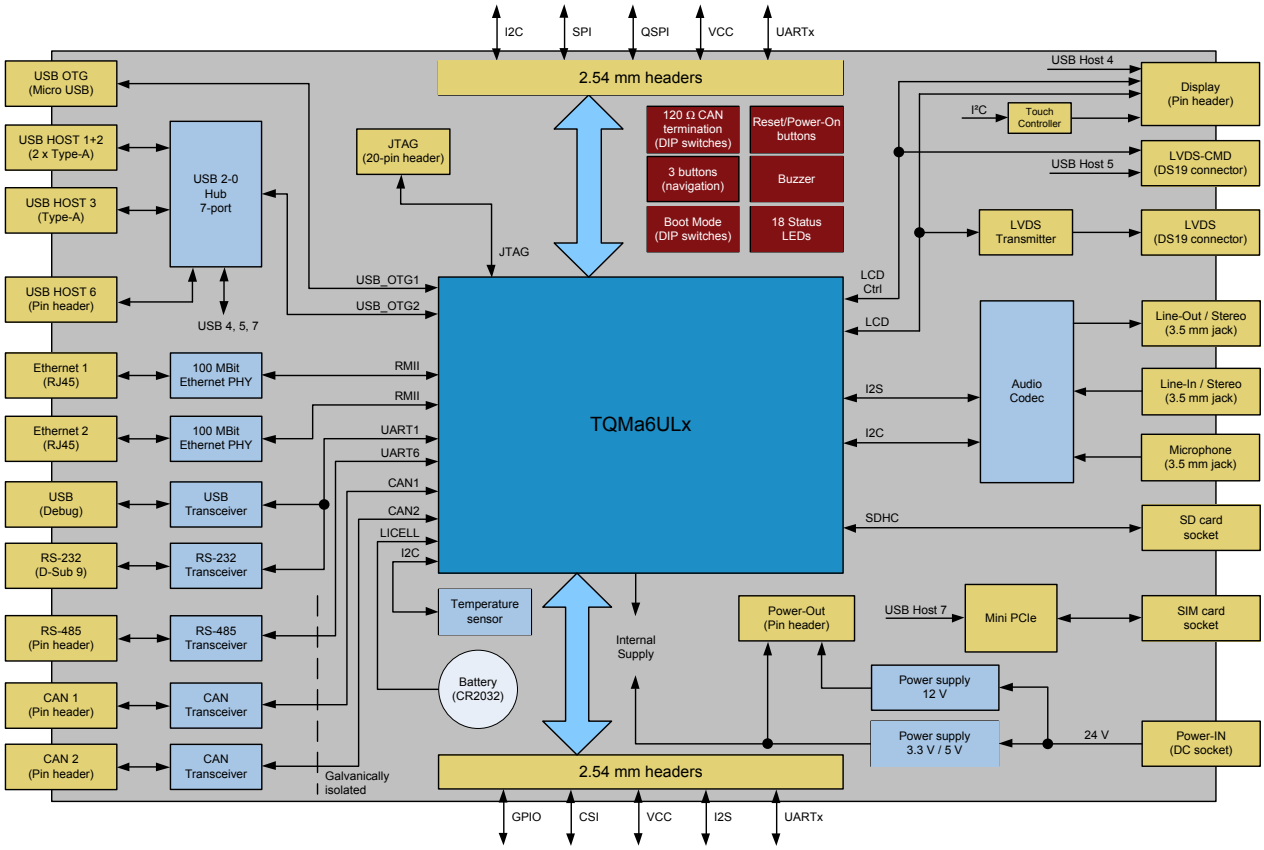


Illustration 1: Block diagram MBa6ULx

3.1.2 Functionality

Core of the system is the TQMa6ULx / TQMa6ULxL with an NXP i.MX6ULx CPU.

In addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, LVDS etc. all other available TQMa6ULx signals are routed to 100 mil headers.

The MBa6ULx provides the following interfaces and functions:

Table 2: Overview interfaces

Interface	Qty.	Type of connector	Remark
USB 2.0 Hi-Speed host	2	USB receptacle Type-A	Dual port receptacle, right angle
USB 2.0 Hi-Speed host	1	USB receptacle Type-A	Single port receptacle, right angle
USB 2.0 Hi-Speed host	1	100 mil header	–
USB 2.0 Hi-Speed OTG	1	USB receptacle Micro-AB	–
USB 2.0 Debug	1	USB receptacle Micro-AB	–
Ethernet 10/100BASE-T	2	RJ45 receptacle	Receptacle with integrated magnetics
CAN	2	Phoenix basic housing	Straight version, CAN gal. separated
RS-485	1	Phoenix basic housing	Straight version, RS-485 gal. separated
RS-232	1	D-Sub 9-pin connector	Right angle, Debug-UART1
LVDS	1	DF19 receptacle	LVDS data
LVDS-CMD	1	DF19 receptacle	LVDS control signals
Audio	3	3.5 mm jack	1 × Line-out (stereo) 1 × Line-in (stereo) 1 × Microphone (mono)
SD card	1	Push-Pull-Type	–
PCIe	1	Mini PCIe	–
	1	SIM card holder	–
Headers	3	Header, 100 mil pitch	3.3 V @ 2 A, 5 V @ 2 A, 12 V @ 3 A Parallel LCD interface 2 × CAN 1 × eMMC interface [1] 2 × I^2C 1 × QSPI 1 × RESET_IN# 1 × RESET_OUT# 1 × WDOG 1 × Buzzer 1 × Ext. wakeup 1 × MX6UL_ONOFF 1 × PMIC_PWRON 1 × TEMP_OS# 1 × SAI 10 × TAMPER 1 × ECSPI 4 × Touch signal 3 × UART 2 × USB-HOST
Power-IN	1	DC jack (2.5 mm / 5.5 mm)	V_{IN} = 24 V DC ±5 %
	1	DC jack 2-pin (screw terminals)	
Battery holder	1	CR2032 holder	Backup battery RTC

Table 3: Overview diagnostic and user's interfaces

Interface	Qty.	Component	Remark
Status	22	Chip LEDs	Power-LEDs, LEDs at GPIOs, Eth-activity/speed
Temperature	1	Temperature sensor	SE97BTP
Power	1	Push button	CPU-ONOFF/PMIC-Reset
Reset	1	Push button	CPU-RESET
Ext. wakeup	1	Push button	EXT_WAKEUP
Navigation	3	Push button	–
Boot-Mode configuration	18	DIP switch	–
CAN- and RS-485 termination	4	DIP switch	–
Signal generator	1	Buzzer	Connected to GPIO expander
JTAG	1	20-pin header, 100 mil pitch	–

1: Interface only available on TQMa6ULx without eMMC.

4. ELECTRONICS

4.1 System components

4.1.1 TQMa6ULx

4.1.1.1 Overview TQMa6ULx

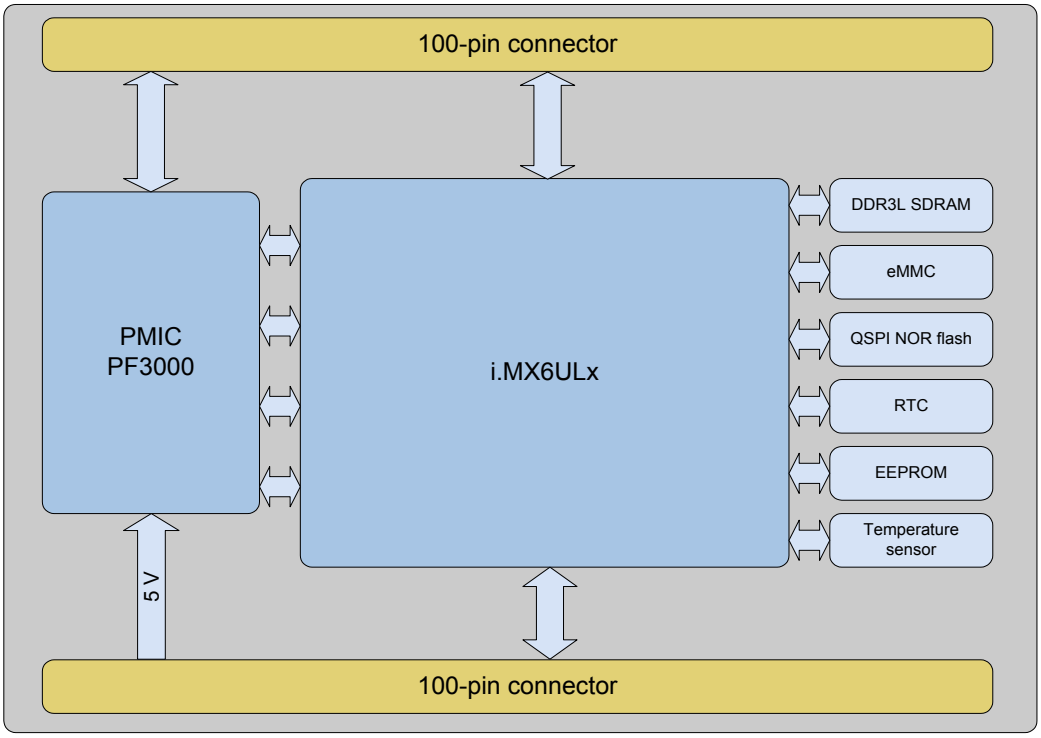


Illustration 2: Block diagram TQMa6ULx

The TQMa6ULx with the i.MX6ULx CPU is the central system component. It provides DDR3L SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMa6ULx are derived from the supply voltage of 5 V. More information is to be taken from the accompanying User's Manual of the TQMa6ULx (8).

The boot behaviour of the TQMa6ULx can be customised. The required Boot-Mode configuration can be set with DIP switches on the MBa6ULx, see chapter 4.3.5.

4.1.1.2 Pinout X1, X2

All signals and interfaces are routed via two connectors form the TQMa6ULx onto the MBa6ULx.

The pins assignment listed in Table 4 and Table 5 refers to the BSP provided by TQ-Systems GmbH.

Note:	TQMa6ULx interfaces
	Depending on the selected TQMa6ULx, not all interfaces are available. Available interfaces are to be taken from the pinout table in the TQMa6ULx User's Manual.

Table 4: Pinout connector X1

CPU ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	CPU ball
–	P	5 V	Power	VCC5V	1	2	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	3	4	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	5	6	VCC5V	Power	5 V	P	–
–	P	0 V	Ground	DGND	7	8	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	9	10	LICELL [2]	Power	3.3 V	P	–
–	P	1.8 V	Power	VCC1V8_OUT	11	12	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	13	14	VCC3V3_V33_OUT	Power	3.3 V	P	–
–	P	3.0 V	Power	VSNVS_REF_OUT	15	16	DGND	Ground	0 V	P	–
–	P	3.3 V	Power	VCC3V3_REF_OUT	17	18	VCC2V5_OUT	Power	2.5 V	P	–
–	P	0 V	Ground	DGND	19	20	DGND	Ground	0 V	P	–
–	P	0.675 V	Power	VCCDDR_OUT	21	22	VCCCORE_OUT	Power	1.4 V	P	–
–	P	0 V	Ground	DGND	23	24	DGND	Ground	0 V	P	–
F4	P	1.8 / 3.3 V [3]	Power	NVCC_CSI	25	26	NVCC_ENET	Power	2.5 / 3.3 V [4]	P	F13
–	P	0 V	Ground	DGND	27	28	DGND	Ground	0 V	P	–
P17	O	2.5 V	CCM	CCM_CLK1_P	29	30	DGND	Ground	0 V	P	–
P16	O	2.5 V	CCM	CCM_CLK1_N	31	32	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	33	34	DGND	Ground	0 V	P	–
R8	I	3.3 V	Config	MX6ULx_ONOFF	35	36	USB_OTG2_OC	USB	3.3 V	I	L17
T9	I	3.3 V	Config	PMIC_PWRON	37	38	USB_OTG2_PWR	USB	3.3 V	O	L14
–	P	0 V	Ground	DGND	39	40	DGND	Ground	0 V	P	–
U16	O	Open-Drain	USB	USB_OTG1_CHD#	41	42	USB_OTG2_VBUS	Power	5 V	P	U12
–	P	0 V	Ground	DGND	43	44	USB_OTG2_ID	USB	3.3 V	I	M17
T12	P	5 V	Power	USB_OTG1_VBUS	45	46	DGND	Ground	0 V	P	–
K13	I	3.3 V	USB	USB_OTG1_ID	47	48	USB_OTG2_DN	USB	3 V	I/O	T13
L15	I	3.3 V	USB	USB_OTG1_OC	49	50	USB_OTG2_DP	USB	3 V	I/O	U13
M16	O	3.3 V	USB	USB_OTG1_PWR	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	UART3_RX_DATA	UART	3.3 V	I	H16
T15	I/O	3 V	USB	USB_OTG1_DN	55	56	UART3_TX_DATA	UART	3.3 V	O	H17
U15	I/O	3 V	USB	USB_OTG1_DP	57	58	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	59	60	BOOT_MODE0	Boot	3.0 V [5]	I	T10
N8	I	3.3 V	SNVS	SNVS_TAMPER5	61	62	BOOT_MODE1	Boot	3.0 V [5]	I	U10
N11	I	3.3 V	SNVS	SNVS_TAMPER6	63	64	DGND	Ground	0 V	P	–
N10	I	3.3 V	SNVS	SNVS_TAMPER7	65	66	SNVS_TAMPER0	SNVS	3.3 V	I	R10
N9	I	3.3 V	SNVS	SNVS_TAMPER8	67	68	SNVS_TAMPER1	SNVS	3.3 V	I	R9
R6	I	3.3 V	SNVS	SNVS_TAMPER9	69	70	SNVS_TAMPER2	SNVS	3.3 V	I	P11
–	P	0 V	Ground	DGND	71	72	SNVS_TAMPER3	SNVS	3.3 V	I	P10
M14	I	3.3 V	JTAG	JTAG_TCK	73	74	SNVS_TAMPER4	SNVS	3.3 V	I	P9
P14	I	3.3 V	JTAG	JTAG_TMS	75	76	DGND	Ground	0 V	P	–
N16	I	3.3 V	JTAG	JTAG_TDI	77	78	JTAG_TDO	JTAG	3.3 V	O	N15
–	P	0 V	Ground	DGND	79	80	JTAG_TRST#	JTAG	3.3 V	I	N14
M15	I/O	3.3 V	GPIO	GPIO1_IO09	81	82	JTAG_MOD	JTAG	3.3 V	I	P15
K15	O	3.3 V	SD	USDHC1_WP [6]	83	84	DGND	Ground	0 V	P	–
J14	I	3.3 V	SD	USDHC1_CD# [7]	85	86	UART1_RX_DATA	UART	3.3 V	I	K16
J16		3.3 V	I2C	I2C4_SDA	87	88	UART1_TX_DATA	UART	3.3 V	O	K14
J17		3.3 V	I2C	I2C4_SCL	89	90	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	91	92	CAN2_RX	CAN	3.3 V	I	H14
N17	O	3.3 V	Config	WDOG1#	93	94	CAN2_TX	CAN	3.3 V	O	J15
P8	I	3.3 V	Config	RESET_IN#	95	96	CAN1_RX	CAN	3.3 V	I	G14
–	O	3.3 V	Config	RESET_OUT#	97	98	CAN1_TX	CAN	3.3 V	O	H15
–	P	0 V	Ground	DGND	99	100	DGND	Ground	0 V	P	–

2: LICELL can be left open, if RTC backup or other functions of the SNVS domain are not required (see NXP documentation).
3: 1.8 V, if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V, if NVCC_CSI is connected to VCC3V3_V33_OUT.
4: 2.5 V, if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V, if NVCC_ENET is connected to VCC3V3_REF_OUT.
5: Use VSNVS_REF_OUT as reference voltage for BOOT-CFG resistors.
6: TQMa6ULx revision 02xx: GPIO; TQMa6ULx revision 03xx: USDHC1_WP.
7: TQMa6ULx revision 02xx: GPIO; TQMa6ULx revision 03xx: USDHC1_CD#.

Table 5: Pinout connector X2

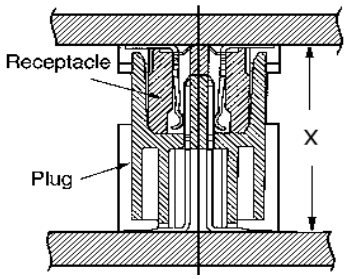
CPU ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	CPU ball
–	P	0 V	Ground	DGND	1	2	DGND	Ground	0 V	P	–
G16	O	3.3 V	SPI	SPI2_SS0#	3	4	SPI2_MISO	SPI	3.3 V	I	G13
G17	O	3.3 V	SPI	SPI2_SCLK	5	6	SPI2_MOSI	SPI	3.3 V	O	F17
F15	O	2.5 / 3.3 V [8]	ENET	ENET1_TX_EN	7	8	DGND	Ground	0 V	P	–
F14	O	2.5 / 3.3 V [8]	ENET	ENET1_TX_CLK	9	10	ENET_MGMT_MDC	ENET	2.5 / 3.3 V [8]	O	L16
–	P	0 V	Ground	DGND	11	12	ENET_MGMT_MDIO	ENET	2.5 / 3.3 V [8]	I/O	K17
E15	O	2.5 / 3.3 V [8]	ENET	ENET1_TDATA0	13	14	ENET2_TX_CLK	ENET	2.5 / 3.3 V [8]	O	D17
E14	O	2.5 / 3.3 V [8]	ENET	ENET1_TDATA1	15	16	DGND	Ground	0 V	P	–
F16	I	2.5 / 3.3 V [8]	ENET	ENET1_RDATA0	17	18	ENET2_RX_ER	ENET	2.5 / 3.3 V [8]	I	D16
E17	I	2.5 / 3.3 V [8]	ENET	ENET1_RDATA1	19	20	ENET2_RDATA1	ENET	2.5 / 3.3 V [8]	I	C16
E16	I	2.5 / 3.3 V [8]	ENET	ENET1_RX_EN	21	22	ENET2_RDATA0	ENET	2.5 / 3.3 V [8]	I	C17
D15	I	2.5 / 3.3 V [8]	ENET	ENET1_RX_ER	23	24	ENET2_RX_EN	ENET	2.5 / 3.3 V [8]	I	B17
–	P	0 V	Ground	DGND	25	26	ENET2_TX_EN	ENET	2.5 / 3.3 V [8]	O	B15
B16	I/O	3.3 V [9]	LCD	LCD_DATA23	27	28	ENET2_TDATA0	ENET	2.5 / 3.3 V [8]	O	A15
A14	I/O	3.3 V [9]	LCD	LCD_DATA22	29	30	ENET2_TDATA1	ENET	2.5 / 3.3 V [8]	O	A16
B14	I/O	3.3 V [9]	LCD	LCD_DATA21	31	32	DGND	Ground	0 V	P	–
C14	I/O	3.3 V [9]	LCD	LCD_DATA20	33	34	LCD_DATA15	LCD	3.3 V [9]	I/O	D13
–	P	0 V	Ground	DGND	35	36	LCD_DATA14	LCD	3.3 V [9]	I/O	A12
D14	I/O	3.3 V [9]	LCD	LCD_DATA19	37	38	LCD_DATA13	LCD	3.3 V [9]	I/O	B12
A13	I/O	3.3 V [9]	LCD	LCD_DATA18	39	40	LCD_DATA12	LCD	3.3 V [9]	I/O	C12
B13	I/O	3.3 V [9]	LCD	LCD_DATA17	41	42	DGND	Ground	0 V	P	–
C13	I/O	3.3 V [9]	LCD	LCD_DATA16	43	44	LCD_DATA11	LCD	3.3 V [9]	I/O	D12
–	P	0 V	Ground	DGND	45	46	LCD_DATA10	LCD	3.3 V [9]	I/O	E12
D11	I/O	3.3 V [9]	LCD	LCD_DATA07	47	48	LCD_DATA09	LCD	3.3 V [9]	I/O	A11
A10	I/O	3.3 V [9]	LCD	LCD_DATA06	49	50	LCD_DATA08	LCD	3.3 V [9]	I/O	B11
B10	I/O	3.3 V [9]	LCD	LCD_DATA05	51	52	DGND	Ground	0 V	P	–
C10	I/O	3.3 V [9]	LCD	LCD_DATA04	53	54	LCD_CLK	LCD	3.3 V [9]	O	A8
–	P	0 V	Ground	DGND	55	56	DGND	Ground	0 V	P	–
D10	I/O	3.3 V [9]	LCD	LCD_DATA03	57	58	LCD_ENABLE	LCD	3.3 V [9]	O	B8
E10	I/O	3.3 V [9]	LCD	LCD_DATA02	59	60	LCD_RESET	LCD	3.3 V [9]	O	E9
A9	I/O	3.3 V [9]	LCD	LCD_DATA01	61	62	LCD_HSYNC	LCD	3.3 V [9]	O	D9
B9	I/O	3.3 V [9]	LCD	LCD_DATA00	63	64	LCD_VSYNC	LCD	3.3 V [9]	I/O	C9
–	P	0 V	Ground	DGND	65	66	QSPI_A_DATA0	QSPI	3.3 V	I/O	A3
B3	I/O	3.3 V	SD	SD1_DATA0	67	68	QSPI_A_DATA1	QSPI	3.3 V	I/O	C5
B2	I/O	3.3 V	SD	SD1_DATA1	69	70	QSPI_A_DATA2	QSPI	3.3 V	I/O	B5
B1	I/O	3.3 V	SD	SD1_DATA2	71	72	QSPI_A_DATA3	QSPI	3.3 V	I/O	A4
A2	I/O	3.3 V	SD	SD1_DATA3	73	74	QSPI_A_SS1#	QSPI	3.3 V	O	A5
C2	I/O	3.3 V	SD	SD1_CMD	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	QSPI_A_SCK	QSPI	3.3 V	O	D5
C1	O	3.3 V	SD	SD1_CLK	79	80	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	81	82	QSPI_A_SS0#	QSPI	3.3 V	O	E6
E4	I/O	1.8 / 3.3 V [10]	GPIO	GPIO4_IO21	83	84	DGND	Ground	0 V	P	–
E3	I/O	1.8 / 3.3 V [10]	GPIO	GPIO4_IO22	85	86	GPIO4_IO25	GPIO	1.8 / 3.3 V [10]	I/O	D4
–	P	0 V	Ground	DGND	87	88	GPIO4_IO26	GPIO	1.8 / 3.3 V [10]	I/O	D3
E2	I/O	1.8 / 3.3 V [10]	GPIO	GPIO4_IO23	89	90	GPIO4_IO27	GPIO	1.8 / 3.3 V [10]	I/O	D2
E1	I/O	1.8 / 3.3 V [10]	GPIO	GPIO4_IO24	91	92	GPIO4_IO28	GPIO	1.8 / 3.3 V [10]	I/O	D1
–	I	–	RFU	RFU1	93	94	DGND	Ground	0 V	P	–
F3	O	3.3 V	I²C	I2C2_SCL	95	96	UART6_RX_DATA	UART	3.3 V	I	E5
F2	I/O	3.3 V	I²C	I2C2_SDA	97	98	UART6_TX_DATA	UART	3.3 V	O	F5
–	P	0 V	Ground	DGND	99	100	DGND	Ground	0 V	P	–

8: 2.5 V, if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V, if NVCC_ENET is connected to VCC3V3_REF_OUT.
9: Use VCC3V3_REF_OUT as reference voltage for BOOT-CFG resistors.
10: 1.8 V, if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V, if NVCC_CSI is connected to VCC3V3_V33_OUT.

4.1.1.3 Connectors on MBa6ULx

The connectors used on the MBa6ULx are listed in Table 6.
If a different board-to-board distance is required, higher connectors can be used.
Suitable connectors are to be taken from Table 6.

Table 6: Carrier board mating connectors

Manufacturer	Pin count / part number	Remark	Stack height (X)	
TE connectivity	100-pin: 5177986-4	On MBa6ULx	5 mm	
	100-pin: 1-5177986-4	–	6 mm	
	100-pin: 2-5177986-4	–	7 mm	
	100-pin: 3-5177986-4	–	8 mm	

Note:	TQMa6ULx interfaces
	Depending on the selected TQMa6ULx, not all interfaces are available. Available interfaces are to be taken from the pinout table in the TQMa6ULx User's Manual.

4.1.2 I²C address mapping

An audio codec, three port replicators, the I²C touch screen controller and a temperature sensor with EEPROM can be addressed via I2C4. Table 7 shows the addresses used on the MBa6ULx and TQMa6ULx.

The I2C4 interface is also connected to pin header X1, pins 12 and 13. Optionally, the I2C2 interface can be routed to these pins. The following table shows the address assignment of MBa6ULx and TQMa6ULx.

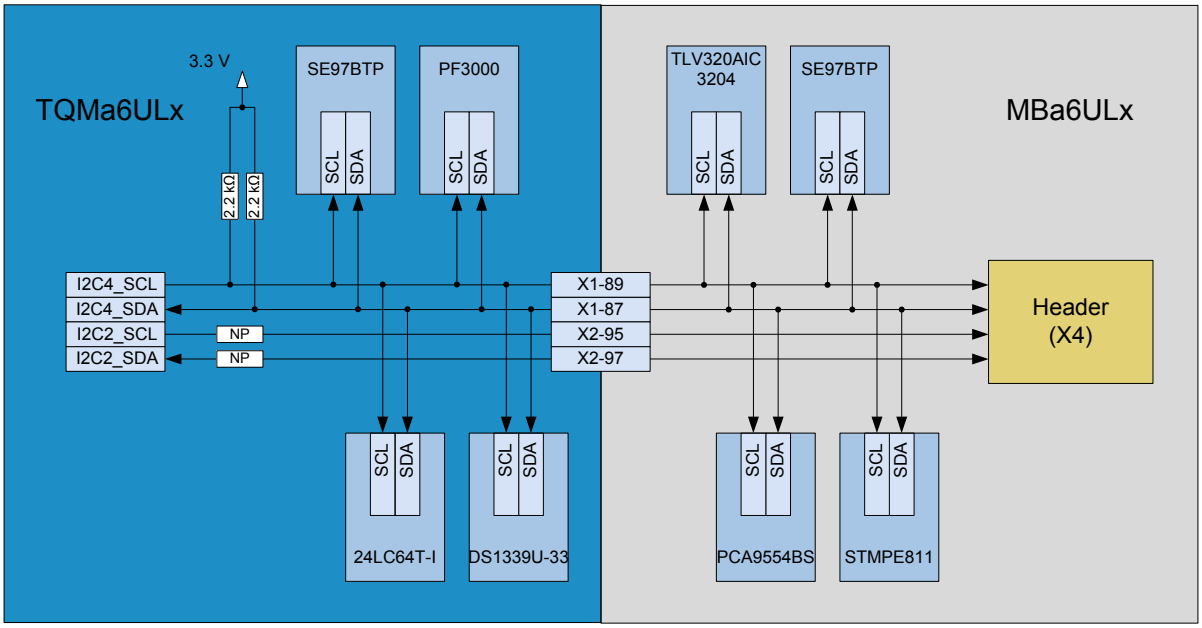


Illustration 3: Block diagram I²C busses

Table 7: I2C4 address assignment

Component	Ref ID	Address		Location
PMIC (PF3000/3001)	–	0x08	000 1000b	TQMa6ULx
Audio Codec (TLV320AIC3204)	N2200	0x18	001 1000b	MBa6ULx
Temperature sensor (SE97BTP)	D2400	0x19	001 1001b	MBa6ULx
Temperature sensor (SE97BTP)	–	0x1A	001 1010b	TQMa6ULx
Port replicator outputs (PCA9554BS), D900	D900	0x20	010 0000b	MBa6ULx
Port replicator inputs (PCA9554BS), D901	D901	0x21	010 0001b	MBa6ULx
Port replicator outputs (PCA9554BS), D902	D902	0x22	010 0010b	MBa6ULx
I²C Touch Screen Controller (STMPE811)	D2001	0x41	100 0001b	MBa6ULx
EEPROM (24LC64T-I_MC)	–	0x50	101 0000b	TQMa6ULx
EEPROM (SE97BTP)	D2400	0x51	101 0001b	MBa6ULx
EEPROM (SE97BTP)	–	0x52	101 0010b	TQMa6ULx
RTC (DS1339U-33)	–	0x68	110 1000b	TQMa6ULx

Attention:	I2C4 bus
	Attention when using I2C4. Since the PMIC can be addressed on I2C4, errors on the bus can lead to instabilities of the TQMa6ULx!

4.1.3 Temperature sensor / SPD EEPROM

On the TQMa6ULx as well as on the MBa6ULx a temperature sensor SE97BTP is assembled. Both temperature sensors are connected to the I2C4 bus. The SE97BTP on the MBa6ULx is placed on the top side, underneath the TQMa6ULx.

The temperature sensor has address `0x19`; the SPD EEPROM has address `0x51`.

The addresses can be changed by reassembling some resistors. For details see MBa6ULx schematics.

If the address is changed, attention has to be paid that no address conflict occurs with other I²C devices.

Table 8: Electrical characteristics SE97BTP

Parameter	Value	Range
Accuracy	±1 °C (max.)	+75 °C to +95 °C
	±2 °C (max.)	+40 °C to +125 °C
	±3 °C (max.)	–40 °C to +125 °C
Resolution	0.125 °C	11 Bit

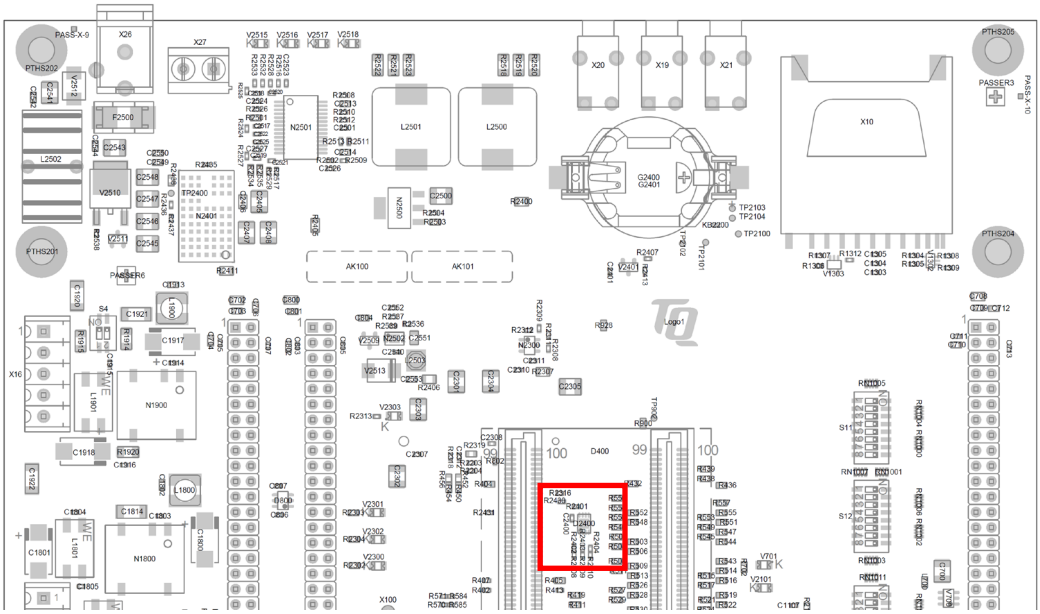


Illustration 4: Position of SE97BTP on MBa6ULx, D2400

4.1.4 RTC supply

The TQMa6ULx provides a discrete RTC. Another RTC is provided by the i.MX6ULx on the TQMa6ULx.
Both RTCs are supplied via the LICELL pin X1-10.
A lithium battery type CR2032 with very low self-discharge is provided on the MBa6ULx as a backup supply for both RTCs.

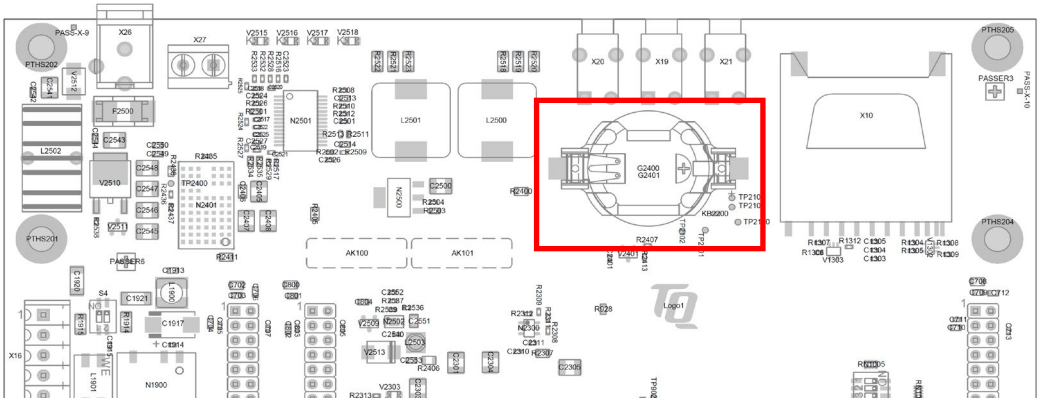


Illustration 5: Block diagram RTC supply

The increased current consumption must be considered, if the i.MX6ULx RTC is used.
This leads to a fast battery discharge. More information can be found in the TQMa6ULx User's Manual.
For the RTCs installed on the MBa6ULx the following applies:

Table 9: RTC supply, components

Parameter	Value	Remark
Coin cell	2.1 V to 3.7 V, typical 3.0 V, 220 mAh	–20 °C to +60 °C
Current consumption RTC	See TQMa6ULx User's Manual	Depends on RTC used

4.1.5 Port replicator

Some of the 24 ports of the PCA9554BS port replicators are used to control various components on the MBa6ULx.
These include the buzzer, user LEDs, interrupts, resets, mini PCIe and navigation buttons.
All port replicators are configured via I2C4. The respective address can be changed by reassembling resistors.
When changing the address, it must be ensured that no address conflicts occur with existing I²C devices.
The assembly options are documented in the MBa6ULx circuit diagram.
In the initial state after power-on, all ports are set as input.
As a result, the components controlled by an output pin cannot be used before initialization and are therefore deactivated.

The following table shows the functions of all port expanders.

Table 10: Functions of port expander ports

Reference	Port	Signal	Direction	Default	Remark
D900	IO0_0	PCIE.RST#	O	Low	PCIe Reset, 0 Ω in series NP
	IO0_1	LCD.PWR_EN	O	High	Enable signal for LVDS, 0 Ω in series
	IO0_2	PCIE.PWR_EN	O	Low	Enable signal for PCIe, 0 Ω in series
	IO0_3	LVDS_SHTDN#	O	High	LVDS Shutdown, 0 Ω in series
	IO0_4	LCD.BLT_EN	O	High	LCD Backlight Enable, 0 Ω in series
	IO0_5	PCIE.WAKE#	O	High	PCIe Wakeup, 0 Ω in series
	IO0_6	PCIE.DIS#	O	High	PCIe Disable, 0 Ω in series
	IO0_7	NC	–	–	–
D901	IO1_0	BUTTON.1#	I	High	Input for button 1
	IO1_1	BUTTON.2#	I	High	Input for button 2
	IO1_2	BUTTON.3#	I	High	Input for button 3
	IO1_3	LCD.INT#	I	High	LCD Interrupt, 0 Ω in series
	IO1_4	NC	I	–	Test point
	IO1_5	TEMP_OS#	I	High	Thermal Alarm Output SE97BTP
	IO1_6	ENET 1.INT#	I	High	Ethernet 1 Interrupt, 0 Ω in series
	IO1_7	ENET 2.INT#	I	High	Ethernet 2 Interrupt, 0 Ω in series
D902	IO2_0	USB.RST#	O	High	USB HUB Reset, 0 Ω in series
	IO2_1	ENET1.RST#	O	High	Ethernet 1 Phy-Reset, 0 Ω in series
	IO2_2	ENET2.RST#	O	High	Ethernet 2 Phy-Reset, 0 Ω in series
	IO2_3	AUDIO.RST#	O	High	Audio Reset, 0 Ω in series
	IO2_4	LED1	O	Low	LED green On / Off, 0 Ω in series
	IO2_5	LED2	O	Low	LED green On / Off, 0 Ω in series
	IO2_6	BUZZER	O	Low	Sound On / Off, 0 Ω in series
	IO2_7	NC	O	–	Test point

Table 11: Port expander, component

Manufacturer / part number	Description
NXP / PCA9554BS	• 8-fold port expander • I²C interface • Configurable as input or output

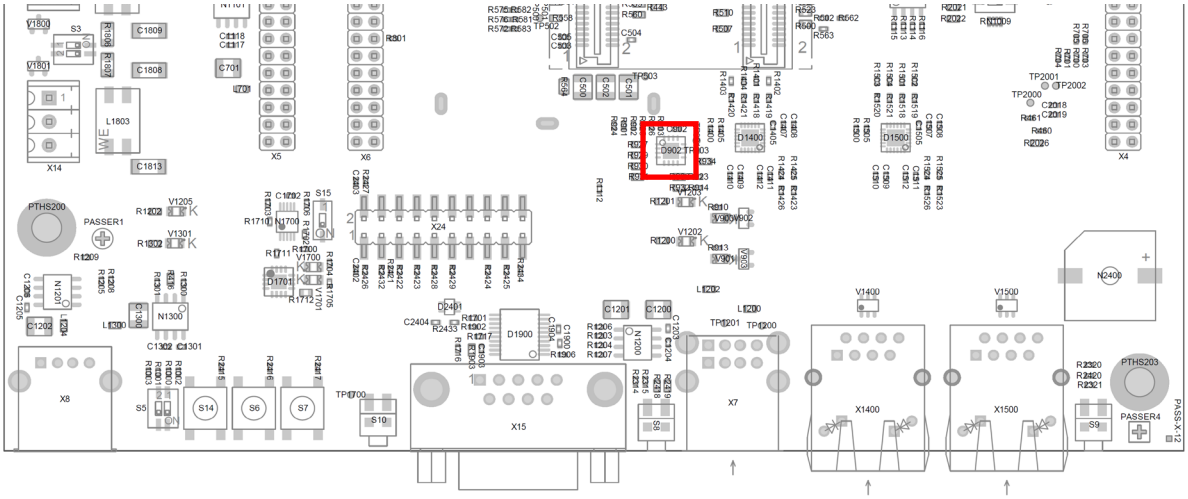


Illustration 6: Port expander placement, top

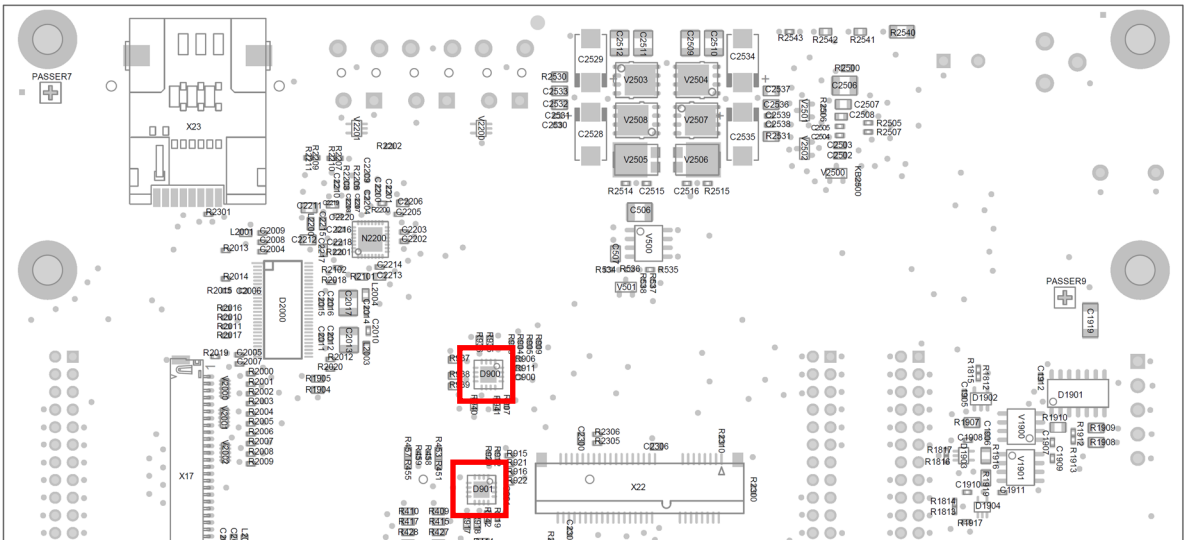


Illustration 7: Port expander placement, bottom

4.1.6 Power and Reset

The MBa6ULx provides several options to trigger a complete or partial reset of the assembly.
The following table shows the signals used.

Table 12: TQMa6ULx Reset signals

Reset-Signal	Source	Type	Default	Remark
PCIE.PWR_EN	Port-Expander D900 IO02	O	Low	Enable for Mini-PCIe-supply
LCD_RESET#	TQMa6ULx i.MX6UL	O	High	See TQMa6ULx User's Manual (8). Configure as a reset signal by a driver.
PCIE_RST#	Port-Expander D902 IO03	O	High	Reset for mPCIe
AUDIO.RST#	Port-Expander D900 IO00	O	High	Reset for Audio-Codec
USB.RST#	Port-Expander D902 IO00	O	High	Reset for USB-Hub-Controller
LVDS_SHDN#	Port-Expander D900 IO03	O	High	Reset for LVDS-Transceiver
PMIC_PWRON	TQMa6ULx PMIC	I	High	See TQMa6ULx User's Manual (8). Can be used by User-Button S8.
RESET_IN#	TQMa6ULx i.MX6UL	I	High	See TQMa6ULx User's Manual (8). Can be used by User-Button S10.
IMX_ONOFF#	TQMa6ULx i.MX6UL	I	High	See TQMa6ULx User's Manual (8). Can be used by User-Button S8.
RESET_OUT#	TQMa6ULx i.MX6UL	O	High	See TQMa6ULx User's Manual (8) Activates when i.MX6UL reset is active. Reset for peripherals on carrier board. Becomes STKRST#.
ENET_RST#	TQMa6ULx i.MX6UL	O	High	See TQMa6ULx User's Manual (8) Configure as a reset signal by a driver.
ENET1_RST#	TQMa6ULx i.MX6UL	O	High	Reset for Ethernet-PHY 1 Configure as a reset signal by a driver.
ENET2_RST#	TQMa6ULx i.MX6UL	O	High	Reset for Ethernet-PHY 2 Configure as a reset signal by a driver.
WDOG1#	TQMa6ULx i.MX6UL	O	High	Used for software/warm reset. Controls the reset input of the TQMa6ULx. Configure as WDOG signal by driver.

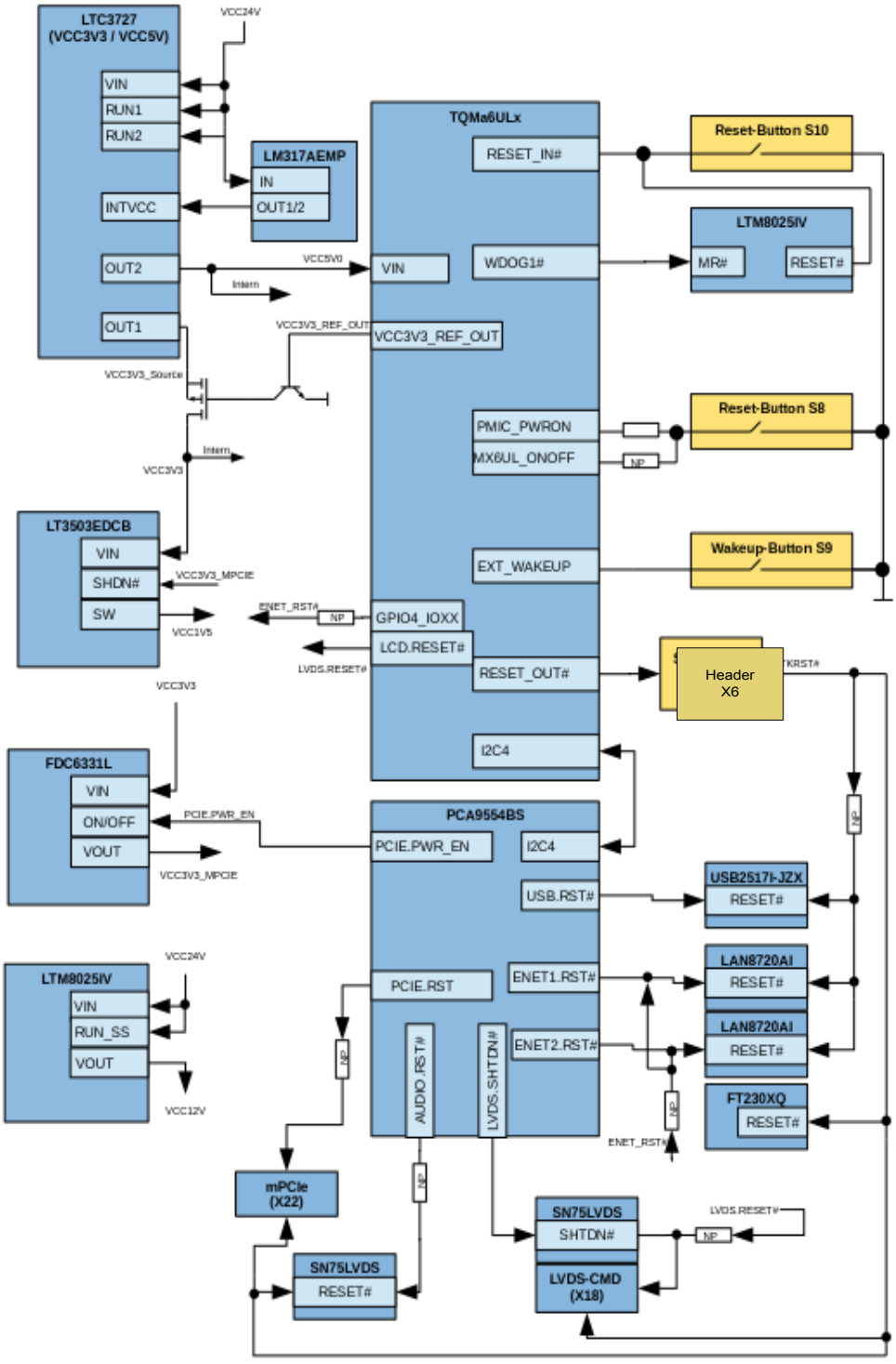


Illustration 8: Block diagram Power and Reset

4.1.7 Power supply

The MBa6ULx is supplied with 24 V via X26 or X27. From this voltage 1.5 V, 3.3 V, 5 V and 12 V are generated on the MBa6ULx. These voltages are used to supply the components on the MBa6ULx.

Additionally, 3.3 V, 5 V and 12 V are available at each of the three headers, X4, X5, and X6.

5 V and 12 V are available at the LVDS-CMD connector, X18. All five connectors share the available power.

The PCIe connector is supplied with 1.5 V and 3.3 V. 1.5 V are generated from 5 V and are only available at the PCIe connector.

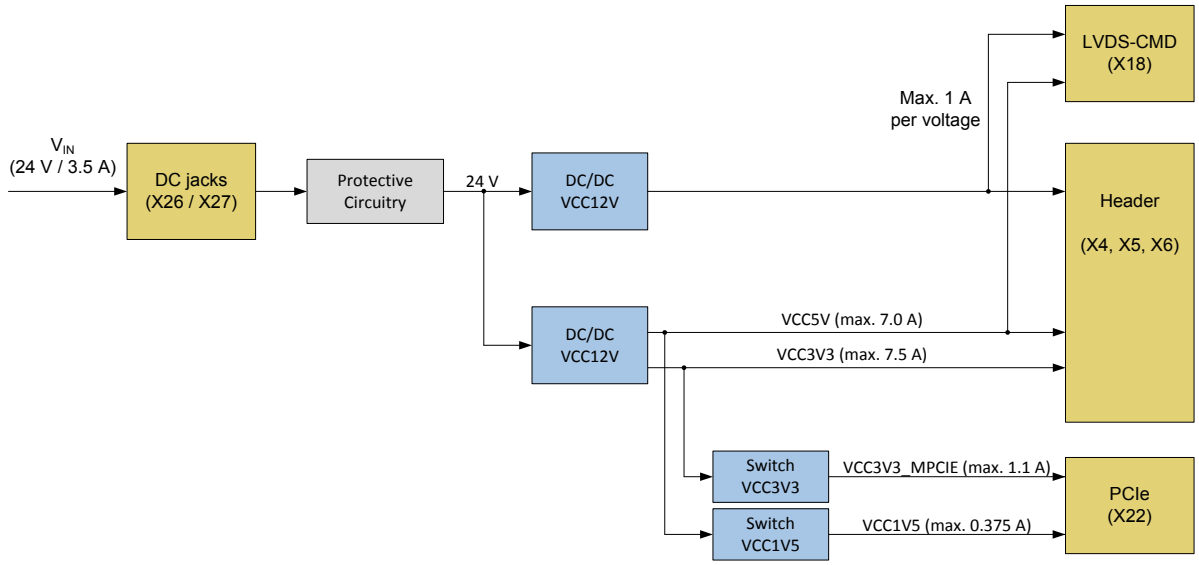


Illustration 9: Block diagram power supply

Attention:	Malfunction
	In an own design, the switching regulator for VCC3V3 should be switched on or off using TQMa6ULx signal VCC3V3_REF_OUT, to avoid cross supply and errors in the power-up/down sequence of the TQMa6ULx [11]. Please refer to the MBa6ULx circuit diagram for a corresponding circuit suggestion.

11: Attention: When the PMIC is switched off, voltage VCC3V3_REF_OUT (from the TQMa6ULx) drops to approx. 2.7 V due to cross-supply effects of the still activated 3.3 V (on the MBa6ULx). It must be ensured that the circuitry can respond to this level.

4.1.7.1 Protective circuitry

The 3.3 V / 5 V and the 12 V switching regulators are supplied with V_{IN}. The protective circuit has the following characteristics:

- Slow blow fuse 5 A
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

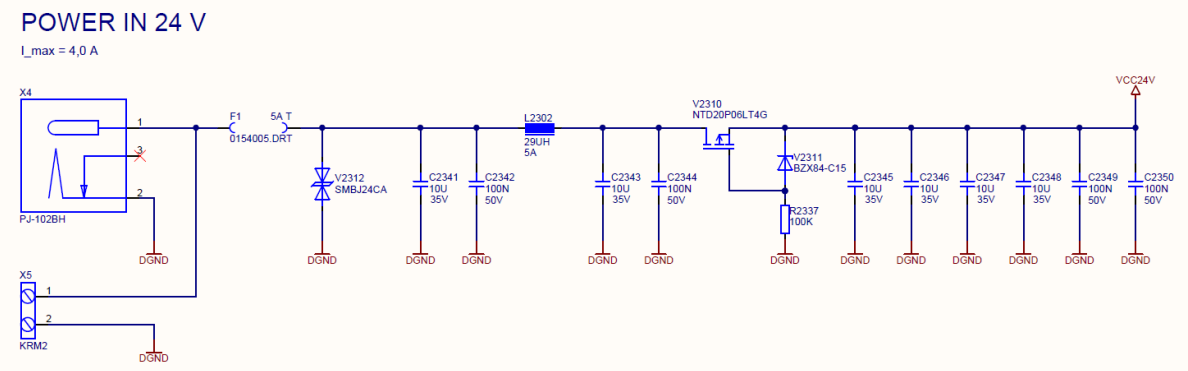


Illustration 10: Protective circuit for V_{IN}

Table 13: Characteristics of protective circuit

Parameter	Min.	Typ.	Max.	Unit
Overcurrent limitation by fuse (slow blow)	–	5	–	A
Excess voltage limitation by SMBJ24CA	26.7	–	29.5	V

4.1.7.2 Power consumption

Theoretically the combination of TQMa6ULx plus MBa6ULx takes up 65 W under full load (all supply voltages at the pin strips are loaded with maximum current). The power supply used must be dimensioned accordingly. In most applications, however, the power consumption will be significantly lower. The combination of TQMa6ULx plus MBa6ULx typically consumes 4.5 W at full CPU load.

4.1.7.3 Electrical characteristics switching regulator

The characteristics in the following tables apply to switching regulators LTM8025, LTC3727, and LT3503 shown in Illustration 9.

Table 14: Characteristics LTM8025

Parameter	Min.	Typ.	Max.	Unit	Remark
VCC12V					
Output voltage	–	12	–	V	–
Output current	–	–	3	A	–

Table 15: Characteristics LTC3727

Parameter	Min.	Typ.	Max.	Unit	Remark
VCC5V					
Output voltage	4.99	–	5.02	V	–
Output current	–	–	7	A	–
VCC3V3					
Output voltage	3.29	3.3	3.31	V	–
Output current	–	–	7.5	A	Minus VCC3V3_MPCIE
VCC3V3_MPCIE					
Output voltage	3.25	3.3	3.35	V	–
Output current	–	–	1.1	A	–

Table 16: Characteristics LT3503

Parameter	Min.	Typ.	Max.	Unit	Remark
VCC1V5					
Output voltage	1.49	1.5	1.51	V	–
Output current	–	–	0.375	A	–

4.1.7.4 Power supply connectors

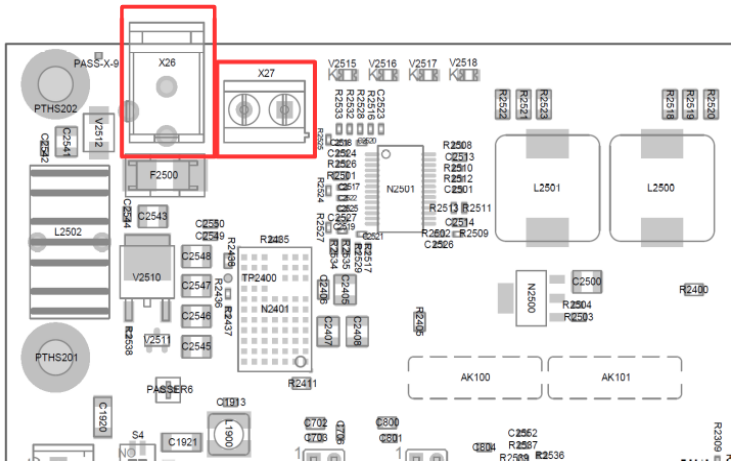


Illustration 11: Position of connectors X26, X27

Table 17: Types of power supply connectors

Manufacturer / part number	Description
Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V
Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A

4.2 Communication interfaces

4.2.1 USB 2.0 Hi-Speed Host

The TQMa6ULx provides a chip-to-chip connection for USB via HSIC, which only differs from USB in the physical layer.
A USB hub USB2517I provides seven USB 2.0 Hi-Speed Host interfaces. The hub offers one upstream port and seven downstream ports. The supply of the USB connectors with 5 V is realized by power distribution switches. The components used have current monitoring and can switch off the bus voltage in case of overload and/or overheating. Detailed information can be found in the data sheets of the switches MIC2026.
USB host 1 and 2 are connected to the dual port USB Type-A connector X7, USB host 3 to a single port USB Type-A connector.
USB host 6 can be tapped on pin header X5 and USB host 5 can be tapped on the LVDS-CMD connector X18.
USB host 4 is routed to header X4; USB host 7 is routed to mini PCIe connector X22.

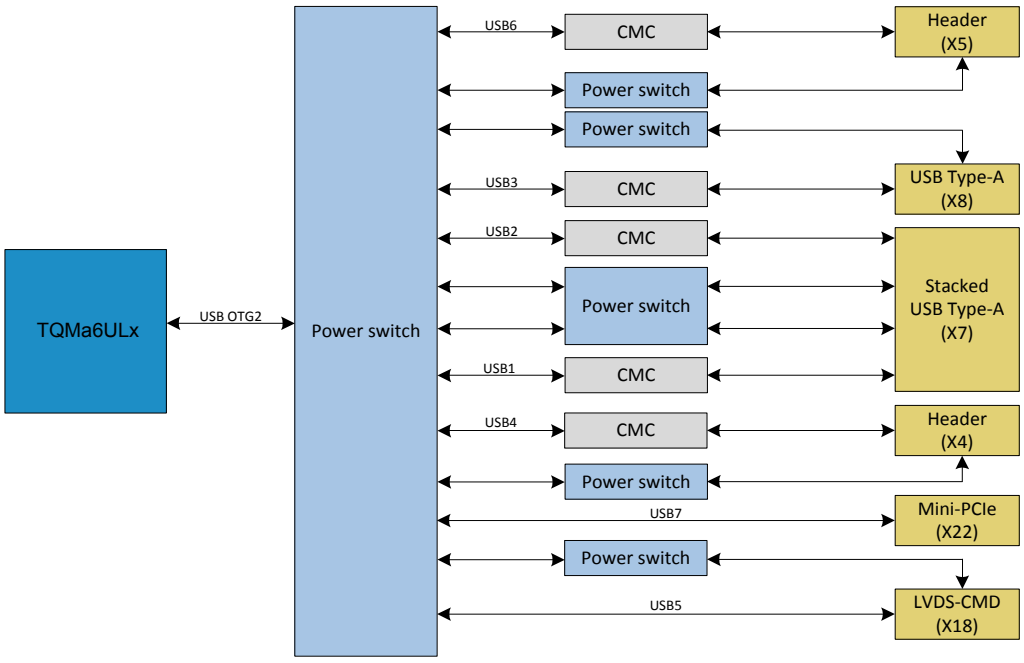


Illustration 12: Block diagram USB-Hosts

The following tables show the pinout of the connectors used.

Table 18 Pinout USB Host 1 & 2, dual port USB receptacle – X7

Pin	Pin name	Signal	Direction	Remark
1A	VBUS	USB_H1_VBUS	P	100 µF to DGND + EMI Filter
2A	D–	USB_H1_D_N	I/O	Common Mode Choke in series
3A	D+	USB_H1_D_P	I/O	Common Mode Choke in series
4A	DGND	DGND	P	–
1B	VBUS	USB_H2_VBUS	P	100 µF to DGND + EMI Filter
2B	D–	USB_H2_D_N	I/O	Common Mode Choke in series
3B	D+	USB_H2_D_P	I/O	Common Mode Choke in series
4B	DGND	DGND	P	–
M1 – M4	DGND	DGND	P	–

Table 19 Pinout USB Host 3, single port USB receptacle – X8

Pin	Pin name	Signal	Direction	Remark
1	VBUS	USB_H3_VBUS	P	100 µF to DGND + EMI Filter
2	D–	USB_H3_D_N	I/O	Common Mode Choke in series
3	D+	USB_H3_D_P	I/O	Common Mode Choke in series
4	DGND	DGND	P	–
M1, M2	DGND	DGND	P	–

Table 20 Pinout USB Host 4, display header – X4

Pin	Pin name	Signal	Direction	Remark
34	VBUS	USB_H4_VBUS	P	100 µF to DGND + EMI Filter
36	D–	USB_H4_D_N	I/O	Common Mode Choke in series
38	D+	USB_H4_D_P	I/O	Common Mode Choke in series

Table 21 Pinout USB Host 5, LVDS-CMD connector – X18

Pin	Pin name	Signal	Direction	Remark
11	VBUS	USB_H5_VBUS	P	100 µF to DGND + EMI Filter
13	D–	USB_H5_D_N	I/O	Common Mode Choke in series
14	D+	USB_H5_D_P	I/O	Common Mode Choke in series

Table 22 Pinout USB Host 6, header – X5

Pin	Pin name	Signal	Direction	Remark
53	VBUS	USB_H6_VBUS	P	100 µF to DGND + EMI Filter
55	D–	USB_H6_D_N	I/O	Common Mode Choke in series
57	D+	USB_H6_D_P	I/O	Common Mode Choke in series

Table 23 Pinout USB Host 7, mPCIe connector – X22

Pin	Pin name	Signal	Direction	Remark
36	D–	USB_H7_D_N	I/O	Common Mode Choke in series
38	D+	USB_H7_D_P	I/O	Common Mode Choke in series

The USB host port of the TQMa6ULx provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

Table 24: Characteristics USB

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5	5.25	V	–
Current	–	500	900	mA	–
Read	–	15.7	–	Mbyte/s	USB stick at port 1: 100 Mbyte file, 10 Mbyte block size
Write	–	7.4	–	Mbyte/s	USB stick at port 1: 100 Mbyte file, 10 Mbyte block size

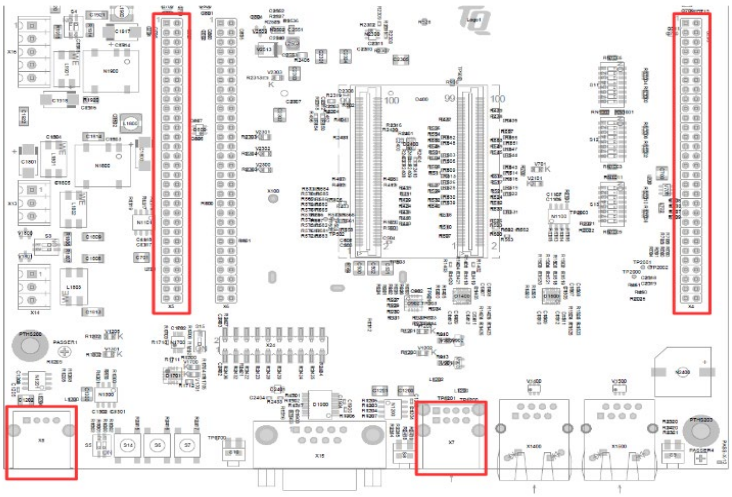


Illustration 13: Position of USB Host – X4, X5, X7, X8

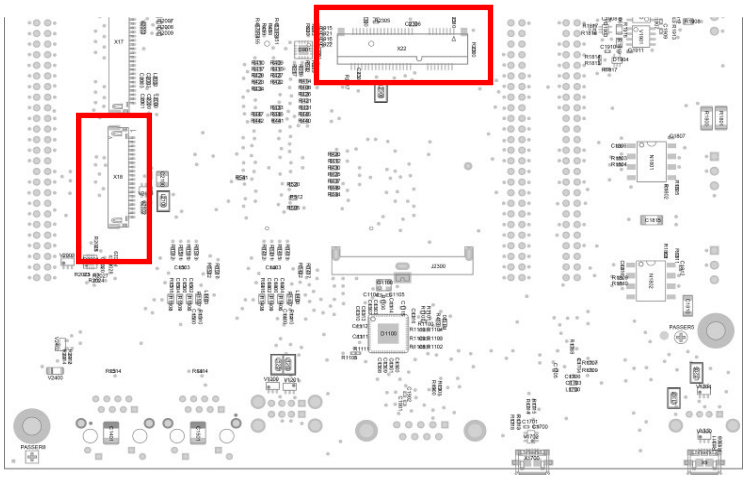


Illustration 14: Position of USB Host – X18, X22

Table 25: USB, components

Manufacturer / part number	Description
Yamaichi / USB-A-002A	Dual port USB receptacle, Type-A, U_N=30 V AC_{RMS} / I_N=1 A
Molex / 67643-2910	Single port USB receptacle Type-A, U_N=30 V / I_N=1.5 A
Hirose / DF19G-20P-1H	Board-to-Cable connector 20-pin, 1 mm pitch
Fischer Elektronik / SL 22 124 60 G	Header, 100 mil pitch, 2 × 30 pins

4.2.2 USB 2.0 Hi-Speed OTG

Both USB-OTG interfaces of the TQMa6ULx are provided on the MBa6ULx. OTG1 is provided with a 5-pin Micro-AB receptacle. OTG2 is connected to the USB hub controller. Both OTG interfaces are operated in the standard BSP in host mode only. An OTG or device function is not implemented in software except for the serial downloader.

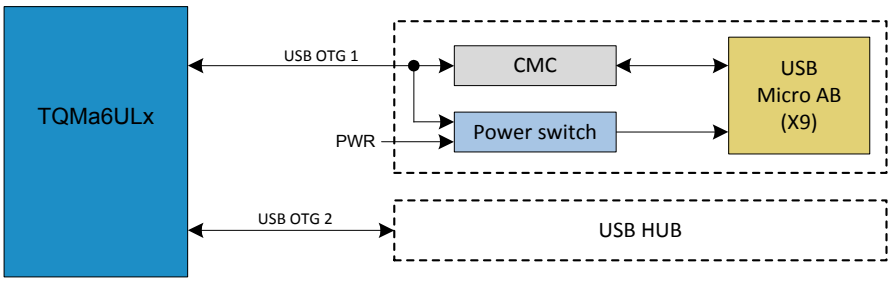


Illustration 15: Block diagram USB 2.0 Hi-Speed OTG

The following table shows the pinout of the connector used.

Table 26: Pinout USB-Host OTG – X9

Pin	Pin name	Signal	Direction	Remark
1	VBUS	USB_OTG_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
2	D–	USB_OTG_D_N	I/O	Common mode choke in series
3	D+	USB_OTG_D_P	I/O	Common mode choke in series
4	ID	USB_OTG.ID	I	–
5	DGND	DGND	P	–
M1 – M6	DGND	DGND	P	–

The interface can serve as Client or Host. To use this feature, appropriate software support is necessary, however.
The OTG ports of the TQMa6ULx provide a theoretical data rate of 480 Mbit/s. The data rate can significantly deviate depending on the hardware and software used.

Table 27: Characteristics USB 2.0 Hi-Speed OTG

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5	5.25	V	–
Current	–	500	900	mA	–
Read	–	20.4	–	Mbyte/s	USB 2.0 stick: 100 Mbyte file, 10 Mbyte block size
Write	–	8.0	–	Mbyte/s	USB 2.0 stick: 100 Mbyte file, 10 Mbyte block size

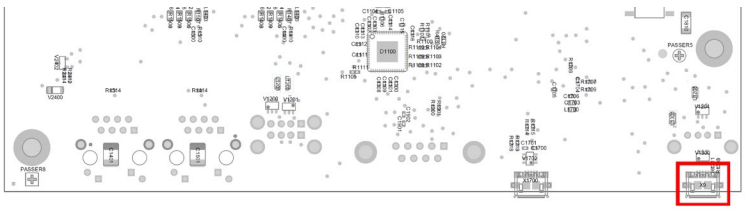


Illustration 16: Position of USB 2.0 Hi-Speed OTG – X9

Table 28: Type of USB Micro-AB receptacle

Manufacturer / part number	Description
TE connectivity / 1981584-1	USB receptacle, Micro-AB

4.2.3 Ethernet 100BASE-T

Both Ethernet MACs of the TQMa6ULx are provided on the MBa6ULx via a connection to an SMSC PHY LAN8720Ai each.
Both RMII interfaces contain their own PHY reset and interrupt signals as well as a common PHY reset.
The PHY LAN8720Ai has bootstraps to start with configurable default values.
All bootstraps can be customised through assembly options.
Further information is available in the MBa6ULx circuit diagram.

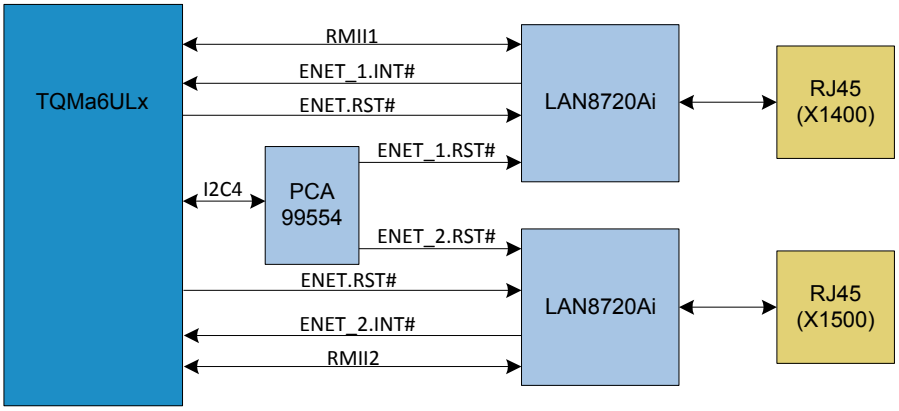


Illustration 17: Block diagram Ethernet 100 BASE-T

Both RJ45 jacks contain integrated magnetics and two status LEDs.
The following tables show the pinout of the RJ45 receptacles.

Table 29: Pinout Ethernet 1 – X1400

Pin	Pin name	Signal	Direction
1	TX+	ETH1_MDI_TX_P	I/O
2	TX–	ETH1_MDI_TX_N	I/O
3	RX+	ETH1_MDI_RX_P	I/O
4	–	AVDD_ETH_1	P
5	–	AVDD_ETH_1	P
6	RX–	ETH1_MDI_RX_N	I/O
7	–	NC	–
8	–	GND	P

Table 30: Pinout Ethernet 2 – X1500

Pin	Pin name	Signal	Direction
1	TX+	ETH2_MDI_TX_P	I/O
2	TX–	ETH2_MDI_TX_N	I/O
3	RX+	ETH2_MDI_RX_P	I/O
4	–	AVDD_ETH_2	P
5	–	AVDD_ETH_2	P
6	RX–	ETH2_MDI_RX_N	I/O
7	–	NC	–
8	–	GND	P

The possible data throughput is influenced by the system load and the software platform used.
The following transfer rates can be achieved with the MBa6ULx and the standard TQ-BSP.

Table 31: Data throughput Ethernet 1&2

Direction	Typical
Upstream	94 Mbit/s
Downstream	93.5 Mbit/s

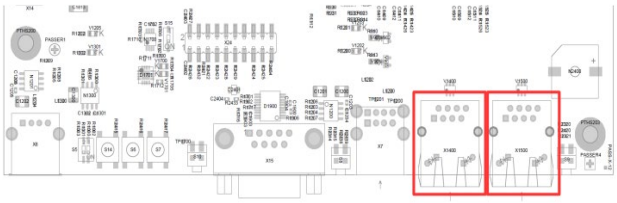


Illustration 18: Position of Ethernet 100BASE-T – X1400, X1500

Table 32: Ethernet 100BASE-T connector

Manufacturer / part number	Description
Pulse Electronics / J0006D21BNL	RJ45 receptacle, 10/100BASE-T, integrated magnetics

4.2.4 CAN

Both CAN interfaces on the MBa6ULx are directly connected to the CAN ports of the TQMa6ULx and are routed to the 3-pin connectors X13 and X14. Both interfaces are galvanically separated. The CAN interfaces are galvanically not separated among themselves. The CAN signals can be terminated with 120 Ω using DIP switches S3-1 and S3-2.

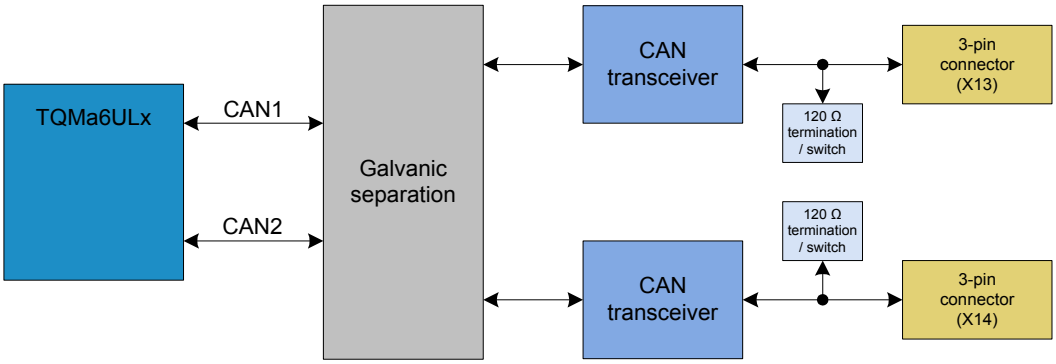


Illustration 19: Block diagram CAN

Table 33: CAN termination – S3

Switch	Interface	ON	OFF
S3-1	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated
S3-2	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated

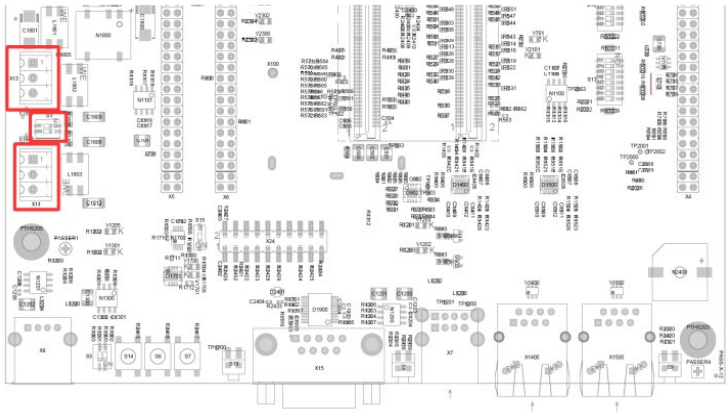


Illustration 20: Position of CAN – X13, X14, S13

Table 34: Pinout CAN1, CAN2 – X13, X14

Connector	Pin	Pin name	Signal	Direction	Remark
X13	1	CAN_H	CAN2_P	I/O	Galvanically separated
	2	CAN_L	CAN2_N	I/O	Galvanically separated
	3	DGND	DGND_CAN	P	Galvanically separated
X14	1	CAN_H	CAN1_P	I/O	Galvanically separated
	2	CAN_L	CAN1_N	I/O	Galvanically separated
	3	DGND	DGND_CAN	P	Galvanically separated

Table 35: Type of CAN connector

Manufacturer / part number	Description
Phoenix Contact / MCV1,5/3-G-3,5	3-pin housing, 160 V / 8 A, 3.5 mm pitch

4.2.5 RS-485

The UART6 interface of the TQMa6ULx is routed to an RS-485 transceiver (SP491), which provides the signals at the 9-pin D-Sub connector X16. The RS-485 interface is galvanically separated.

In full-duplex mode (default) the interface can operate with a maximum data rate of 1 Mbit/s.

Half-duplex is possible with an assembly option. In this case the receiver is controlled by UART6.RTS#.

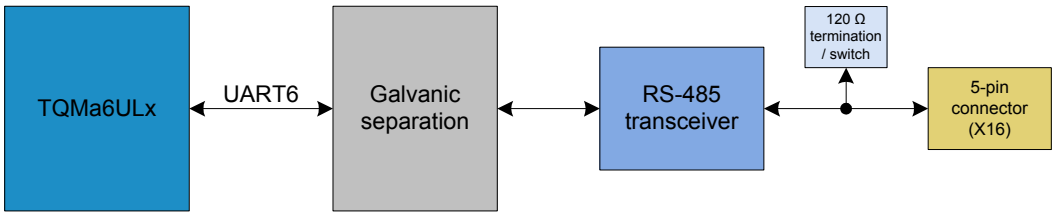


Illustration 21: Block diagram RS-485

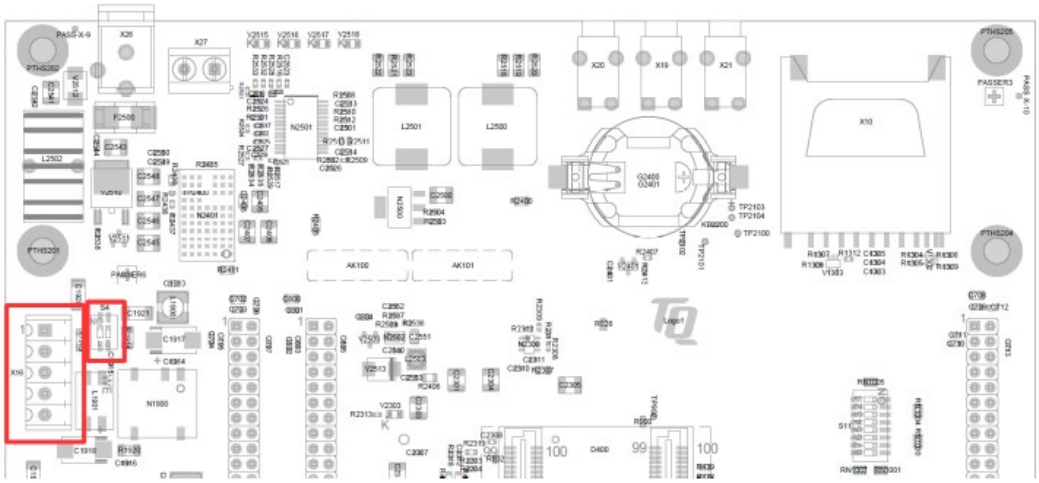


Illustration 22: Position of RS-485 – X16, S4

Table 36: RS-485 mode settings

Mode	R1913	R1912	Remark
Full-duplex	n.a.	0 Ω	Receiver always active (default)
Half-duplex	0 Ω	n.a.	Receiver controlled by RTS# (UART6.RTS#)

The RS-485 signals can be terminated with 120 Ω using DIP switches S4-1 and S4-2.

Table 37: RS-485 termination – S4

Switch	Interface	ON	OFF
S4-1	RS-485	Receive path terminated with 120 Ω	Receive path not terminated
S4-2	RS-485	Transmit path terminated with 120 Ω	Transmit path not terminated

Table 38: Pinout RS-485 – X16

Pin	Pin name	Signal	Direction	Remark
1	A	RS-485_A	I	Galvanically separated
2	B	RS-485_B	I	Galvanically separated
3	Y	RS-485_Y	O	Galvanically separated
4	Z	RS-485_Z	O	Galvanically separated
5	DGND	DGND_RS485	P	Galvanically separated

The following characteristics apply to the interface:

Table 39: Characteristics RS-485

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	921.6	kbit/s	–
Electric strength	–	–	1	kV	–
Output swing RS-485_Y/Z	–	10.6	–	V	High-Level (open load)
Output voltage RS-485_Y/Z	–	4.44	–	V	Low-Level (27 Ω load)
Insulation clearance	1.4	–	–	mm	Inner layer
Insulation clearance	2.6	–	–	mm	Outer layer

Table 40: Type of RS-485 connector

Manufacturer / part number	Description
Phoenix Contact / MCV1,5/5-G-3,5	5-pin housing, 160 V / 8 A, 3.5 mm pitch

4.2.6 Debug interfaces RS-232 / USB

On the MBa6ULx the debug interfaces are available as RS-232 and USB device interface.
In both cases, the UART1 interface of the TQMa6ULx is used. No software configuration is required.
DIP switch S15 selects the interface, see Table 44.

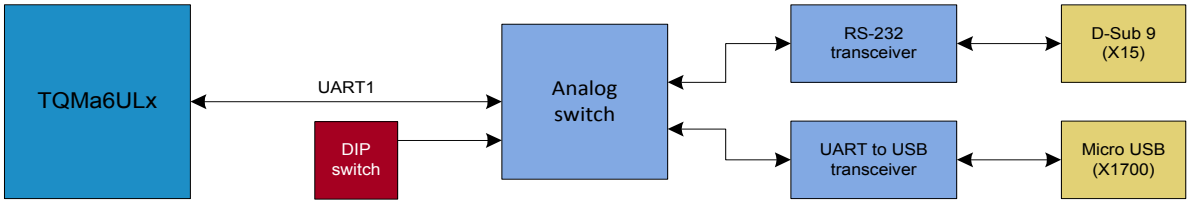


Illustration 23: Block diagram debug interfaces RS-232 / USB

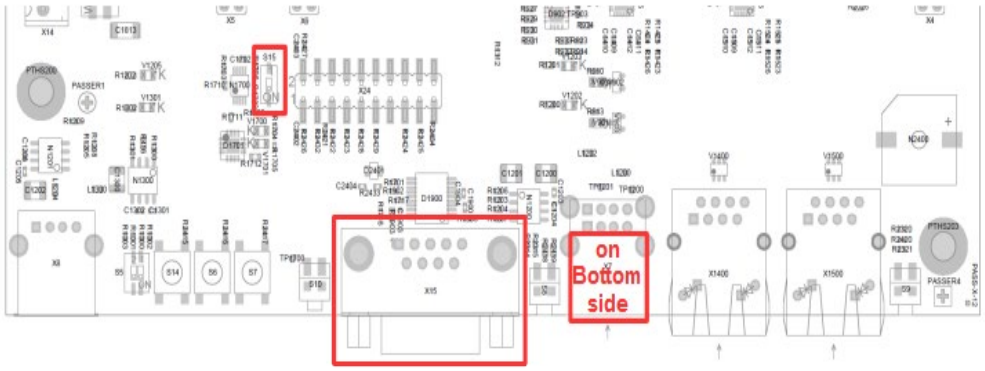


Illustration 24: Position of RS-232 – X15

Table 41: Debug interface connectors

Manufacturer / part number	Description
Yamaichi / DRA-09P11-ZN	9-pin D-Sub connector
TE connectivity / 1981584-1	USB receptacle, Micro-AB, right angle

The following table shows the pinout of the D-Sub 9 socket.

Table 42: Pinout RS-232 – X15

Pin	Pin name	Signal	Direction	Remark
1	–	NC	–	Not used
2	RXD	RS232_RXD	I	–
3	TXD	RS232_TXD	O	–
4	–	NC	–	Not used
5	DGND	DGND	P	–
6	–	NC	–	Not used
7	–	NC	–	Not used
8	–	NC	I	Not used
9	–	NC	–	Not used
M1, M2	DGND	DGND	P	–

The following table shows the pinout of the Debug Micro USB port.

Table 43: Pinout Debug USB – X1700

Pin	Pin name	Signal	Direction	Remark
1	VBUS_SENSE	VBUS_SENSE	–	–
2	USB_D_N	USB_RS232_D_N	I/O	–
3	USB_D_P	USB_RS232_D_P	I/O	–
4	–	NC	–	Not used
5	DGND	DGND	P	–
M1 – M6	DGND	DGND	P	–

Table 44: Debug interface selection – S15

DIP switch	On	Off
S15	Debug-Interface USB-Device at X1700	Debug-Interface RS-232 at X15

4.2.7 LVDS, LVDS-CMD

An LVDS display (4 × TX pairs) can be connected to the MBa6ULx. Since the i.MX6ULx does not provide a native LVDS interface, the LVDS signals are generated by a transceiver connected to the parallel LCD interface. An SN75LVDS83B is used for this purpose. The LVDS interface is connected to a DF19 connector. The LVDS data signals as well as 3.3 V and 5 V are routed to this connector (30-pin, X17). A second DF19 connector (20-pin, X18) provides additional power supplies 12 V and 5 V, as well as control signals and USB signals. The touch controller is connected to header X4 (see Table 60). The pin assignment of the connectors is shown in Table 45 and Table 46. The LVDS transceiver is configured for 8-bit FORMAT-1 mode and operates at 65 MHz. [12]

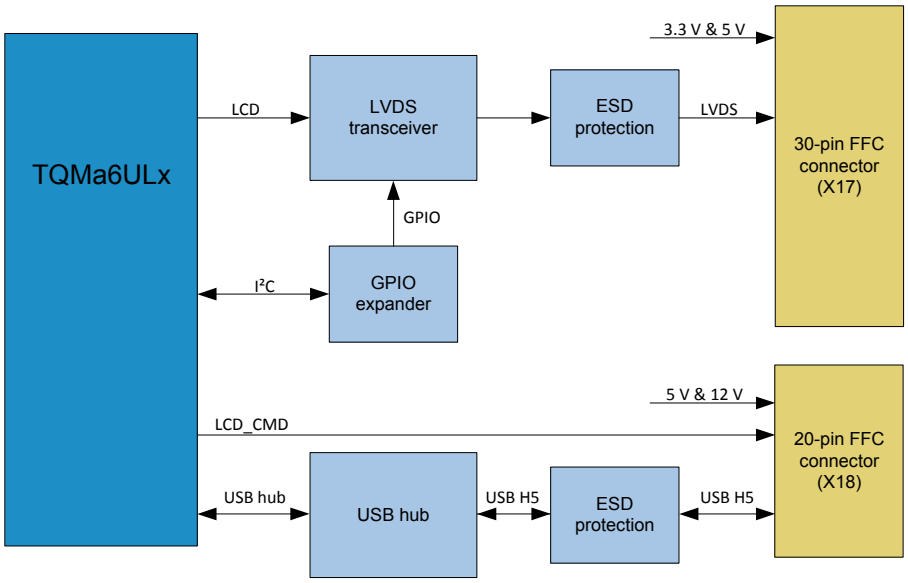


Illustration 25: Block diagram LVDS – X17, X18

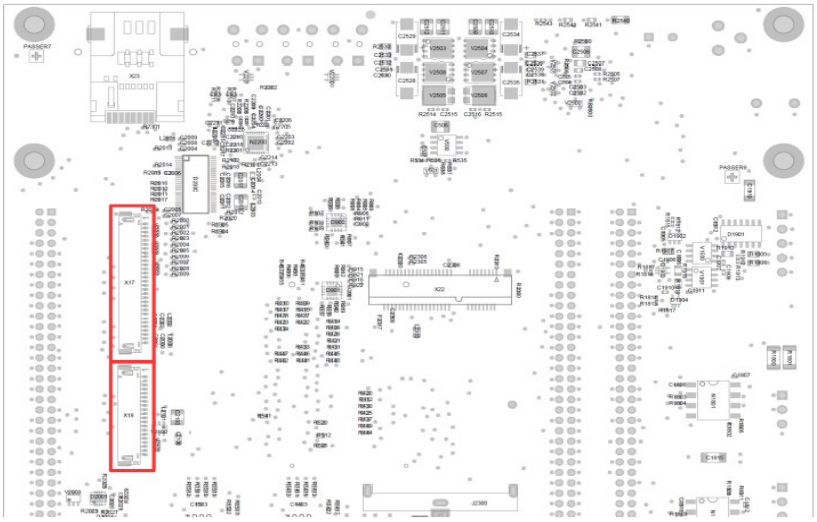


Illustration 26: Position of LVDS interface – X17, X18

12: See https://www.ti.com/lit/ds/symlink/sn75lvds83b.pdf.

Table 45: Pinout LVDS – X17

Pin	Pin name	Signal	Direction	Remark
1	LVDS0_TX0–	LVDS0_TX0_N	O	ESD protection
2	LVDS0_TX0+	LVDS0_TX0_P	O	ESD protection
3	LVDS0_TX1–	LVDS0_TX1_N	O	ESD protection
4	LVDS0_TX1+	LVDS0_TX1_P	O	ESD protection
5	LVDS0_TX2–	LVDS0_TX2_N	O	ESD protection
6	LVDS0_TX2+	LVDS0_TX2_P	O	ESD protection
7	DGND	DGND	P	–
8	LVDS0_CLK–	LVDS0_CLK_N	O	ESD protection
9	LVDS0_CLK+	LVDS0_CLK_P	O	ESD protection
10	LVDS0_TX3–	LVDS0_TX3_N	O	ESD protection
11	LVDS0_TX3+	LVDS0_TX3_P	O	ESD protection
12	NC	NC	–	–
13	NC	NC	–	–
14	DGND	DGND	P	–
15	NC	NC	–	–
16	NC	NC	–	–
17	DGND	DGND	P	–
18	NC	NC	–	–
19	NC	NC	–	–
20	NC	NC	–	–
21	NC	NC	–	–
22	NC	NC	–	–
23	NC	NC	–	–
24	DGND	DGND	P	–
25	VCC5V	VCC5V0_LVDS	P	I_{max} = 1 A [13] [14]
26	VCC5V	VCC5V0_LVDS	P	
27	VCC5V	VCC5V0_LVDS	P	
28	VCC3V3	VCC3V3_LVDS	P	I_{max} = 1 A [13] [14]
29	VCC3V3	VCC3V3_LVDS	P	
30	VCC3V3	VCC3V3_LVDS	P	
M1, M2	DGND	DGND	P	–

13: Due to maximum load of FFC contacts.
14: Excluding the current drawn from the headers.

To connect an LVDS display, the LVDS-CMD connector X18 is placed near the LVDS connector X17.
The FFC connector X18 provides a USB interface and control signals for display and backlight.
In addition to the data signals 5 V and 12 V are available as supply voltages.

Table 46: Pinout LVDS-CMD – X18

Pin	Pin name	Signal	Direction	Remark
1	VCC12V	VCC12V	P	I_{max} = 1 A [15] [16]
2	VCC12V	VCC12V	P	
3	VCC12V	VCC12V	P	
4	DGND	DGND	P	–
5	DGND	DGND	P	–
6	DGND	DGND	P	–
7	VCC5V	VCC5V	P	I_{max} = 1 A [15] [16]
8	VCC5V	VCC5V	P	
9	DGND	DGND	P	–
10	DGND	DGND	P	–
11	VBUS	USB_H5_VBUS	P	ESD protection
12	DGND	DGND	P	–
13	D–	USB_H5_D_N	I/O	ESD protection + common mode choke in series
14	D+	USB_H5_D_P	I/O	ESD protection + common mode choke in series
15	DGND	DGND	P	–
16	LCD_RESET#	LCD.RESET#	O	ESD protection
17	LCD_BLT_EN	LCD.BLT_EN	O	ESD protection
18	LCD_PWR_EN	LCD.PWR_EN	O	ESD protection
19	LCD_CONTRAST	LCD.CONTRAST	O	ESD protection
20	DGND	DGND	P	–
M1, M2	DGND	DGND	P	–

Table 47: Type of LVDS / LVDS-CMD connectors

Manufacturer / part number	Description
Hirose / DF19G-20P-1H	Board-to-Cable FFC connector 20-pin, 1 mm pitch
Hirose / DF19G-30P-1H	Board-to-Cable FFC connector 30-pin, 1 mm pitch

15: Due to maximum load of FFC contacts.
16: Excluding the current drawn from the headers.

4.2.8 Audio

An audio codec TI TLV320AIC3204 is provided on the MBa6ULx.
It is connected to the TQMa6ULx via SAI (configured as I^2S) and I^2C.
The audio codec provides microphone, line-in and line-out signals. The signals can be tapped from 3.5 mm jacks.
A placement option allows the user to choose between line-out and headphone. Table 48 shows the configuration.

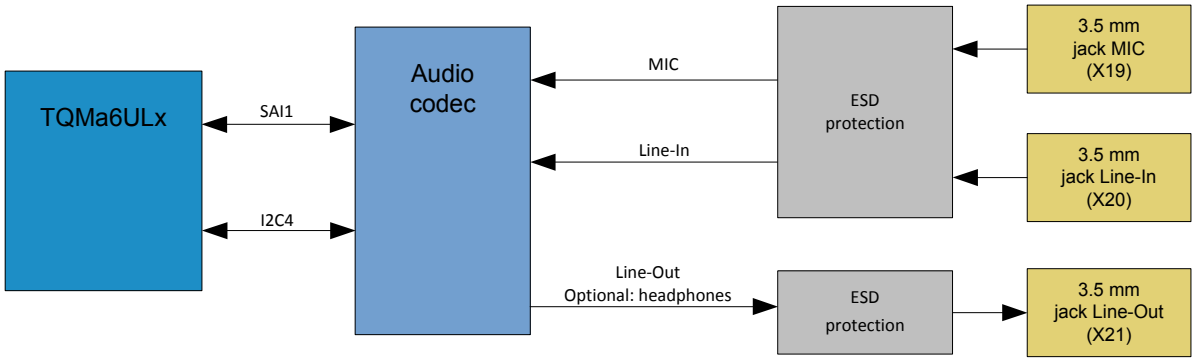


Illustration 27: Block diagram audio

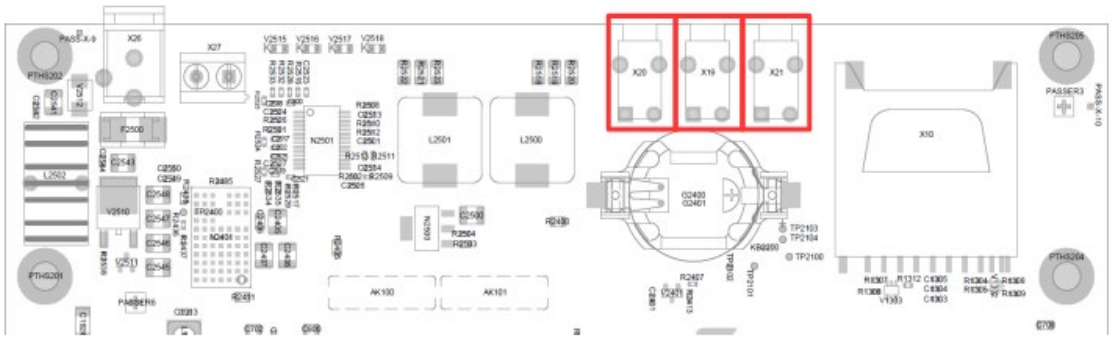


Illustration 28: Position of audio connectors – X20, X21, X22

An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 48: Configuration line-out or headphone

Mode	R2207	R2209	R2210	R2211	Remark
Headphone	n.a.	n.a.	0 Ω	0 Ω	–
Line-out	0 Ω	0 Ω	n.a.	n.a.	Default

Table 49: Pinout Microphone – X19

Pin	Signal	Remark
1	AGND_AUDIO	–
2A, 2B	MIC_IN	2.2 kΩ in series to MIC_BIAS + ESD protection
3	AGND_AUDIO	10 kΩ to AGND_AUDIO, right channel not used (only mono)

Table 50: Pinout Line-In – X20

Pin	Signal	Remark
1	AGND_AUDIO	–
2A, 2B	LINE_IN_L	470 nF in series + ESD protection
3	LINE_IN_R	470 nF in series + ESD protection

Table 51: Pinout Line-Out – X21

Pin	Signal	Remark
1	AGND_AUDIO	–
2A, 2B	AUDIO_OUT_L	1 µF +100 Ω in series; 47 nF to AGND_AUDIO+ ESD protection; optional connection to HP_L + ESD protection
3	AUDIO_OUT_R	1 µF +100 Ω in series; 47 nF to AGND_AUDIO+ ESD protection; optional connection to HP_R + ESD protection

Table 52: Type of audio jack

Manufacturer / part number	Description
Yamaichi / LJE3530K	Jack 3.5 mm

4.2.9 SD card

The SD card connector is directly connected to the SDHC controller on the TQMa6ULx with a 4-bit wide data interface.
The SDHC controller on the TQMa6ULx supports the UHS-I mode, but it is not used on the MBa6ULx.
Therefore, the maximum available is the High-Speed mode. All data lines provide ESD protection.
Booting from SD card is possible (see chapter 4.3.5).

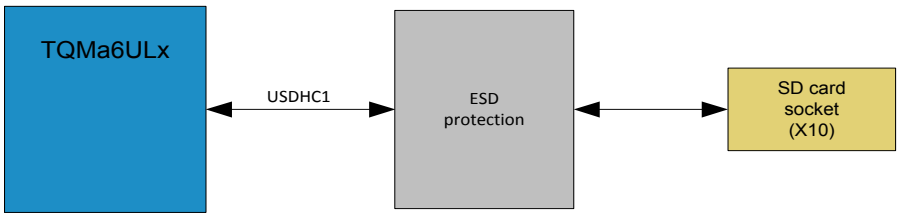


Illustration 29: Block diagram SD card

The read and write speeds of the SD card interface depend on the SD card used.

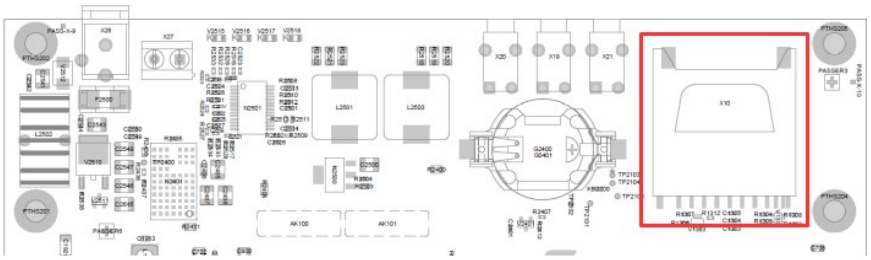


Illustration 30: Position of SD card – X10

Table 53: Pinout SD card – X10

Pin	Signal	Remark
1	USDHC1.DAT3	10 kΩ Pull-Up to VCC3V3 + ESD protection
2	USDHC1.CMD	10 kΩ Pull-Up to VCC3V3 + ESD protection
3	DGND	–
4	VCC3V3	–
5	USDHC1.CLK	ESD protection
6	DGND	–
7	USDHC1.DAT0	10 kΩ Pull-Up to VCC3V3 + ESD protection
8	USDHC1.DAT1	10 kΩ Pull-Up to VCC3V3 + ESD protection
9	USDHC1.DAT2	10 kΩ Pull-Up to VCC3V3 + ESD protection
CDS	USDHC1.CD#	10 kΩ Pull-Up to VCC3V3 + ESD protection
COM	DGND	–
WP	USDHC1.WP	10 kΩ Pull-Up to VCC3V3 + ESD protection
M1, M2	DGND	SHIELD

Table 54: Type of SD card connector

Manufacturer / part number	Description
Yamaichi / FPS009-2405-0	SD-/MMC card connector

4.2.10 Mini PCIe

The MBa6ULx provides a Mini PCIe slot for full-size cards. The USB and I²C signals are routed to the interface, see Table 57. According to the standard, the slot accepts cards with 50.95 × 30 mm. The connector socket is located 3.71 mm above the board. Every standard Mini PCIe card can be used. [17]
A SIM card holder to connect an UMTS / GSM modem is also available.

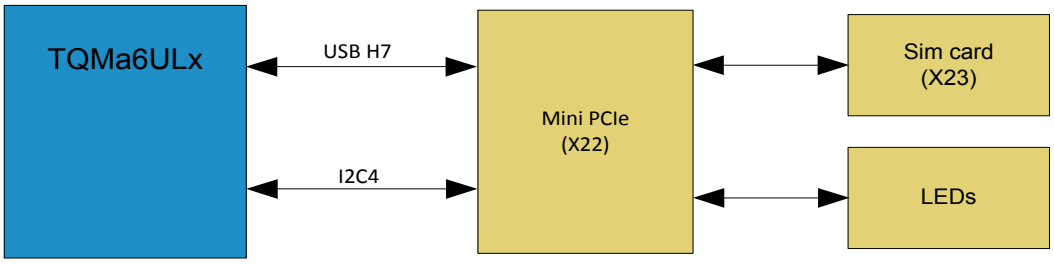


Illustration 31: Block diagram Mini PCIe

The maximum load on the voltages provided for the Mini PCIe card is given in the following table.

Table 55: Current load Mini PCIe

Parameter	I_{max}	Remark
Current @ 3.3 V	1.1 A	VCC3V3_MPCIE
Current @ 1.5 V	0.375 A	VCC1V5

Note:	5 V SIM card
	SIM cards, which require a 5 V supply are not supported!

Note:	Space between PCB and PCIe card
	The space between PCB and PCIe card has to be taken into account!

17: If suitable Mini PCIe card driver software is provided.

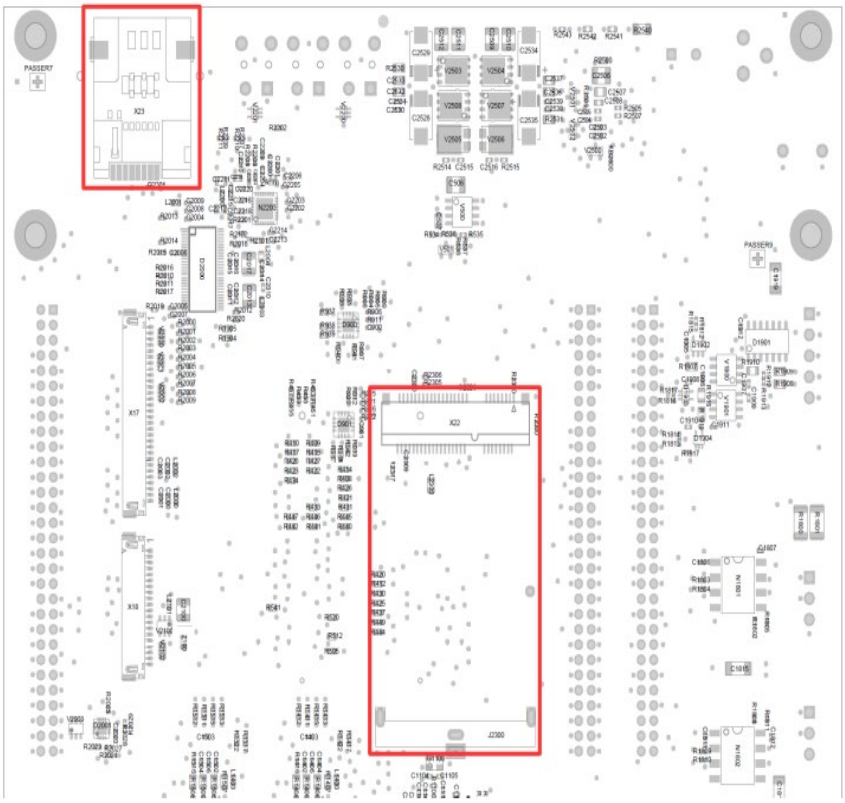


Illustration 32: Position of Mini PCIe + SIM card

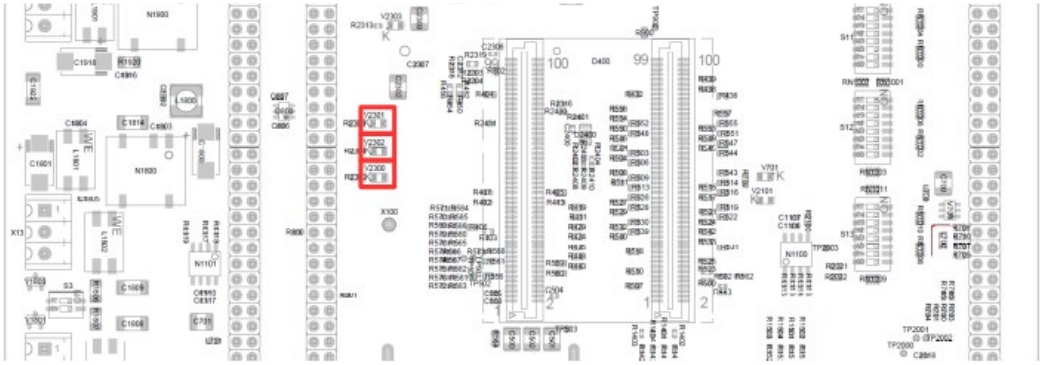


Illustration 33: Position of Mini PCIe status LEDS

Table 56: Mini PCIe interface, components

Manufacturer / part number	Description
Nexus / 5020HB56R	52-pin Mini PCIe connector
Nexus / 5022M56R	Mini PCIe holder
YAMAICHI / FMS006Z-2101-0	8-pin SIM card holder

Table 57: Pinout Mini PCIe – X22

Pin	Signal	Remark
1	PCIE_WAKE#	–
2	VCC3V3_MPCIE	See Table 55
3	NC	–
4	DGND	–
5	NC	–
6	VCC1V5	See Table 55
7	NC	–
8	UIM_PWR	SIM card signal, see Table 58
9	DGND	–
10	UIM_DATA	SIM card signal, see Table 58
11	NC	–
12	UIM_CLK	SIM card signal, see Table 58
13	NC	–
14	UIM_RST	SIM card signal, see Table 58
15	DGND	–
16	UIM_VPP	SIM card signal, see Table 58
17	NC	–
18	DGND	–
19	NC	–
20	PCIE_DIS#	–
21	DGND	–
22	PCIE_RST#	–
23	NC	–
24	VCC3V3_MPCIE	See Table 55
25	NC	–
26	DGND	–
27	DGND	–
28	VCC1V5	See Table 55
29	DGND	–
30	I242.SCL	–
31	NC	–
32	I2C4.SDA	For I2C4 address mapping see Table 7
33	NC	–
34	DGND	–
35	DGND	–
36	USB_H7_D_N	Common mode choke in series
37	DGND	–
38	USB_H7_D_P	Common mode choke in series
39	VCC3V3_MPCIE	See Table 55
40	DGND	–
41	VCC3V3_MPCIE	See Table 55
42	LED_WWAN#	In series with 330 Ω and green LED at VCC3V3_MPCIE
43	DGND	–
44	LED_WLAN#	In series with 330 Ω and green LED at VCC3V3_MPCIE
45	NC	–
46	LED_WPAN	In series with 330 Ω and green LED at VCC3V3_MPCIE
47	NC	–
48	VCC1V5	See Table 55
49	NC	–
50	DGND	–
51	NC	–
52	VCC3V3_MPCIE	See Table 55

Table 58: Pinout SIM card – X23

Pin	Signal	Remark
C1	UIM_PWR	–
C2	UIM_RST	–
C3	UIM_CLK	–
C5	DGND	–
C6	UIM_VPP	–
C7	UIM_DATA	–
SW1, SW2	NC	–

4.2.11 Headers

The MBa6ULx is equipped with several headers. All unused signals are made available on these.
In addition to the signals, 3.3 V, 5 V and 12 V are provided on each header.
Each voltage rail can be loaded with 3 A, accumulated over all pins of a voltage.

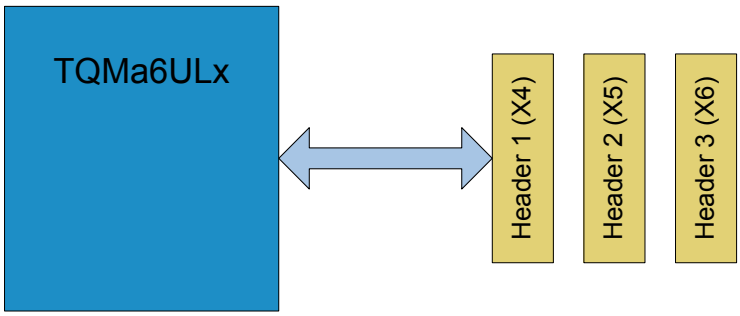


Illustration 34: Block diagram of Starterkit headers – X4, X5, X6

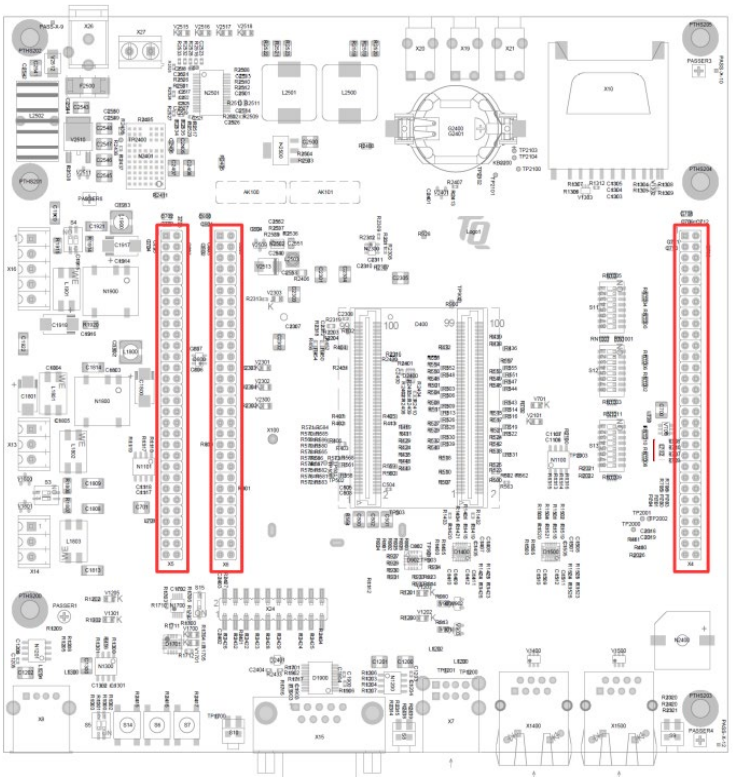


Illustration 35: Position of Starterkit headers – X4, X5, X6

Table 59: Type of headers

Manufacturer / part number	Description
Fischer Elektronik / SL 22 124 60 G	Header, 100 mil pitch, 2 × 30 pins

Table 60: Pinout header 1 – X4

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
LCD	LCD.CLK	7	8	LCD.ENABLE	LCD
LCD	LCD.HSYNC	9	10	LCD.DAT3	LCD
LCD	LCD.VSYNC	11	12	LCD.DAT5	LCD
LCD	LCD.DAT2	13	14	LCD.DAT7	LCD
LCD	LCD.DAT4	15	16	LCD.DAT11	LCD
LCD	LCD.DAT6	17	18	LCD.DAT13	LCD
LCD	LCD.DAT10	19	20	LCD.DAT15	LCD
LCD	LCD.DAT12	21	22	LCD.DAT19	LCD
LCD	LCD.DAT14	23	24	LCD.DAT21	LCD
LCD	LCD.DAT18	25	26	LCD.DAT23	LCD
LCD	LCD.DAT20	27	28	LCD.DAT0	LCD
LCD	LCD.DAT22	29	30	LCD.DAT1	LCD
LCD	LCD.DAT8	31	32	LCD.DAT9	LCD
LCD	LCD.DAT16	33	34	USB_H4_VBUS	Power
LCD	LCD.DAT17	35	36	USB_H4_D_N	USB4
Power	DGND	37	38	USB_H4_D_P	USB4
I2C4	I2C4.SCL	39	40	DGND	Power
I2C4	I2C4.SDA	41	42	SPI2.CS0	SPI2
SPI2	SPI2.MOSI	43	44	SPI2.MISO	SPI2
–	NC	45	46	SPI2.SCLK	SPI2
LCD	LCD.INT#	47	48	DGND	Power
LCD	LCD.PWR_EN	49	50	LCD.BLT_EN	LCD
STKRST	STKRST#	51	52	LCD.CONTRAST	LCD
Power	DGND	53	54	DGND	Power
Touch	TOUCH.Y+	55	56	TOUCH.X+	Touch
Touch	TOUCH.Y–	57	58	TOUCH.X–	Touch
Power	DGND	59	60	DGND	Power

Table 61: Pinout header 2 – X5

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
QSPI	QSPI_A.SCK	7	8	QSPI_A.SS1#	QSPI
QSPI	QSPI_A.DAT0	9	10	QSPI_A.DAT1	QSPI
QSPI	QSPI_A.DAT2	11	12	QSPI_A.DAT3	QSPI
–	NC	13	14	NC	–
Power	DGND	15	16	DGND	Power
UART3	UART3.RTS#	17	18	UART3.CTS#	UART3
SAI	SAI1.MCLK	19	20	SAI1.TX_SYNC	SAI1
SAI	SAI1.TX_BCLK	21	22	SAI1.RX_DATA	SAI1
SAI	SAI1.TX_DATA	23	24	DGND	Power
Power	DGND	25	26	DCAN1.TX	DCAN
UART6	UART6.RTS#	27	28	DCAN1.RX	DCAN
UART6	UART6.CTS#	29	30	DCAN2.TX	DCAN
–	NC	31	32	DCAN2.RX	DCAN
Power	DGND	33	34	DGND	Power
SPI2	SPI2.MOSI	35	36	SPI2.MISO	SPI2
SPI2	SPI2.SCLK	37	38	SPI2.CS0	SPI2
Power	DGND	39	40	DGND	Power
UART1	UART1.RX	41	42	UART1.TX	UART1
Power	DGND	43	44	DGND	Power
UART3	UART3.RX	45	46	UART3.TX	UART3
Power	DGND	47	48	DGND	Power
UART6	UART6.RX	49	50	UART6.TX	UART6
Power	DGND	51	52	DGND	Power
Power	USB_H6_VBUS	53	54	NC	–
USB6	USB_H6.D_N	55	56	NC	–
USB6	USB_H6.D_P	57	58	NC	–
Power	DGND	59	60	DGND	Power

Table 62: Pinout header 3 – X6

Group	Signal	Pin		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
WDOG1	WDOG1#	7	8	NC	–
RES1	RES1.SPARE1	9	10	NC	–
RES2	RES1.SPARE2	11	12	NC	–
–	NC	13	14	NC	–
–	NC	15	16	NC	–
–	NC	17	18	MX6UL_ONOFF	MX6UL on/off
–	NC	19	20	DGND	Power
Power	DGND	21	22	SNVS_TAMPER.0	Tamper
Reset	RESET_IN#	23	24	SNVS_TAMPER.1	Tamper
Reset	RESET_OUT#	25	26	SNVS_TAMPER.2	Tamper
–	NC	27	28	SNVS_TAMPER.3	Tamper
Ext. Wakeup	EXT_WAKEUP	29	30	SNVS_TAMPER.4	Tamper
Power	DGND	31	32	SNVS_TAMPER.5	Tamper
Tamper	SNVS_TAMPER.6	33	34	SNVS_TAMPER.7	Tamper
Tamper	SNVS_TAMPER.8	35	36	SNVS_TAMPER.9	Tamper
Power	DGND	37	38	DGND	Power
LICELL	LICELL [18]	39	40	NC	–
EMMC	EMMC.D7	41	42	PMIC_PWRON	PMIC
EMMC	EMMC.D6	43	44	NC	–
EMMC	EMMC.D5	45	46	TEMP_OS#	TEMP
EMMC	EMMC.D4	47	48	VSNVS_REF_OUT [18]	VSNVS
Power	DGND	49	50	DGND	Power
EMMC	EMMC.D3	51	52	BUZZER	Buzzer
EMMC	EMMC.D2	53	54	EMMC.RST#	EMMC
EMMC	EMMC.D1	55	56	EMMC.CMD	EMMC
EMMC	EMMC.D0	57	58	EMMC.SCK	EMMC
Power	DGND	59	60	DGND	Power

18: 100 Ω in series on MBa6ULx.

4.3 Diagnostic- and user interfaces

4.3.1 Diagnostic LEDs

The MBa6ULx provides 22 diagnostic and status LEDs to indicate the system condition.
The following table lists the function of each LED.

Table 63: Meaning of diagnostic LEDs

Interface	Reference	Colour	Signal
USB	V1202	green	VBUS USB Host 1 (lights up when VBUS of USB Host 1 is active)
	V1203	green	VBUS USB Host 2 (lights up when VBUS of USB Host 2 is active)
	V1205	green	VBUS USB Host 3 (lights up when VBUS of USB Host 3 is active)
	V701	green	VBUS USB Host 4 (lights up when VBUS of USB Host 4 is active)
	V2101	green	VBUS USB Host 5 (lights up when VBUS of USB Host 5 is active)
USB OTG	V1301	green	VBUS USB OTG 8 (lights up when VBUS of USB OTG is active)
Mini-PCIe	V2300	green	Mini-PCIe WWAN
	V2301	green	Mini-PCIe WLAN
	V2302	green	Mini-PCIe WPAN
	V2303	green	Status 3.3 V Mini-PCIe (lights up when supply 3.3 V for Mini-PCIe is active)
GPIO	V900	green	LED an Port-Expander Port (D902) IO2 (lights up when Port high)
	V901	green	LED an Port-Expander Port (D902) IO3 (lights up when Port high)
Power	V2515	green	Status 24 V (lights up when supply 24 V is active)
	V2516	green	Status 12 V (lights up when supply 12 V is active)
	V2517	green	Status 5 V (lights up when supply 5 V is active)
	V2518	green	Status 3.3 V (lights up when supply 3.3 V is active)
USB-Debug	V1700	green	TX-LED (lights up when transmission is active)
	V1701	green	RX-LED (lights up when transmission is active)
Ethernet	X1400C	yellow	Error-LED Ethernet 1 (lights up in case of error) (Speed-LED Ethernet 1)
	X1400B	green	Activity-LED Ethernet 1 (lights up when link is active, flashes during data transmission)
	X1500C	yellow	Error-LED Ethernet 2 (lights up in case of error) (Speed-LED Ethernet 2)
	X1500B	green	Activity-LED Ethernet 2 (lights up when link is active, flashes during data transmission)
Reset	V5	red	Reset-LED (lights up when TQMa6ULx is in reset)

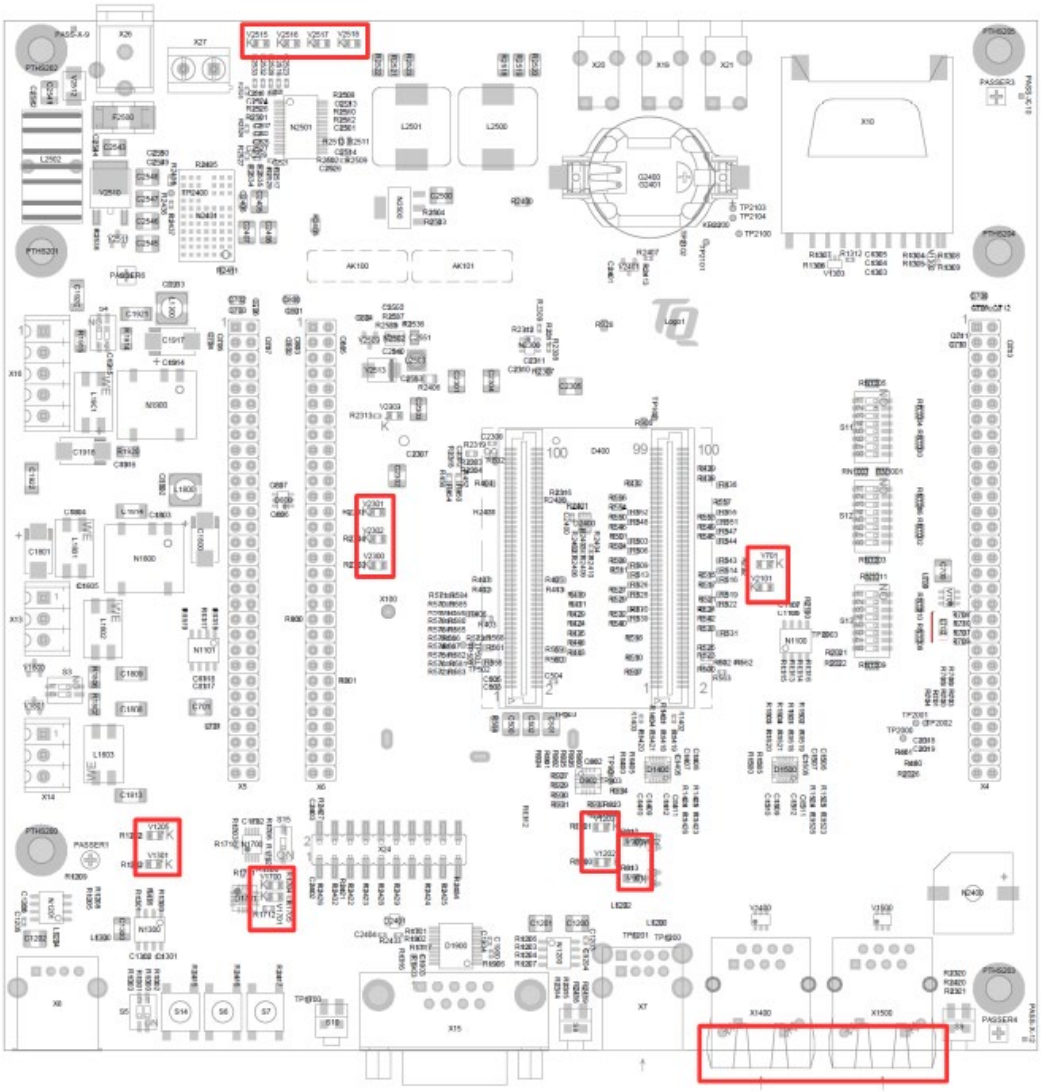


Illustration 36: Position of LEDs

Table 64: Type of LEDs

Manufacturer / part number	Description
Osram / LGR971-KN-1	SMD LED, green
Status LEDs Ethernet	See Table 32
Reset LED	See TQMa6ULx User's Manual

4.3.2 Navigation buttons

For development purposes, three navigation buttons on the MBa6ULx are connected to the port expander.
By using the signal GPIOEXP_IN_INT#, the port expander is interrupt-capable.
The signals between Button and Port Expander have 10 kΩ Pull-Up resistors to 3.3 V.
The buttons are not debounced in hardware. Hence, the buttons have to be debounced in software.

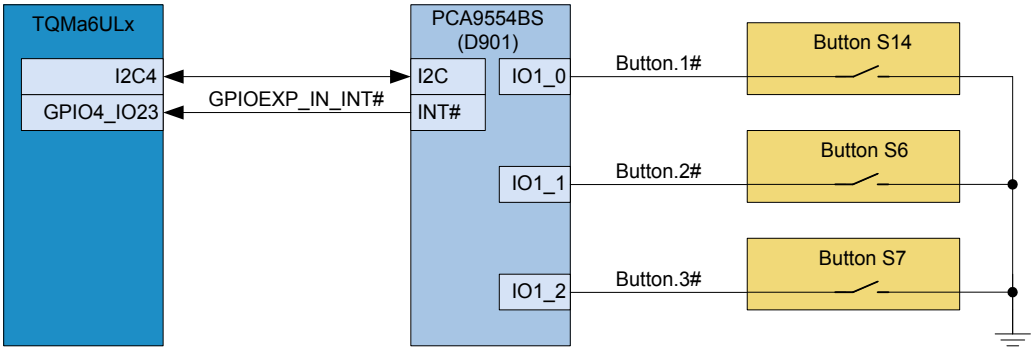


Illustration 37: Block diagram navigation buttons

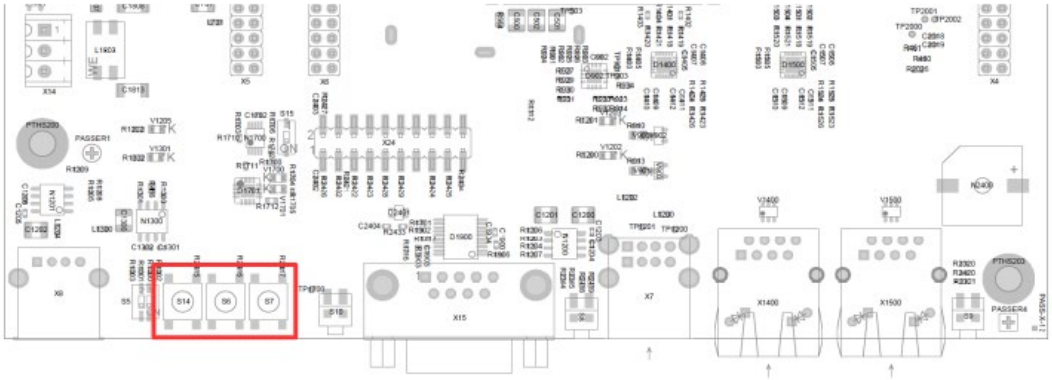


Illustration 38: Position of navigation buttons – S6, S7, S14

Table 65: Type of navigation buttons

Manufacturer / part number	Description
Knitter switch / TSS 61N	Push button

4.3.3 Power-On and Reset-button

For further information see chapter 4.1.6.

4.3.4 CAN and RS-485 termination

For further information see chapter 4.2.4 and 4.2.5.

4.3.5 Boot-Mode configuration

The TQMa6ULx can boot from different media:

- eMMC (on TQMa6ULx)
- QSPI NOR flash
- SD card
- Serial downloader via USB-OTG 1

The settings of DIP switches S11, S12, S13 and S5 determine, which device is selected to boot from. [19]
Each signal and its meaning regarding the boot process is to be taken from the TQMa6ULx User's Manual.
Please also visit https://support.tq-group.com/doku.php?id=en:arm:tqma6ulx:mba6ulx:dip_switches.

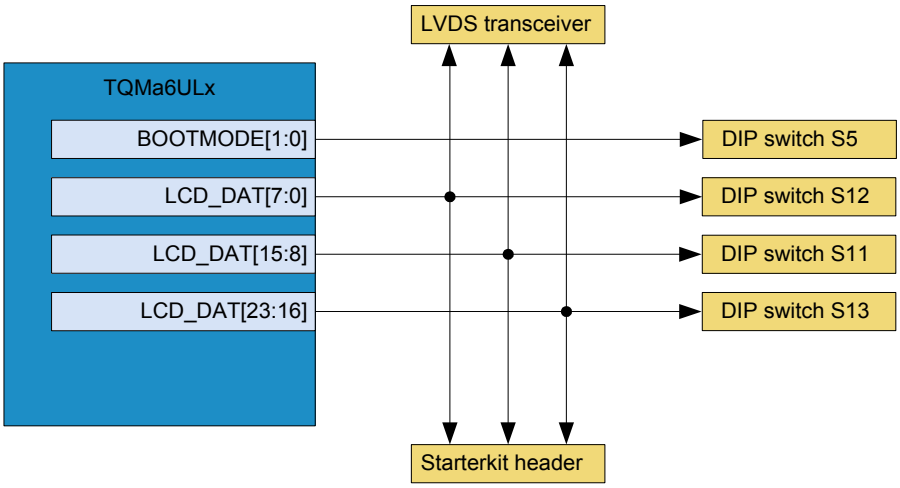


Illustration 39: Block diagram Boot-Mode

After reading the boot configuration and starting the bootloader, the boot configuration signals BOOT_CFG are used as parallel LCD signals and routed to the starter kit header and the LVDS transceiver, depending on the multiplexing.

Attention:	Customer specific design
	For EMC and signal quality reasons it is not recommended to connect the LCD interface to a header and an LVDS transceiver like on the MBa6ULx. On the MBa6ULx, the interface was only implemented in this way to provide the function. In each customer design, the LCD interface should be as short as possible and designed as a direct connection.

The following tables describe the DIP switch settings for each boot media.
Further settings such as transfer modes and CPU clock are to be taken from the TQMa6ULx User's Manual (8).
With DIP switch S5, switch position "ON" means logical "1", switch position "OFF" means logical "0".

Table 66: Boot-Mode configuration

Boot-Mode	S5-2, BOOT_MODE1	S5-1, BOOT_MODE0
Boot from eFuses	Low (OFF)	Low (OFF)
Serial Downloader	Low (OFF)	High (ON)
Internal Boot [20]	High (ON)	Low (OFF)
Reserved	High (ON)	High (ON)

19: Only applies to TQMa6ULx with unburnt eFuses.
20: Boot configuration is set with DIP switches S11, S12, S13 and S5.

Attention:	DIP switch S5 on MBa6ULx revision 01xx and revision 02xx
	The switches of DIP switch S5 are twisted between MBa6ULx revision 01xx and 02xx. The following table shows the assignment.

Table 67: DIP switch S5 assignment

MBa6ULx revision	DIP switch S5	Signal
01xx	Switch 1	BOOT_MODE1
	Switch 2	BOOT_MODE0
02xx	Switch 1	BOOT_MODE0
	Switch 2	BOOT_MODE1

With DIP switch S5, switch position "OFF" means “low”, switch position "ON" means “high”.
DIP switches S11, S12 and S13 operate inverted. Switch position "OFF" means “high”, switch position "ON" means “low”.

Table 68: Boot-Mode configurations – S11, S12, S13, and S5 [21]

DIP switch		Signal	eMMC	SD card	QSPI NOR	Serial-Downloader
S5	1	BOOT_MODE0	Low (OFF)	Low (OFF)	Low (OFF)	High (ON)
	2	BOOT_MODE1	High (ON)	High (ON)	High (ON)	Low (OFF)
S12	1	LCD.DAT0	Low (ON)	Low (ON)	Low (ON)	X
	2	LCD.DAT1	Low (ON)	Low (ON)	Low (ON)	X
	3	LCD.DAT2	X	**High (OFF)**	Low (ON)	X
	4	LCD.DAT3	Low (ON)	Low (ON)	Low (ON)	X
	5	LCD.DAT4	Low (ON)	Low (ON)	**High (OFF)**	X
	6	LCD.DAT5	**High (OFF)**	Low (ON)	Low (ON)	X
	7	LCD.DAT6	**High (OFF)**	**High (OFF)**	Low (ON)	X
	8	LCD.DAT7	Low (ON)	Low (ON)	Low (ON)	X
S11	8	LCD.DAT8	Low (ON)	Low (ON)	Low (ON)	X
	7	LCD.DAT9	Low (ON)	Low (ON)	Low (ON)	X
	6	LCD.DAT10	Low (ON)	Low (ON)	Low (ON)	X
	5	LCD.DAT11	**High (OFF)**	Low (ON)	Low (ON)	X
	4	LCD.DAT12	Low (ON)	Low (ON)	Low (ON)	X
	3	LCD.DAT13	Low (ON)	**High (OFF)**	Low (ON)	X
	2	LCD.DAT14	**High (OFF)**	Low (ON)	Low (ON)	X
	1	LCD.DAT15	Low (ON)	Low (ON)	Low (ON)	X
S13	8	LCD.DAT16	Low (ON)	Low (ON)	Low (ON)	X
	7	LCD.DAT17	Low (ON)	Low (ON)	Low (ON)	X
	6	LCD.DAT18	Low (ON)	Low (ON)	Low (ON)	X
	5	LCD.DAT19	Low (ON)	Low (ON)	Low (ON)	X
	4	LCD.DAT20	Low (ON)	Low (ON)	Low (ON)	X
	3	LCD.DAT21	Low (ON)	Low (ON)	Low (ON)	X
	2	LCD.DAT22	Low (ON)	Low (ON)	Low (ON)	X
	1	LCD.DAT23	Low (ON)	Low (ON)	Low (ON)	X

21: DIP switch settings: 0 = OFF | 1 = ON | X = don’t care.

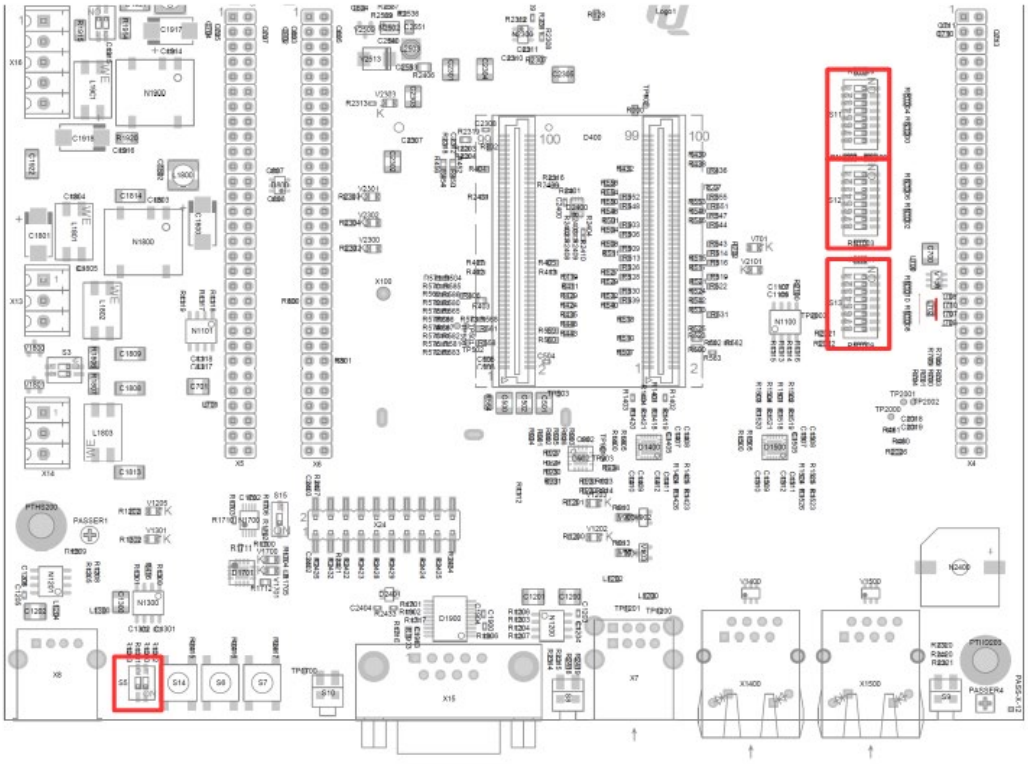


Illustration 40: Position of Boot-Mode configuration switches – S5, S11, S12, S13

Table 69: Types of Boot-Mode DIP switches

Manufacturer / part number	Description
Nidec Copal / CHS-08TA	8-fold DIP switch, 1.27 mm pitch
Nidec Copal / CHS-02TA	2-fold DIP switch, 1.27 mm pitch

4.3.6 Buzzer

The MBa6ULx provides a buzzer to signal acoustic events. The buzzer is controlled via a port expander.

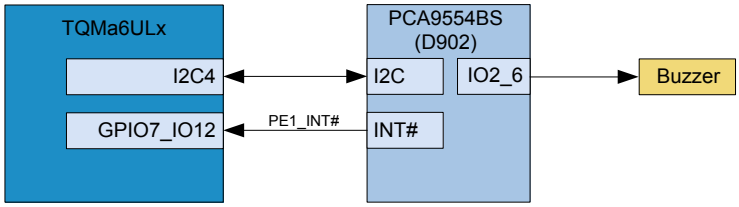


Illustration 41: Block diagram buzzer

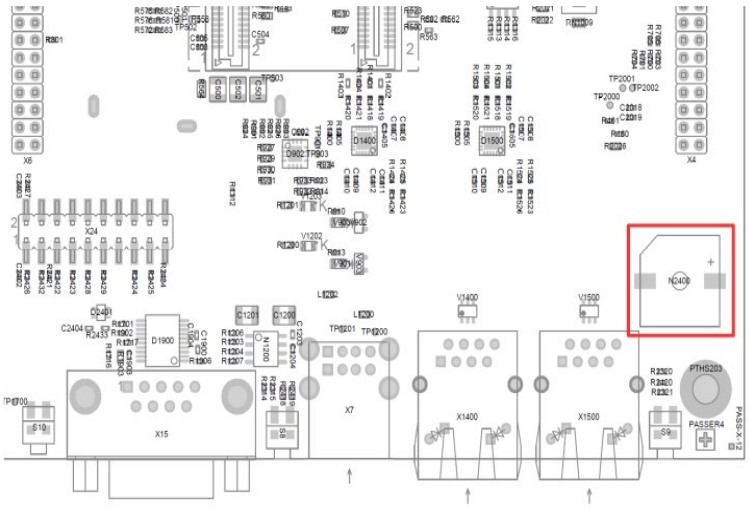


Illustration 42: Position of buzzer – N2400

Table 70: Type of buzzer

Manufacturer / part number	Description
PUI Audio / SMI-1324-TW-5V-2-R	Buzzer, 5 V (typ.), 30 mA (max.), 2.4 kHz ±400 Hz

4.3.7 JTAG

The JTAG interface is routed to a 20-pin header X24. The pull-ups required for lines TDI, TMS, TRST# and SRST# are provided on the MBa6ULx. All signals have 3.3 V level. The JTAG interface is not ESD protected. The JTAG mode can be configured by an assembly option. Information can be found in the MBa6ULx schematics.

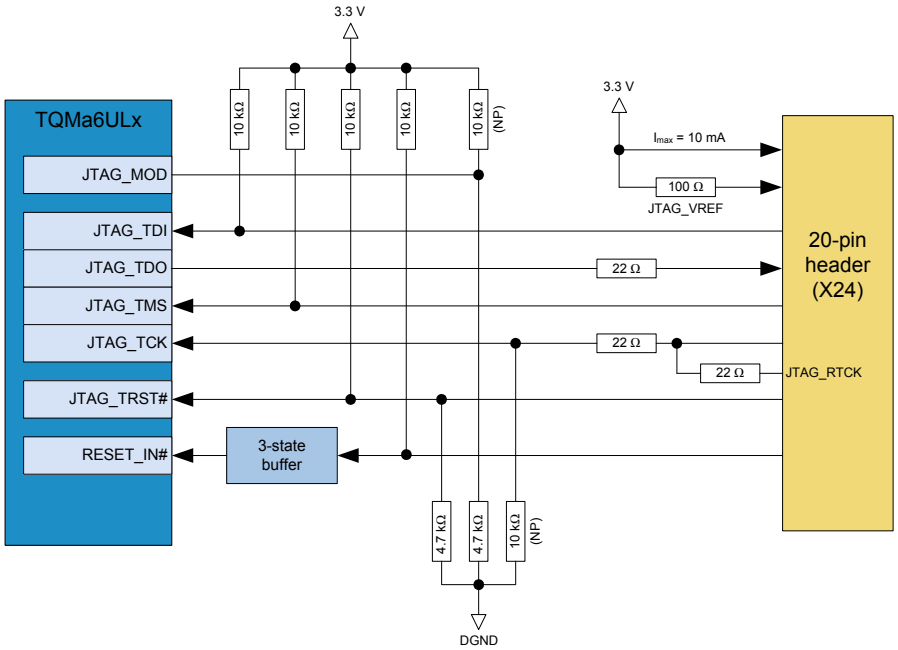


Illustration 43: Block diagram JTAG

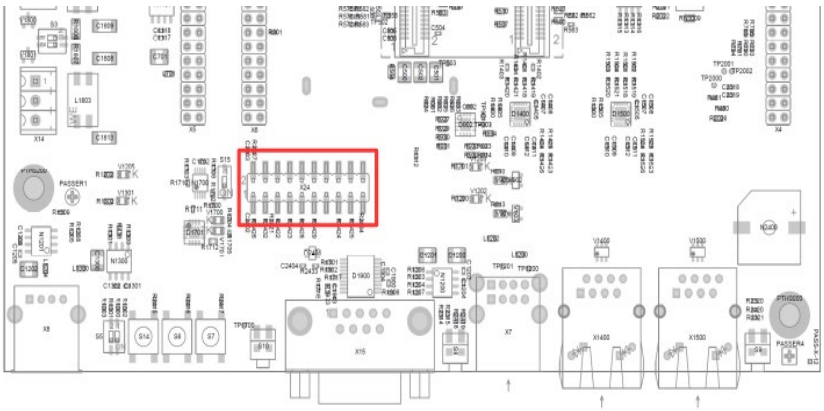


Illustration 44: Position of JTAG – X25

Table 71: Type of JTAG connector

Manufacturer / part number	Description
Fischer Elektronik / SL-11-SMD-052-20-G-BTR	Header, 100 mil pitch, 2 × 10 pins

The following table shows the pinout of the JTAG connector.

Table 72: Pinout JTAG – X24

Pin	Signal	Direction	Remark
1	JTAG.VREF	P	100 Ω in series to VCC3V3, use as reference only!
2	VCC3V3	P	0 Ω in series to VCC3V3, I_{max} = 10 mA
3	JTAG.TRST#	I	10 kΩ Pull-Up to VCC3V3
4	DGND	P	–
5	JTAG.TDI	I	10 kΩ Pull-Up to VCC3V3
6	DGND	P	–
7	JTAG.TMS	I	10 kΩ Pull-Up to VCC3V3
8	DGND	P	–
9	JTAG.TCK	I	22 Ω in series
10	DGND	P	–
11	JTAG.RTCK	I	2 × 22 Ω in series
12	DGND	P	–
13	JTAG.TDO	O	22 Ω in series
14	DGND	P	–
15	JTAG.SRST#	I	10 kΩ Pull-Up to VCC3V3, Open-Drain-Buffer at RESET_IN#
16	DGND	P	–
17	VCC3V3	P	10 kΩ in series to VCC3V3
18	DGND	P	–
19	DGND	P	10 kΩ in series to DGND
20	DGND	P	–

5. MECHANICS

5.1 Dimensions

The design of the MBa6ULx is based on the Mini-ITX form factor (170 × 170 mm²) and has a maximum height of approximately 27 mm. The MBa6ULx has six 4.3 mm holes for mounting in a housing and weighs approximately 230 grams without TQMa6ULx.

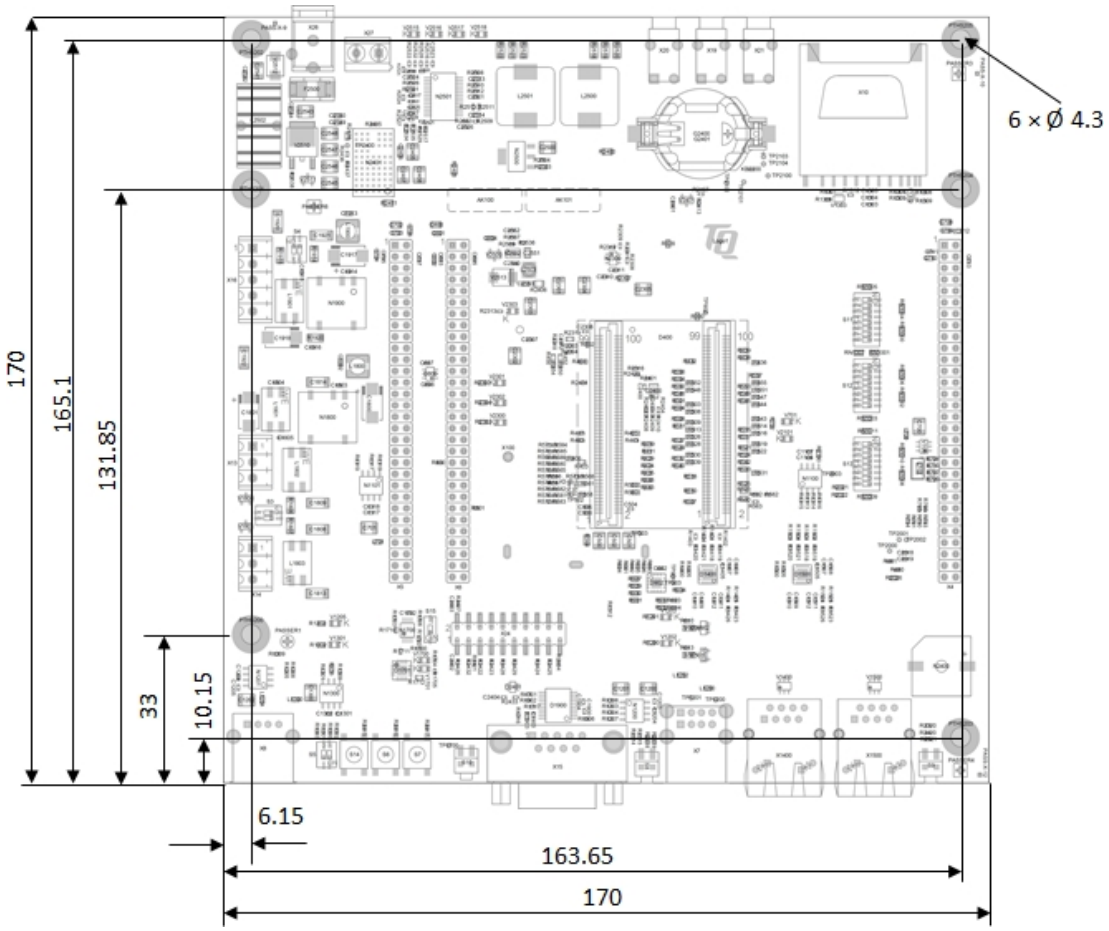


Illustration 45: MBa6ULx dimensions

Attention:	Destruction or malfunction!
	To avoid damages caused by mechanical stress, the TQMa6ULx may only be extracted from the carrier board by using the extraction tool MOZIa6ULx. 2.5 mm should be kept free on the carrier board, on both long sides of the TQMa6x for the extraction tool MOZIa6ULx.

5.2 Thermal management

No special precautions were taken concerning the thermal management of the MBa6ULx. A maximum of 5 W, including TQMa6x, have to be dissipated. More information is to be taken from the TQMa6ULx User's Manual.

Attention:	Destruction or malfunction
	The i.MX6ULx belongs to a performance category in which a cooling system is essential in most applications. It is the sole responsibility of the user to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board curvature, BGA balls, BGA package, thermal pad, heatsink) must be ensured when connecting the heat sink. The CPU is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa6ULx and thus malfunction, deterioration or destruction.

5.3 Assembly

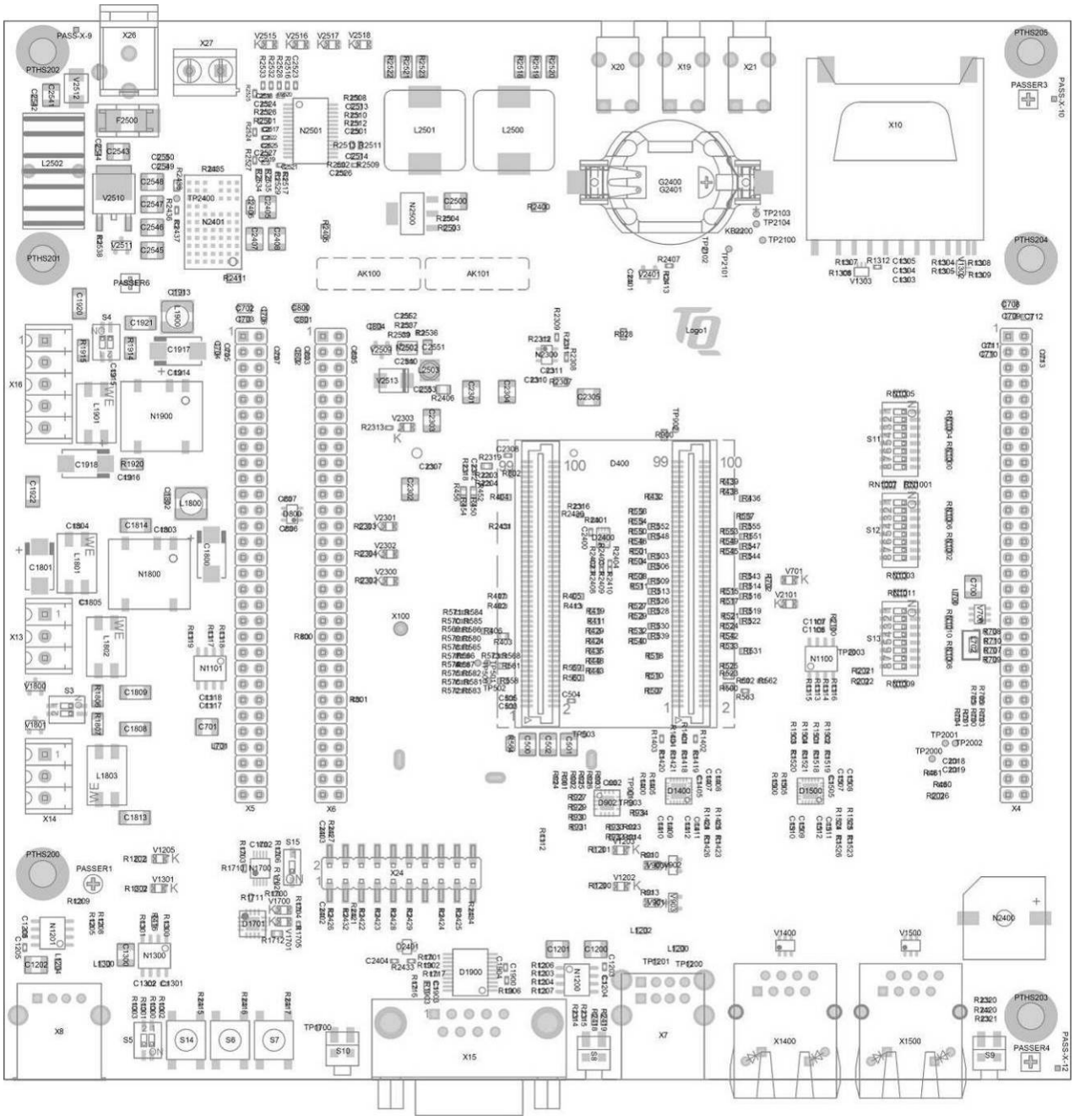


Illustration 46: Component placement top

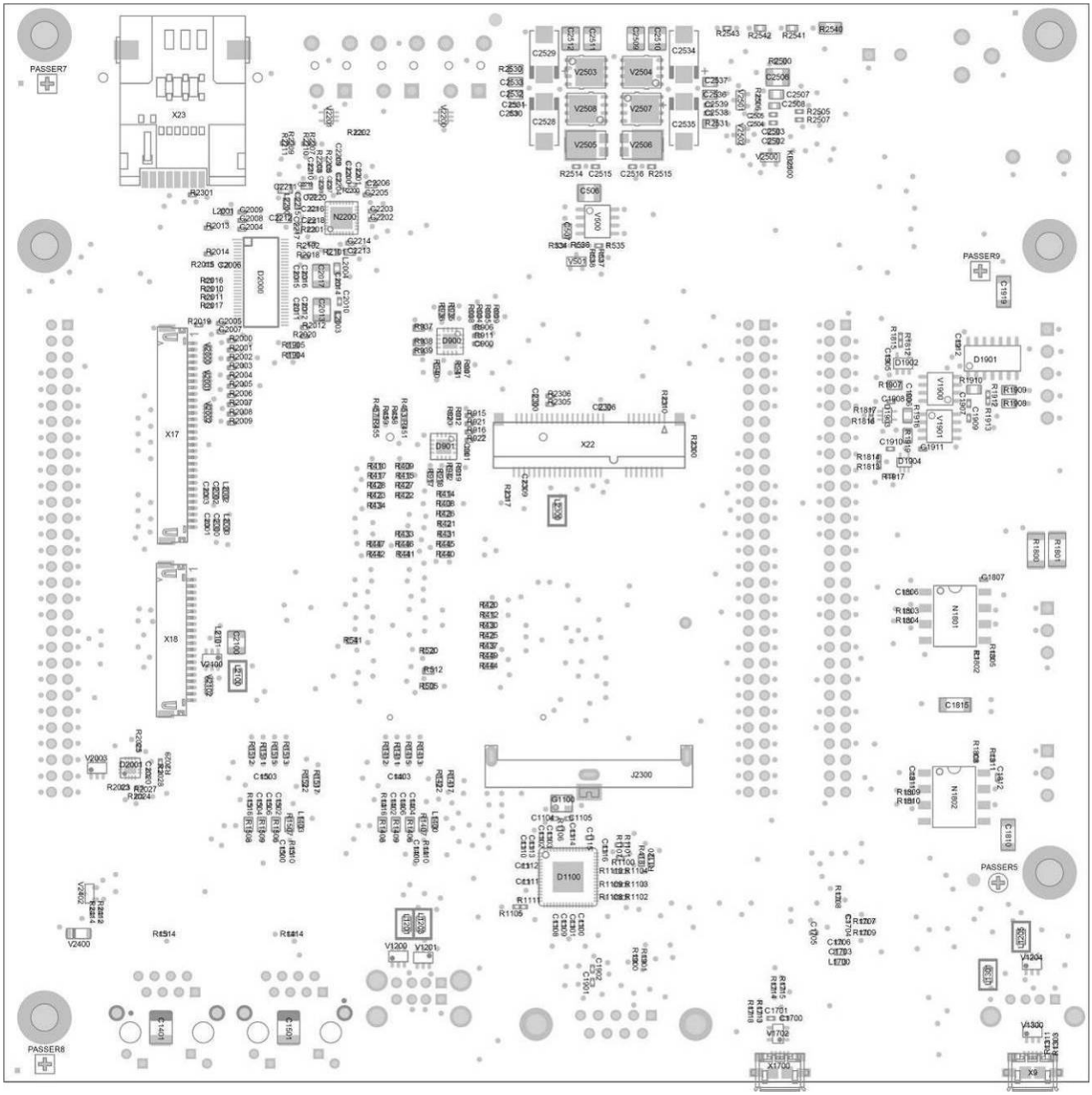


Illustration 47: Component placement bottom

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Because the MBa6ULx is a development platform, no EMC specific tests have been carried out.

Nevertheless DIN EN 55022:2010 class A was taken into account during development:

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

6.2 ESD

Most of the interfaces on the MBa6ULx are protected against electrostatic discharge. [22]
The interfaces, which provide an ESD protection is to be taken from the circuit diagram.

6.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety have not been carried out.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 73: Climatic and operational conditions MBa6ULx (without TQMa6ULx)

Parameter	Range	Remark
Permitted environmental temperature	0 °C to +70 °C	Without Lithium battery CR2032
Permitted environmental temperature	0 °C to +60 °C	With Lithium battery CR2032
Permitted storage temperature	–10 °C to +60 °C	With Lithium battery CR2032
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

7.1 Protection against external effects

Protection class IP00 was defined for the MBa6ULx. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa6ULx.

The MBa6ULx is designed to be insensitive to vibration and impact.

High quality industrial grade connectors are assembled on the MBa6ULx.

22: The JTAG and PMIC interfaces do not provide ESD protection.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa6ULx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa6ULx was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa6ULx must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBa6ULx enable compliance with EuP requirements for the MBa6ULx.

8.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa6ULx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The MBa6ULx is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

Due to technical reasons a battery is necessary for this product. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa6ULx, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 74: Acronyms

Acronym	Meaning
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrienorm)
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
FFC	Flat Flex Cable
FIT	Failure In Time
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MAC	Media Access Control
mPCIe	Mini PCIe
MTBF	Mean operating Time Between Failures
n.a.	Not Assembled
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go

Table 74: Acronyms (continued)

Acronym	Meaning
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RFU	Reserved for Future Usage
RJ45	Registered Jack 45
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SAI	Serial Audio Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identity Module
SMD	Surface-Mounted Device
SPI	Serial Peripheral Interface
THT	Through-Hole Technology
TSSOP	Thin-Shrink Small Outline Package
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High Speed
UM	User's Manual
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 75: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 6UltraLite Applications Processor Reference Manual, IMX6ULRM	Rev. 1, 04/2016	NXP
(2)	i.MX 6UltraLite Applications Processor for Industrial Products Data Sheet, IMX6ULIEC	Rev. 1, 04/2016	NXP
(3)	i.MX6UL & i.MX 6SL/SX/UL Power Management integrated circuit, PF3000	Rev. 7.0, 09/2016	NXP
(4)	i.MX 6UltraLite Power Consumption Measurement, AN5170_power	Rev. 2, 05/2016	NXP
(5)	i.MX 6UltraLite Chip Errata, IMX6ULCE	Rev. 1, 04/2016	NXP
(6)	i.MX 6UltraLite Applications Processor Hardware Development Guide, IMX6ULHDG	Rev. 1, 03/2016	NXP
(7)	USB2517 Data Sheet, USB251x	Rev. 1.1, 06.03.2014	SMSC
(8)	TQMa6ULx User's Manual	– current –	TQ-Systems
(9)	TQMa6ULx Support-Wiki	– current –	TQ-Systems

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